To our customers,

Old Company Name in Catalogs and Other Documents

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April 1st, 2010
Renesas Electronics Corporation

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	7 November 2000	No.	TN-SH7-274A/E
THEME	SH7615 usage notice of multiply/multiply and accumulate instruction execution		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents	■ Limitation on Use	
PRODUCT NAME	HD6417615AF/ARF		
REFERENCE DOCUMENTS	SH7615 Hardware manual	Effective Date: Permanent Lot#: ALL	

Multiplier access contention occurs by consecutive execution of multiply/multiply and accumulate instructions, and the stall cycle may be produced. If their stall cycle occur, sequence of instruction execution is reversed when S bit (saturation arithmetic bit) of SR register (status register) is changed right after the multiply and accumulate instruction. Then the instruction is executed after S bit is changed (it should be executed before the S bit is changed). Consequently, malfunction may occur on the operation.

The instructions affected by S bit change are,

Multiply and accumulate instruction : MAC.W and MAC.L instruction

<Condition & Phenomenon>

The following is an example of the condition.

1. Multiply/multiply and accumulate instructions

```
(1) DMULU.L   R4, R10          ; MUL.L, DMULS.L, DMULU.L and MAC.L come under (1).
(2) MAC.L   @R5+, @R5+         ; MAC.W and MAC.L come under (2). Multiplier access contention
                                  occurs, and stall cycle may be produced
(3) LDC     R0, SR             ; Change the saturation arithmetic mode
```

Multiplier access contention occurs between DMULU.L instruction(1) and MAC.L instruction(2), so MAC.L instruction execution(2) should be stalled. However, S bit change(3) is executed right before the MAC.L instruction execution(2) in the CPU due to the pipeline operation. Consequently, sequence of the execution(2) and (3) is reversed, and MAC.L operation result becomes inaccurate value. Instruction(1) corresponds to multiply/multiply and accumulate instructions. Instruction(2) corresponds to multiply and accumulate instructions.

<Workaround>

This problem can be avoided by any of the following workaround.

(1) Please do not execute SR register access right after multiply and accumulate instructions.

(2) Please insert NOP instruction right before LDC Rn, SR instruction.

(3) Please prevent the multiplier access contention (not to produce stall cycle).