To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

date: 2002/06/24

HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	MPU		No	TN-SH7-412A/E	Rev	1
THEME	SH7615/SH7616 limitation of DACKn output timing.	Classification of Information	1. Spec change 2. Supplement of Documents (3.) Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	HD6417615ARF HD6417616RF	Lot No. ALL	Reference Documents	SH7615 Hardware Manual ADE-602-198 Rev.1.0 SH7616 Hardware Manual ADE-602-243 Rev.1.0	Effective Date Permanent	

There is a limitation on use of internal Direct Memory Access Controller (DMAC) in SH7615/SH7616, and the countermeasures for this limitation are shown below.

[Phenomenon]

When all following conditions are met, SH7615/SH7616 DACKn(n=0,1) outputs with “Error timing”.

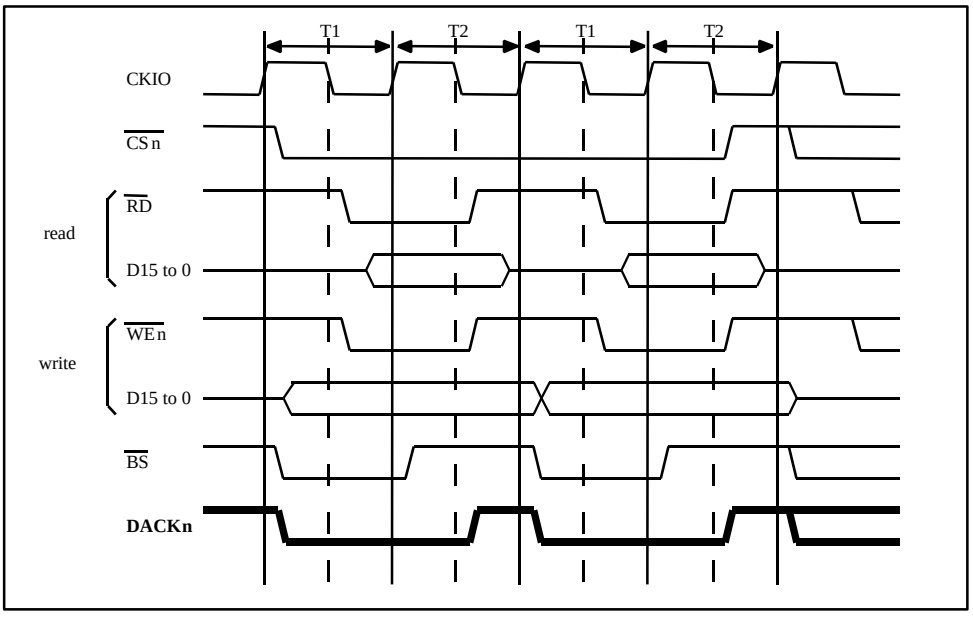
<Condition>

(1) Iø:Eø=1:1.

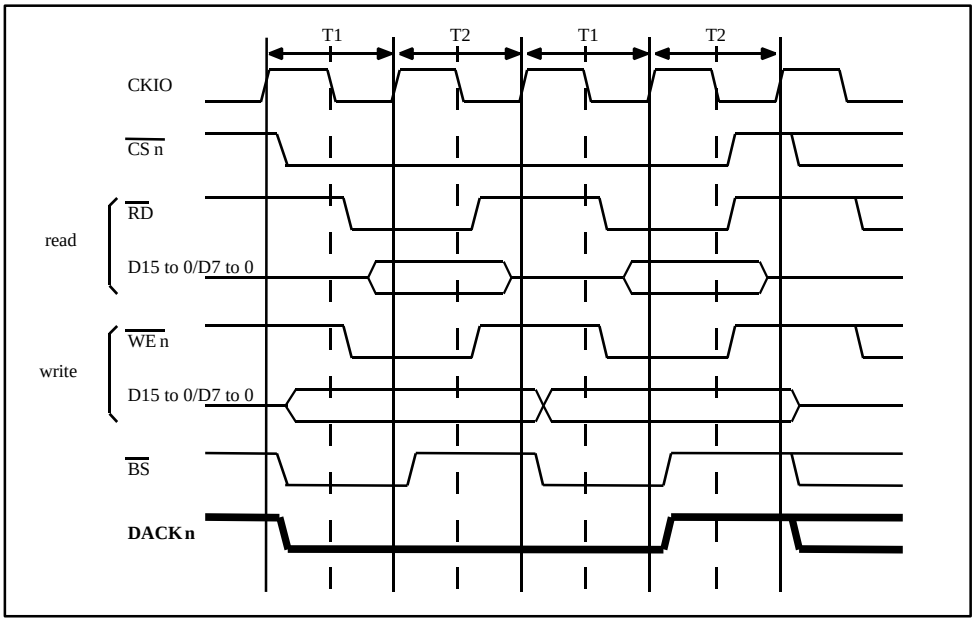
(2) DMA transfer to Ordinary space or Burst ROM.

(3) 16-byte/Long word DMA transfer on 16-bit bus width or 16-byte/Long word/Word DMA transfer on 8-bit bus width.

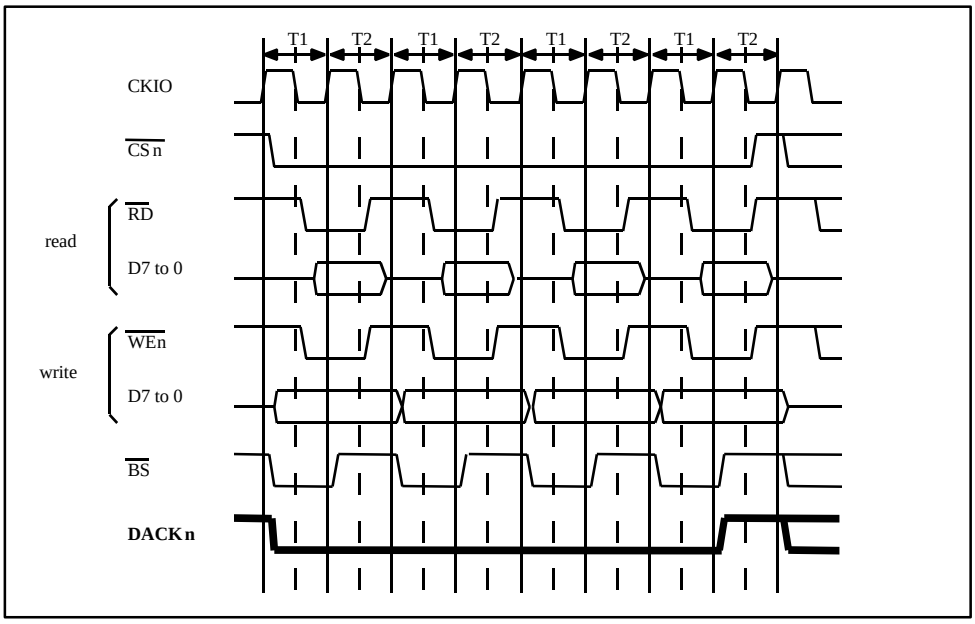
Correct timing



Error timing (1)



Error timing (2)



DACKn(n=0,1) assert timing and the number of repeat.

	16-byte unit	Long word unit	Word unit
16-bit bus width	Error timing(1) x 4	Error timing (1) x 1	———
8-bit bus width	Error timing(2) x 4	Error timing (2) x 1	Error timing(1) x 1

[Countermeasures]

This problem is avoided by any of the following countermeasures.

(1) Use frequency mode except Iø:Eø=1:1.

(2) Use 32-bit bus width.

(3) When the bus width is 16 bits, set DMA transfer size per Word unit or Byte unit.

(4) When the bus width is 8 bits, set DMA transfer size per Byte unit.