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April 1st, 2010
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HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	12 April 2001	No.	TN-SH7-312A/E
THEME	SH7615 limitation on use of Synchronous DRAM.		
CLASSIFICATION	☐ Spec change ■ Limitation on Use ☐ Supplement of Documents		
PRODUCT NAME	HD6417615ARF	Lot No.etc.	ALL
REFERENCE DOCUMENTS	SH7615 Hardware manual	Effective Date	Permanent

There is a limitation on use of Synchronous DRAM(SDRAM) in SH7615, and their countermeasures are shown below.

<Phenomenon>

In SDRAM burst write mode and bank active mode, there is a case that SH7615 outputs wrong SDRAM write data in any case below.

(1)Ethernet controller Direct Memory Access Controller(E-DMAC) transfers receive data to SDRAM as receive data buffer.

(2)DMAC executes 16byte transfer to SDRAM.

(3)Cache controller executes write-back to SDRAM.

<Condition>

When all following conditions are met, SH7615 drives wrong SDRAM write data on the first 4Byte of 16Byte.

(1)Frequency mode except External clock(Eø) freq. : Internal clock(Iø) freq.=1:1

(2)SDRAM burst write mode.

(3)SDRAM bank active mode.

(4)E-DMAC receives data transfer to SDRAM, or DMAC 16Byte transfer from an internal memory or peripheral module to SDRAM, or Cache controller write-back to SDRAM.

<Countermeasures>

This problem in SDRAM burst write mode is avoided by any of the following countermeasures.

(1)Use frequency mode in External clock(Eø) freq. : Internal clock(Iø) freq.=1:1

(2)Set to SDRAM auto pre-charge mode.