# **RENESAS TECHNICAL UPDATE**

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Product Category	MPU/MCU	Document No.	TN-SH7-A874A/E	Rev.	1.00	
Title	SH7450 Group, SH7451 Group User's Manu Hardware Errata Rev. B	Information Category	Technical Notification			
Applicable Product	SH7450 Group, SH7451 Group	Lot No.	Reference Document	SH7450 Group, SH74 User's Manual: Hardw (R01UH0286EJ0110)		

We inform you of the corrections of "SH7450 Group, SH7451 Group User's Manual: Hardware Rev. 1.10 (Published on September 27, 2011)".

When you use "SH7450 Group, SH7451 Group User's Manual: Hardware Rev. 1.10", should be used together the attached errata.

In addition, the corrections in the following are also included in the attached errata (Rev. B).

- Technical update TN-SH7-A826A/E: Errata (Rev. A)
- Technical update TN-SH7-A859A/E: Errata to User's Manual Regarding CAN Module

Attached document: "SH7450 Group, SH7451 Group User's Manual: Hardware Rev. 1.10" Errata Rev. B - 11 sheets



Rev.	Page	Part	Contents
Added in Rev. A	Page Revision History - xiii	Part 26.3.14 CANi Status Register	Contents         Revision History: Description of CAN is added.         -Page of Previous Edition: 26-49         -Description:         Description of the bit 1 (SDST bit) in the CANi Status Register (CiSTR) (i = 0 to 4 is corrected.         Error:       The SDST bit is set to "1" when at least one SENTDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register.         Correction:       The SDST bit is set to "1" when at least one SENTDATA bit in the CiMCTLj (j = 32 to 63) register is "1" regardless of the value of the CiMIER register.         -Page of Previous Edition: 26-49       -Description:         Description:       Description of the bit 0 (NDST bit) in the CANi Status Register (CiSTR) (i = 0 to 4 is corrected.         Error:       The NDST bit is set to "1" when at least one NEWDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register.         Correction:       The NDST bit is set to "1" when at least one NEWDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register.         Correction:       The NDST bit is set to "1" when at least one NEWDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register.
Added in Rev. A	Revision History - xv	32.5.1 FlexRay Error Interrupt Register	CiMIER register. Revision History: Description of FlexRay is added. -Page of Previous Edition: 32-17 -Description of the bit 24 (EDB bit) in the FlexRay Error Interrupt Register (FREIF is corrected. Error: 0: No error detected on channel B RW Correction: 0: No error detected on channel B -Page of Previous Edition: 32-18 -Description: Description of the bit 9 (IIBA bit) in the FlexRay Error Interrupt Register (FREIR) corrected. Error: 0: No illegal CPU access to <u>Output</u> Buffer occurred 1: Illegal CPU access to <u>Input</u> Buffer occurred 1: Illegal CPU access to <u>Input</u> Buffer occurred 1: Illegal CPU access to <u>Input</u> Buffer occurred
Added in Rev. A Added in Rev. A	Revision History - xvi 32-76	Appendix A CPU Operation Mode Register 32.7.1 FlexRay CC Status Vector Register	Revision History: Description of Appendix A is added.         -Page of Previous Edition: A-1         -Description:         Value after reset of the bit 5 (RABD bit) in the CPU Operation Mode Register (CPUOPM) is revised.         Error:       Value after reset of the RABD bit is "1"         Correction:       Value after reset of the RABD bit is "0"         Description of the bit 29 to 24 (PSL5 to PSL0 bit) in the FlexRay CC Status Vecto Register (FRCCSV) is corrected.         Error:       Set to B'000100 when leaving HALT state.         Correction:       Set to B'000000 when leaving HALT state.
Added in Rev. A	38-33	Table 38.26 RSPI Timing	Concertion: Decret b Docorde when reduning in the rotate.Table 38.26 RSPI Timing : Incorrect description is corrected.Error:Min.Max.UnitFiguresData input setup timeSlave $t_{SU}$ $25 + 2 \times t_{cyc}$ -ns $38.28$ to $38.31$ Correction:ItemSymbolMin.Max.UnitFigures $38.31$ Correction:ItemSymbolMin.Max.UnitFigures $38.28$ to $38.31$ Data input setup timeSlave $t_{SU}$ $25 - 2 \times t_{cyc}$ -ns $38.28$ to $38.31$



Rev.	Page	Part		Co	ontents			
			Figure 38.30 RSPI Timing (		A = "0") :	Incorrect	descript	ion is corrected.
			O in a figure shows the ad	ded part.				
			Error:				tm	
			SSL00,					÷
			SSL10, SSL20,				_/\	A
						<b>+</b> t <sub>tai</sub>	-	
			RSPCK0 to RSPCK2 CPOL = 0	1″	$\downarrow$	¥		
			Input					
			RSPCK0 to RSPCK2			1		
			Input					
					100		4821	
					TA X LS	воит 🗶	MSB IN	→ Мізв оџт
			l territe terr	. "		t <sub>ore</sub> , t <sub>or</sub>	. I	
		Figure 38.30	MOSID to MOSI2	1	~ ~	_		
Added	~~~~	RSPI Timing	Input MSBIN					MSB IN
in Dev A	38-35	(Slave,	1	1				
Rev. A		CPHA = "0")	Correction:					
			SSL00,				<sup>t</sup>	i
			SSL10, SSL20.				_X	X
			Input turne t		I	- LAD		+++-
			RSPCK0 to RSPCK2			$\neg$		sin tssur
			input					
			RSPCK0 to RSPCK2	$\square$		£	<u>      -</u>	
			Input 1		``		$\langle \rangle$	$\sim$
				44	t <sub>op</sub>		4 tree	
			MISO0 to MISO2 Output	SBOUT X DAT	A LS	воит 🗶	MSB IN	MSB OUT
			ter la te	1 "		tore, for	1	
			MOSID to MOSI2	1	~ <u> </u>	_		
			Input MSBIN					MSB IN
			Table 38.29 DRI Timing (W	hen Special	Mode is	On) : Inco	orrect de	scription is
			corrected.					
			Error:					T
			Item	Symbol	Min.	Max.	Unit	Figures
			Item DIN2 to DIN4 sampling	Symbol tar	Min. 8	Max. -	Unit ns	38.33 to
			Item			Max. -		
			Item DIN2 to DIN4 sampling edge undefined time before DIN1 initialization level release <u>(when direct reset</u>			Max.		38.33 to
			Item DIN2 to DIN4 sampling edge undefined time before DIN1 initialization level release (when direct reset is selected)	tar	8	Max. -	ns	38.33 to
			Item DIN2 to DIN4 sampling edge undefined time before DIN1 initialization level release (when direct reset is selected) DIN2 to DIN4 sampling			Max. - -		38.33 to
Added		Table 38.29	Item DIN2 to DIN4 sampling edge undefined time before DIN1 initialization level release (when direct reset is selected)	tar	8	Max. - -	ns	38.33 to
in	38-38	DRI Timing	Item DIN2 to DIN4 sampling edge undefined time before DIN1 initialization level release (when direct reset is selected) DIN2 to DIN4 sampling edge undefined time before	tar	8	Max. - -	ns	38.33 to
	38-38	DRI Timing (When Special	Item DIN2 to DIN4 sampling edge undefined time before DIN1 initialization level release (when direct reset is selected) DIN2 to DIN4 sampling edge undefined time <u>before</u> DIN1 initialization level release	tar	8	Max. - -	ns	38.33 to
in	38-38	DRI Timing	Item DIN2 to DIN4 sampling edge undefined time before DIN1 initialization level release (when direct reset is selected) DIN2 to DIN4 sampling edge undefined time <u>before</u> DIN1 initialization level release Correction:	tar tbr	8	-	ns	38.33 to 38.36
in	38-38	DRI Timing (When Special	Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release (when direct reset         is selected)         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         Correction:	tar tbr Symbol	8 12 Min.	Max.	ns ns Unit	38.33 to 38.36
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in	38-38	DRI Timing (When Special	Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release (when direct reset)         is selected)         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         Correction:         Item         DIN2 to DIN4 sampling         edge undefined time before         DIN2 to DIN4 sampling         edge undefined time before         DIN2 to DIN4 sampling         edge undefined time before	tar tbr Symbol	8 12 Min.	-	ns ns Unit	38.33 to 38.36 Figures 38.33 to
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in	38-38	DRI Timing (When Special	Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release (when direct reset         is selected)         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         Correction:         Item         DIN2 to DIN4 sampling         edge undefined time before         DIN2 to DIN4 sampling         edge undefined time before         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling	tar tbr Symbol	8 12 Min.	-	ns ns Unit	38.33 to 38.36 Figures 38.33 to
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in	38-38	DRI Timing (When Special	Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release (when direct reset         is selected)         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         Correction:         Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time after         DIN1 initialization level         release         Table 38.35 AUDR Module	tar tbr Symbol tar tbr	8 12 Min. 8 12	- - Max. -	ns ns Unit ns ns	38.33 to 38.36 Figures 38.33 to 38.36
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in	38-38	DRI Timing (When Special	Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release (when direct reset         is selected)         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         Correction:         Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time after         DIN1 initialization level         release         Table 38.35 AUDR Module         corrected.         Error:	tar tbr Symbol tar tbr Timing (PVc	8 12 Min. 8 12 cc = 5.0 V	- Max. - () : Incorr	ns ns Unit ns ect desc	38.33 to 38.36 Figures 38.33 to 38.33 to 38.36 ription is
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in Rev. A Added in	38-38	DRI Timing (When Special Mode is On)	Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release (when direct reset         is selected)         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         Correction:         Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time after         DIN1 initialization level         release         Table 38.35 AUDR Module         corrected.         Error:         Item         AUDRD output delay	tar tbr Symbol tar Timing (PVc Symbol td(AUDRCLK	8 12 Min. 8 12 cc = 5.0 V	- Max. - /) : Incorr	ns ns Unit ns ect desc	38.33 to 38.36 Figures 38.33 to 38.35 38.36 ription is
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in Rev. A Added in		DRI Timing (When Special Mode is On) Table 38.35 AUDR Module Timing	Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release (when direct reset         is selected)         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         Correction:         Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time after         DIN1 initialization level         release         Table 38.35 AUDR Module         corrected.         Error:         Item         AUDRD output delay         time before         AUDRCLK	tar tbr Symbol tar Timing (PVc Symbol td(AUDRCLK AUDRD) Symbol	8 12 Min. 8 12 cc = 5.0 V	- Max. - /) : Incorr Max. 35	ns ns Unit ns ect desc Unit ns Unit	38.33 to         38.36         Figures         38.33 to         38.33 to         38.33 to         38.33 to         38.346         Figures         38.46         Figures
in Rev. A Added in		DRI Timing (When Special Mode is On) Table 38.35 AUDR Module Timing	Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release (when direct reset         is selected)         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         Correction:         Item         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time before         DIN1 initialization level         release         DIN2 to DIN4 sampling         edge undefined time after         DIN1 initialization level         release         Table 38.35 AUDR Module         corrected.         Error:         Item         AUDRD output delay         time before         AUDRD output delay         time before         Correction:	tar tbr Symbol tar Timing (PVc Symbol td(AUDRCLK AUDRD)	8 12 Min. 8 12 cc = 5.0 V	- Max. - ') : Incorr Max. 35	ns ns Unit ns ect descr Unit ns	38.33 to         38.36         Figures         38.33 to         38.33 to         38.33 to         38.33 to         38.34 to         ription is         Figures         38.46



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			Table 38.36 AUDR Module Timing (PVcc = 3.3 V) : Incorrect description is corrected. Error:
			Item Symbol Min. Max. Unit Figures
		Table 38.36	AUDRD output delay td(AUDRCLKH 40 ns 38.46
Added in	38-47 AUDR Module Timing	time <u>before</u> AUDRCLK AUDRD)	
Rev. A		(PVcc = 3.3 V)	Correction:
			Item Symbol Min. Max. Unit Figures
			AUDRD output delay     td(AUDRCLKH-     -     40     ns     38.46       time after     AUDRCLK     AUDRD)     -     40     ns     38.46
Added in Rev. B	12-8	12.3.2 Flash Access Status Register (FASTAT)	Description of the bit 7 (ROMAE bit) in the Flash Access Status Register (FASTAT) is corrected.         Error:       An access command is issued to an address other than ROM program/erase addresses H'FD80 0000 to H'FD9F FFFF when the user boot MAT is selected.         Correction:       An access command is issued to an address other than ROM program/erase addresses H'FD80 0000 to H'FD9F FFFF when the user boot MAT is selected.         Correction:       An access command is issued to an address other than ROM program/erase addresses H'FD80 0000 to H'FD80 7FFF when the user boot MAT is selected.
Added in Rev. B	12-23	Figure 12.8 Command State Transitions in ROM Read Mode and P/E Mode	Figure 12.8 Command State Transitions in ROM Read Mode and P/E Mode : Incorrect description is corrected. Error:
Added in Rev. B	12-36	12.9.4 Reset during Programming or Erasure	Description of Reset during Programming or Erasure is added. -Description: When a hardware reset by "L" level input to the RESET# pin, switching the power off, or a FCU reset by setting the FRESET bit in the FRESETR register, is executed during programming or erasure, the whole data in the programming or erasure area becomes undefined. When the data in an area have become undefined, erase the area before using it again.



Rev.	Page	Part	Contents
Added in Rev. B	24-9	24.3.3 RSPli Pin Control Register (SPiPCR)	Description of the bit 5 (MOIFE bit) in the RSPIi Pin Control Register (SPiPCR) is corrected.         Error:       - When the MOIFE bit is cleared to "0", RSPIi outputs <u>on the MOSIi</u> <u>pin the last data unit from the previous serial transfer</u> during the SSL negation period.         - 0: MOSIi output value equals final <u>data</u> from previous transfer         Correction:       - When the MOIFE bit is cleared to "0", RSPIi outputs <u>the final output</u> <u>level of the previous serial transfer to the MOSIi pin</u> during the SSL negation period (When the CPHA bit is "0", MOSIi output value is <u>undefined</u> ).         - 0: MOSIi output value equals final <u>output level</u> from previous transfer (When the CPHA bit is "0", MOSIi output value is undefined).
Added in Rev. B	24-24	24.3.13 RSPIi Command Registers 0 to 3 (SPiCMD0 to SPiCMD3)	Description of the bit 13 (SPNDEN bit) in the RSPIi Command Registers 0 to 3 (SPiCMD0 to SPiCMD3) is corrected. Error: - If the SPNDEN bit is "0", the RSPIi sets the next-access delay to 1 RSPCK. - 0: A next-access delay of 1 RSPCK Correction: - If the SPNDEN bit is "0", the RSPIi sets the next-access delay to 1 RSPCK <u>+ 2 Pck</u> . - 0: A next-access delay of 1 RSPCK <u>+ 2 Pck</u>
Added in Rev. B	24-28	Table 24.7 MOSIi Signal Value Determination during SSL Negation Period	Table 24.7 MOSIi Signal Value Determination during SSL Negation Period :         Incorrect description is corrected.       Error:         MOIFE       MOIFV       MOSIi Signal Value during SSL Negation Period         0       0, 1       Final data from previous transfer         1       0       Always "L"         1       1       Always "H"         Correction:         MOIFE       MOIFV         MOIFE       MOIFV         MOIFE       MOIFV         MOIFE       MOIFV         MOIFE       MOSIi Signal Value during SSL Negation Period         0       0, 1         Final output level of the previous transfer (When the CPHA bit is "0", MOSIi output value is undefined)         1       0         1       1         1       1         1       1
Added in Rev. B	24-34	Figure 24.11 RSPI Transfer Format (CPHA = "0")	Figure 24.11 RSPI Transfer Format (CPHA = "0") : Incorrect description is corrected. Error:



Rev.	Page	Part	Contents
			Figure 24.12 RSPI Transfer Format (CPHA = "1") : Incorrect description is corrected. Error:
			Start Serial transfer period End
			RSPCK 1 2 3 4 5 6 7 8
			RSPCK
			Sampling
		<b>F</b> : 04.40	
Added in	24-34	Figure 24.12 RSPI Transfer	
Rev. B	24-04	Format (CPHA = "1")	Correction:
			Start Serial transfer period End
			RSPCK 1 2 3 4 5 6 7 8
			(CPOL = "1")
			Sampling
			The values after reset of the CANi Clock Select Register (CiCLKR) (i = 0 to 4) are corrected. Error:
			After Besister Name Abbravistica Beset B4 Address Size Berg
			Register Name         Abbreviation         Reset         P4 Address         Size         Page           CAN0 Clock Select Register         COCLKR         H'00         H'FFFF 6847         8, 16, 32         26-16
			:         : <th:< th="">         :         :         :</th:<>
			:         : <th:< th=""> <th:< th=""> <th:< th=""> <th:< th=""></th:<></th:<></th:<></th:<>
			CAN3 Clock Select Register C3CLKR <u>H'00</u> H'FFFF 9847 8, 16, 32 26-16
Added in	26-5	Table 26.3 Register	:         : <th:< th="">         :         :         <th:< th=""></th:<></th:<>
Rev. B		Configuration	Correction:
			After Register Name Abbreviation Reset P4 Address Size Page
			CAN0 Clock Select Register         COCLKR         Undefined         H'FFFF         6847         8, 16, 32         26-16
			CAN1 Clock Select Register         C1CLKR         Undefined         H'FFF 7847         8, 16, 32         26-16           : <td:< td="">         :         <td:< td=""> <td:< td=""></td:<></td:<></td:<>
			CAN2 Clock Select Register         C2CLKR         Undefined         H'FFFF 8847         8, 16, 32         26-16           : <td:< td="">         :         :         <td:< td=""></td:<></td:<>
			CAN3 Clock Select Register C3CLKR Undefined H'FFFF 9847 8, 16, 32 26-16 : : : : :
			CAN4 Clock Select Register C4CLKR Undefined H'FFFF A847 8, 16, 32 26-16
		1	



Rev.	Page	Part					onter				
				ue after reset of corrected.	of the bit 4 in	the	CANi	Clock Se	lect Re	gister (C	CiCLKR) (i =
			EIIOI.	Dit. 7	<u> </u>			2	0	4	0
				Bit: 7	6 {	5	4	3	2	1	0 CCLKS
			After	Reset: 0	0 (	)	0	0	0	0	0
							-			<af< td=""><td>ter Reset: <u>H'0</u></td></af<>	ter Reset: <u>H'0</u>
			Bit	Abbreviation	After Reset	R	w	Descripti	on		
Added in	26-16	26.3.2 CANi Clock Select Register	4	_	<u>0</u>	?	0	Reserved	Bit e written	with "0	and read as
Rev. B		(CiCLKR)	Correct	tion <sup>.</sup>							
		(i = 0 to 4)		Bit: 7	6	-	4	3	2	1	0 CCLKS
			After	Reset: 0	0	) <u>U</u>	Indefin	ied 0	0	0	0
					After				<	<after re<="" td=""><td>eset: <u>Undefine</u></td></after>	eset: <u>Undefine</u>
			Bit	Abbreviation	After Reset	R	w	Descripti	on		
						?	0	Reserved			
			4	_	<u>Undefined</u>	•	0		e written	with "0'	' and read as
			Setting	/alue of the bi	7 to 0 (CiR	-PCF	R bit)	Should be undefined	e written I value.		
		26.3.11	Setting v Control I Error:	Register (CiRI	7 to 0 (CiR PCR) (i = 0 After	PCF to 4)	R bit) is co	Should be undefined in the CA prrected.	e written I value. Ni Rece		
Added		26.3.11 CANi Receive	Setting Control I Error:	Register (CiRI	7 to 0 (CiR PCR) (i = 0 After Reset	PCF to 4) R	R bit) is co W	Should be undefined in the CA prrected.	e written I value Ni Rece	eive FIF	O Pointer
Added	26-42	CANi Receive FIFO Pointer	Setting v Control I Error:	Register (CiRI	7 to 0 (CiR PCR) (i = 0 After	PCF to 4)	R bit) is co	Should be undefined in the CA prrected. Descripti The CPL	e written I value. Ni Rece on J-side p	eive FIF	
	26-42	CANi Receive	Setting Control I Error:	Register (CiRI Abbreviation CiRFPCR	7 to 0 (CiR PCR) (i = 0 After Reset Undefined	PCF to 4) R	R bit) is co W	Should be undefined in the CA prrected. Descripti The CPL	e written I value. Ni Rece on J-side p	eive FIF	O Pointer
in	26-42	CANi Receive FIFO Pointer Control Register (CiRFPCR)	Setting v Control I Error: <u>Bit</u> 7 to 0	Register (CiRI Abbreviation CiRFPCR tion: Abbreviation	7 to 0 (CiR PCR) (i = 0 After Reset	PCF to 4) R R	R bit) is co W	Should be undefined in the CA prrected. Descripti The CPU FIFO is in Descripti	e written I value. Ni Rece on J-side purcement	eive FIF	O Pointer r the receive iting "H'FF"
in	26-42	CANi Receive FIFO Pointer Control Register (CiRFPCR)	Setting v Control I Error: Bit 7 to 0 Correct	Register (CiRI Abbreviation CiRFPCR	7 to 0 (CiR PCR) (i = 0 After Reset Undefined	PCF to 4) R R	R bit) is co W W	Should be undefined in the CA prrected. Descripti The CPU FIFO is in Descripti The CPU	e written I value. Ni Rece on J-side purcement	ointer fo ed by wr	O Pointer
in	26-42	CANi Receive FIFO Pointer Control Register (CiRFPCR)	Setting v Control I Error: Bit 7 to 0 Correct Bit 7 to 0 Setting v	Register (CiRI Abbreviation CiRFPCR tion: Abbreviation	After Reset Undefined	FPCF to 4) R R ?	R bit) i is co W W W R bit)	Should be undefined in the CA prrected. Descripti The CPL FIFO is in Descripti The CPL FIFO is in The CPL FIFO is in	e written I value. Ni Rece on J-side pr ccrement	pinter fo ed by wr pointer fo ointer fo ed by wr	O Pointer r the receive iting "H'FF" r the receive iting "H'FF"
in	26-42	CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0 to 4)	Setting v Control I Error: <u>Bit</u> 7 to 0 <u>Bit</u> 7 to 0 Setting v Control I Error:	Register (CiRI Abbreviation CiRFPCR tion: Abbreviation CiRFPCR /alue of the bi Register (CiTF	After Reset Undefined After Reset Undefined	R R R PCF R PCF to 4)	R bit) is co W W W W	Should be undefined in the CA orrected. Descripti The CPL FIFO is in Descripti The CPL FIFO is in in the CA orrected.	e written I value. Ni Reco D-side p Corement J-side p Crement Ni Trans	pinter fo ed by wr pointer fo ointer fo ed by wr	O Pointer r the receive iting "H'FF" r the receive iting "H'FF"
in	26-42	CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0 to 4) 26.3.13 CANi Transmit FIFO Pointer	Setting v Control I Error: <u>Bit</u> 7 to 0 Correct <u>Bit</u> 7 to 0 Setting v Control I	Abbreviation         CiRFPCR         tion:         Abbreviation         CiRFPCR         value of the bit	7 to 0 (CiR PCR) (i = 0 After Reset Undefined After Reset Undefined	FPCF to 4) R R ?	R bit) i is co W W W R bit)	Should be undefined in the CA prrected. Descripti The CPU FIFO is in The CPU FIFO is in in the CA prrected. Descripti The CPU FIFO contents	e written I value. Ni Reco on J-side pr crement Ni Trans on J-side po	pointer for oointer for oointer for ed by wr smit FIF	O Pointer r the receive iting "H'FF" r the receive iting "H'FF"
in Rev. B Added		CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0 to 4) 26.3.13 CANi Transmit FIFO Pointer Control Register	Setting v Control Error: Bit 7 to 0 Correct Bit 7 to 0 Setting v Control Error: Bit 7 to 0	Register (CiRI Abbreviation CiRFPCR tion: Abbreviation CiRFPCR /alue of the bit Register (CiTF Abbreviation CiTFPCR	After Reset Undefined After Reset Undefined	R R R PCF to 4)	R bit) is co W W W W R bit) is co	Should be undefined in the CA prrected. Descripti The CPU FIFO is in The CPU FIFO is in in the CA prrected. Descripti The CPU FIFO contents	e written I value. Ni Reco on J-side pr crement Ni Trans on J-side po	pointer for oointer for oointer for ed by wr smit FIF	O Pointer r the receive iting "H'FF" r the receive iting "H'FF" O Pointer r the transmi
in Rev. B Added in		CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0 to 4) 26.3.13 CANi Transmit FIFO Pointer	Setting v Control I Error: Bit 7 to 0 Correct Bit 7 to 0 Setting v Control I Error: Bit	Register (CiRI Abbreviation CiRFPCR tion: Abbreviation CiRFPCR /alue of the bit Register (CiTF Abbreviation CiTFPCR	7 to 0 (CiR PCR) (i = 0 After Reset Undefined After Reset Undefined 7 to 0 (CiTI PCR) (i = 0 After Reset Undefined	R R R PCF to 4)	R bit) is co W W W W R bit) is co	Should be undefined in the CA prrected. Descripti The CPU FIFO is in The CPU FIFO is in in the CA prrected. Descripti The CPU FIFO contents	e written I value. Ni Reco on J-side pr crement Ni Trans on J-side po	pointer for oointer for oointer for ed by wr smit FIF	O Pointer r the receive iting "H'FF" r the receive iting "H'FF" O Pointer r the transmi
in Rev. B Added in		CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0 to 4) 26.3.13 CANi Transmit FIFO Pointer Control Register (CiTFPCR)	Setting v Control Error: Bit 7 to 0 Correct Bit 7 to 0 Setting v Control Error: Bit 7 to 0	Register (CiRI Abbreviation CiRFPCR tion: Abbreviation CiRFPCR /alue of the bit Register (CiTF Abbreviation CiTFPCR	After Reset Undefined After Reset Undefined	R R R PCF to 4)	R bit) is co W W W W R bit) is co	Should be undefined in the CA prrected. Descripti The CPU FIFO is in The CPU FIFO is in in the CA prrected. Descripti The CPU FIFO contents	on J-side proceedings Ni Trans	pointer for oointer for oointer for ed by wr smit FIF	O Pointer r the receive iting "H'FF" r the receive iting "H'FF" O Pointer r the transmi



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Added		Part 26.3.20 CANi Error Interrupt Factor		tion of the b (i = 0 to 4 Abbreviation BLIF	) is cor After	rrec R	v w	t) in the CANi Error Interrupt Factor Judge Register
in Rev. B	26-57	Judge Register (CiEIFR) (i = 0 to 4)	Correc Bit	tion: Abbreviation	After Reset	R	w	Description
			7	BLIF	0	R	W	<ul> <li>Bus Lock Detect Flag*<sup>1</sup></li> <li>The BLIF bit is set to "1" if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.</li> <li>After the bit is set to "1", <u>bus lock can be detected again after either of the following conditions is satisfied:</u></li> <li>After this bit is set to "0" from "1", recessive bits are detected (<u>bus lock is resolved</u>).</li> <li>After this bit is set to "0" from "1", the CAN module enters CAN reset mode and then enters CAN operation mode again (<u>internal reset</u>).</li> <li>0: No bus lock detected</li> <li>1: Bus lock detected</li> </ul>



#### Date: October 1, 2013





	Page	Part			Contents	
			description is		t Mode and CAN Halt	Mode : Incorrect
			Error:	Beecher	<b>T</b>	D
			Mode CAN reset mode	Receiver CAN module enters CAN		Bus-Off CAN module enters CAN reset mode
			(forcible transition) CANM = "11"		reset mode without waiting for	without waiting for the end of bus-off recovery.
			CAN reset mode CANM = "01"	CAN module enters CAN reset mode without waiting for the end of message reception.	reset mode after waiting for	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
			CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception* <sup>2</sup> * <sup>3</sup> .	mode after waiting for the end of message transmission* <sup>1</sup> * <sup>4</sup> .	[When the BOM bit is "00"] A halt request from a program will be acknowledged only after bus-off recovery. [When the BOM bit is "01"] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "10"] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "11"] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.
Added	26-74	Table 26.9 Operation in CAN Reset	transitio *2 If the C/ the CiE *3 If a CAN halt mo *4 If a CAN	n occurs when the bus is idle, tl AN bus is locked <u>at the</u> dominar IFR register. I bus error occurs during recept de.	he next transmission ends, or th tt <u>level</u> , the program can detect ion after CAN halt mode is requ curs during transmission after C	ring suspend transmission, mode e CAN module becomes a receiver. this state by monitoring the BLIF bit in ested, the CAN <u>mode transits to</u> CAN AN reset mode or CAN halt mode is
Rev. B		Mode and CAN	Mode	Receiver	Transmitter	Bus-Off
		Halt Mode	CAN reset mode (forcible transition) CANM = "11"	CAN module enters CAN reset mode without waiting for the end of message reception.	t CAN module enters CAN rese mode without waiting for the e of message transmission.	t CAN module enters CAN reset nd mode without waiting for the end of bus-off recovery.
			CAN reset mode CANM = "01"		t CAN module enters CAN rese mode after waiting for the end message transmission.* <sup>1</sup> * <sup>4</sup> .	t CAN module enters CAN reset of mode without waiting for the end of bus-off recovery.
			CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception. $*^{2*^3}$ .	CAN module enters CAN halt mode after waiting for the end message transmission.* <sup>1</sup> * <sup>2</sup> * <sup>4</sup> .	A hait request from a program
						will be acknowledged only after bus-off recovery. [When the BOM bit is "01"]
						bus-off recovery. [When the BOM bit is "01"] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "10"] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from
						bus-off recovery. [When the BOM bit is "01"] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "10"] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery
			Notes: *1 If severa transmis transitio *2 If the C/ CiEIFR	ssion. In a case that the CAN re n occurs when the bus is idle, th AN bus is locked <u>in</u> dominant <u>sta</u> register. <u>The CAN module does</u>	e transmitted, mode transition o set mode is being requested du ne next transmission ends, or th ate, the program can detect this	bus-off recovery. [When the BOM bit is "01"] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "10"] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "11"] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during
			Notes: *1 If sever transmit transitio *2 If the C/ CiEIFR state. E *3 If a CAN halt mov dominar	al messages are requested to bi ssion. In a case that the CAN re n occurs when the bus is idle, th AN bus is locked <u>in</u> dominant <u>str</u> register. <u>The CAN module does</u> ther <u>CAN reset mode instead</u> . I bus error occurs during recept de. <u>However, the CAN module on</u> <u>tt state</u> .	e transmitted, mode transition o set mode is being requested du ne next transmission ends, or th ate, the program can detect this not enter CAN halt mode while ion after CAN halt mode is requ loes not enter CAN halt mode w	bus-off recovery. [When the BOM bit is "01"] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "10"] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "11"] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off. ccurs after the completion of the first ring suspend transmission, mode e CAN module becomes a receiver. state by monitoring the BLIF bit in the the CAN bus is locked in dominant ested, the CAN module enters CAN



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Added in Rev. B	28-11	28.3 Register Descriptions	<ul> <li>28.3 Register Descriptions : Incorrect description is corrected.</li> <li>Error: These flags are used to enable DMA transfer requests. Set these flags to "1" to enable a DMA transfer request, and set them to "0" to disable a request. To prevent incorrect DMA operation, only rewrite these bits from the DMA transfer masked state to the DMA transfer enabled state when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"). Do not rewrite from the DMA transfer enabled state to the DMA transfer masked state when DRI acquisition is enabled (DRI acquisition is enabled, since that can result in a DMA request not being handled.</li> <li>Correction: These flags are used to enable DMA transfer requests. Set these flags to "1" to enable a DMA transfer request, and set them to "0" to disable a DMA transfer request. To prevent incorrect DMA operation, only rewrite these bits from the DMA transfer request.</li> <li>Correction: These flags are used to enable DMA transfer requests. Set these flags to "1" to enable a DMA transfer request. To prevent incorrect DMA operation, only rewrite these bits from the DMA transfer request masked state to the DMA transfer request enabled state when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"). Do not rewrite from the DMA transfer request enabled state to the DMA transfer request masked state when DRI acquisition is enabled, since that can result in a DMA transfer request enabled state to the DMA transfer request masked state when DRI acquisition is enabled.</li> </ul>
Added in Rev. B	28-16	28.3.4 DRI0DIN DMA Transfer Enable Register (DRI0DINDEN)	28.3.4 DRIODIN DMA Transfer Enable Register (DRIODINDEN) : Incorrect         description is corrected.         Error:       Also note that it is only possible to rewrite the DRIODINDEN register bits from the transfer masked state to the transfer enabled state when DRI acquisition is enabled (DRIDCAPCNT.DCPEN bit = "1"). Do not rewrite from the transfer enabled state to the transfer masked state when DRI acquisition is enabled.         Correction:       Also note that it is only possible to rewrite the DRIODINDEN register bits from the transfer enabled state to the transfer masked state when DRI acquisition is enabled.         Correction:       Also note that it is only possible to rewrite the DRIODINDEN register bits from the DMA transfer request masked state to the DMA transfer request enabled state when DRI acquisition is enabled (DRIDCAPCNT.DCPEN bit = "1"). Do not rewrite from the DMA transfer request enabled state to the DMA transfer request enabled state to the DMA transfer request enabled state to the DMA transfer request masked state when DRI acquisition is enabled.
Added in Rev. B	28-21	28.3.8 DRI0DEC DMA Transfer Enable Register (DRI0DECDEN)	<ul> <li>28.3.8 DRIODEC DMA Transfer Enable Register (DRIODECDEN) : Incorrect description is corrected.</li> <li>Error: If a DMA transfer request mask (disable) setting and an internal DMA transfer request occur at the same time, the DMA transfer request mask (disable) setting takes precedence. Also note that it is only possible to rewrite the DRIODECDEN register bits from the transfer masked state to the transfer enabled state when DEC counter operation is enabled (DRIiDECnCNT.DECnEN bit = "1"). Do not rewrite from the transfer enabled state to the transfer masked state when DEC counter operation is enabled.</li> <li>Correction: If a DMA transfer request mask (disable) setting takes precedence. Also note that it is only possible to rewrite the DRIODECDEN register bits from the transfer request mask (disable) setting and an internal DMA transfer request mask (disable) setting and an internal DMA transfer request mask (disable) setting takes precedence. Also note that it is only possible to rewrite the DRIODECDEN register bits from the DMA transfer request mask (disable) setting takes precedence. Also note that it is only possible to rewrite the DRIODECDEN register bits from the DMA transfer request masked state to the DMA transfer request enabled state when DEC counter operation is enabled (DRIIDECnCNT.DECnEN bit = "1"). Do not rewrite from the DMA transfer request enabled state to the DMA transfer request masked state to the DMA transfer request enabled state when DEC counter operation is enabled</li> </ul>



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1.001.		i dit	28.3.12 DRI0 DMA Transfer Enable Register (DRI0TRMDEN) : Incorrect
			description is corrected.
Added in Rev. B	28-27	28.3.12 DRI0 DMA Transfer Enable Register (DRI0TRMDEN)	<ul> <li>Error: Controls the enabled/disabled states for DRI0 transfer related DMA transfer requests. If one of these bits is set to "1", the corresponding DMA transfer request signal output is enabled. If a DMA transfer mask (disable) is set at the same time as an internal DMA transfer request, the DMA transfer mask (disable) takes precedence. Also note that when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"), the DRI0TRMDEN register may only be rewritten from the transfer masked state to the transfer enabled state. Do not rewrite any bits in this register from the transfer enabled state to the transfer masked state when DRI acquisition is enabled.</li> <li>Correction: Controls the enabled/disabled states for DRI0 transfer related DMA transfer requests. If one of these bits is set to "1", the corresponding DMA transfer request signal output is enabled. If a DMA transfer mask (disable) is set at the same time as an internal DMA transfer mask (disable) is set at the same time as an internal DMA transfer mask (disable) is set at the same time as an internal DMA transfer request, the DMA transfer mask (disable) takes precedence. Also note that when DRI acquisition is enabled (DRIiDCAPCNT.DCPEN bit = "1"), the DRI0TRMDEN register may only be rewritten from the DMA transfer request masked state to the DMA transfer request enabled state. Do not rewrite any bits in this register from the DMA transfer request masked state to the DMA transfer request enabled state. Do not rewrite any bits in this register from the DMA transfer request enabled state to the DMA transfer request masked state to the DMA transfer request enabled state. Do not rewrite any bits in this register from the DMA transfer request enabled state to the DMA transfer request masked state to the DMA transfer request enabled state. Do not rewrite any bits in this register from the DMA transfer request enabled state to the DMA transfer request masked state to the DMA transfer request masked state to the DMA transfer request masked state to the DM</li></ul>
			Description of the bit 2 (FBSEN bit) in the FlexRay Operation Control Register
امعامام		32.4.1	(FXROC) is corrected.
Added in	32-13	FlexRay Operation	Error: - FRNVMn
Rev. B	02 10	Control Register	- FRNVMn
		(FXROC)	Correction: - <u>FRNMVn</u> - FRNMVn
Added in Rev. B	32-139	32.12.5 Configuration of NIT Start and Offset Correction Start	<ul> <li>32.12.5 Configuration of NIT Start and Offset Correction Start : Incorrect description is corrected.</li> <li>Error: For the FlexRay module the offset correction start is required to be the OCS bit in the FRGTUC4 register <u>o</u> the NIT bit <u>int</u> the FRGTUC4 register + 1 = k+1.</li> <li>Correction: For the FlexRay module the offset correction start is required to be the OCS bit in the FRGTUC4 register ≥ the NIT bit <u>in</u> the FRGTUC4 register + 1 = k+1.</li> </ul>
			Table 32.8 State Transitions of FlexRay overall state Machine : Incorrect description is corrected.
			Error: T# Condition From To
			T1 Hard reset All states DEFALT CONFIG
			T2 Command CONFIG, bits CMD3 to <u>DEFALT CONFIG</u> CONFIG CMD0 in the FRSUCC1 register = B'0001
Added	32-145	Table 32.8 State Transitions	T15 Command CONFIG, bits CMD3 to HALT DEFALT_CONFIG CMD0 in the FRSUCC1 register = B'0001
in Rev. B	32-145	of FlexRay overall state	
1.0V. D		Machine	Correction:
			T# Condition From To
			T1     Hard reset     All states     DEFAULT CONFIG       T2     Command CONFIG, bits CMD3 to CMD0 in the FRSUCC1 register = B'0001     DEFAULT CONFIG     CONFIG
			T15 Command CONFIG, bits CMD3 to HALT <u>DEFAULT CONFIG</u> CMD0 in the FRSUCC1 register = B'0001

