Date: 6/28/2011

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A781C/E	Rev.	3.00
Title	SH7450 Group, SH7451 Group Hardware Manual Errata Rev.C		Information Category	Technical Notification		
Applicable Product	SH7450 Group, SH7451 Group	Lot No.	Reference Document	SH7450 Group, SH7451 Group Hardware Manual Rev.1.00		

Since we changed the following contents of "TN-SH7-A781 B/E:SH7450 Group and SH7451 Group hardware manual Errata Rev.B (Technical update published on February 17, 2011)", we announce you.

Please use attached errata in the case of use of SH7450 Group and SH7451 Group hardware manual Rev.1.00.

In addition, the contents of errata (Rev.B) of this manual are also indicated to attach errata (Rev.C).

- Technical update TN-SH7-A781B/E: Errata (Rev.B)

Appending Document:"SH7450 Group and SH7451 Group hardware manual Rev.1.00" errata Rev.C – 22 sheets

* In the following, the portion of net credit (■) or an underline is a portion with an addition/change.

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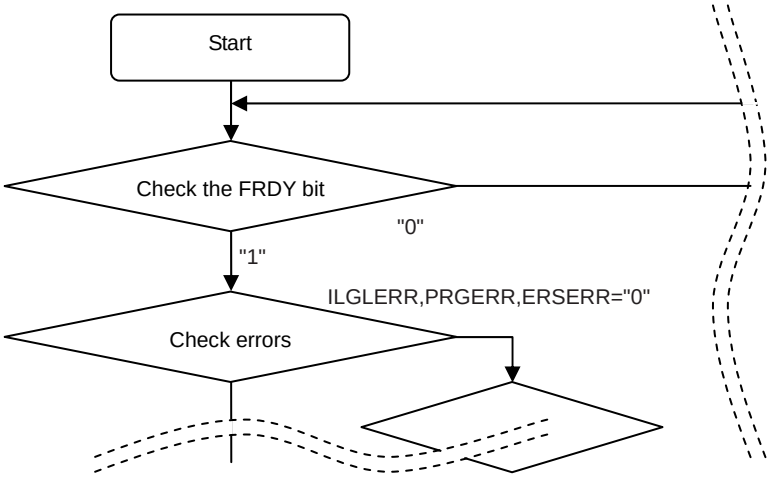
<tr><td rowspan="2">Adds by Rev.A</td><td rowspan="2">11-1</td><td rowspan="2">Section 11 Address Space</td><td>Error</td><td>Figures 11.1 to 11.6 show this MCU address space. This MCU has a 32-bit (4-Gbyte) physical address space. Internal ROM, internal RAM (SHwyRAM), external address spaces are mapped onto the highest 512 Mbytes (H'0000 0000 to H'1FFF FFFF). IL memory, OL memory, and other internal resources are mapped onto the lowest 512 Mbytes (H'E000 0000 to H'FFFF FFFF).</td></tr>
<tr><td>Correction</td><td>Figures 11.1 to 11.6 show this MCU address space. This MCU has a 32-bit (4-Gbyte) physical address space. Internal ROM, internal RAM (SHwyRAM), external address spaces are mapped onto the <u>lowest</u> 512 Mbytes (H'0000 0000 to H'1FFF FFFF). IL memory, OL memory, and other internal resources are mapped onto the <u>highest</u> 512 Mbytes (H'E000 0000 to H'FFFF FFFF).</td></tr>
<tr><td rowspan="2">Adds by Rev.A</td><td rowspan="2">12-25</td><td rowspan="2">Figure 12.10 Procedure for Transition to ROM Read Mode</td><td>Error</td><td> 
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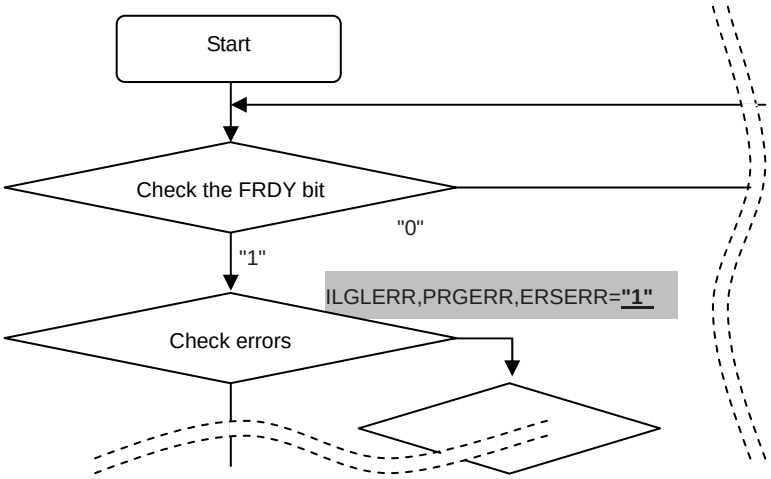
<tr><td>Correction</td><td> 
</td></tr>
<tr><td>Adds by Rev.A</td><td>25-33</td><td>25.8.10 Notes on Master Reception Mode of I²C Bus Interface Mode</td><td>Add</td><td>25.8.10 Notes on Master Reception Mode of I²C Bus Interface Mode
The SCL signal extra outputs a clock after the ninth clock, if issue of stop condition or re-issue of start condition is overlapped with the falling of the ninth clock.
After the completion of a master reception, confirm the falling of the ninth clock on SCL signal, and then issue a stop condition or re-issue a start condition.
The falling of the ninth clock is confirmed as follow.
・Confirm that the RDRF flag (receive data full flag) in the ICSR register is set to “1”, and then the SCLO flag (SCL output level flag) in the ICCR2 register is set to “0” (pins SCL outputs “L” level).</td></tr>
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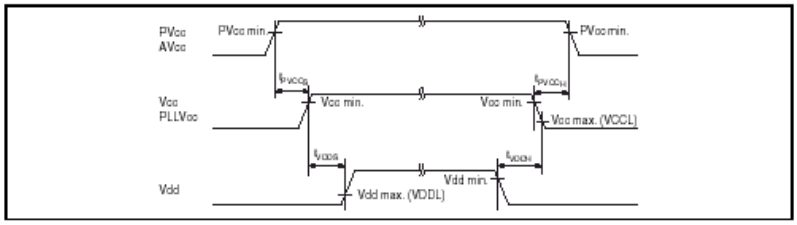
Table 38.3 DC Characteristics - Input Level Voltage: When 5 V is Used
<table>
<tr><th colspan="3">Item</th><th>Symbol</th><th colspan="3">Rating</th><th>Unit</th></tr>
<tr><th></th><th></th><th></th><th></th><th>Min.</th><th>Typ.</th><th>Max.</th><th></th></tr>
<tr><td>Low level input voltage</td><td>Pins without threshold value switching function</td><td>EXTAL</td><td>VIL</td><td>0</td><td></td><td>0.25 Vcc</td><td>V</td></tr>
</table>
</td></tr>
<tr><td>Correction</td><td>
Table 38.3 DC Characteristics - Input Level Voltage: When 5 V is Used
<table>
<tr><th colspan="3">Item</th><th>Symbol</th><th colspan="3">Rating</th><th>Unit</th></tr>
<tr><th></th><th></th><th></th><th></th><th>Min.</th><th>Typ.</th><th>Max.</th><th></th></tr>
<tr><td>Low level input voltage</td><td>Pins without threshold value switching function</td><td>EXTAL</td><td>VIL</td><td>0</td><td></td><td>0.125 Vcc</td><td>V</td></tr>
</table>
</td></tr>
<tr><td rowspan="2">Adds by Rev.A</td><td rowspan="2">38-14</td><td rowspan="2">38.3.1 Power-On/Off Timing</td><td>Error</td><td>
Table 38.16 Power-On/Off Timing
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>PVcc voltage at power off</td><td>VCCL</td><td>0</td><td>1.0</td><td>V</td><td>38.4</td></tr>
</table>


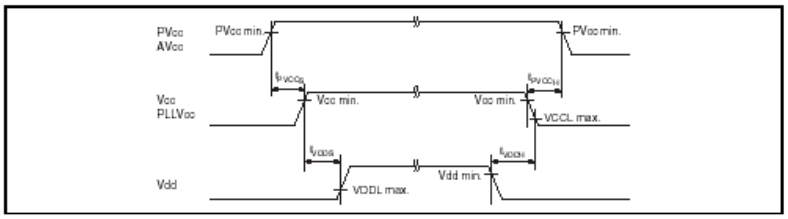
Figure 38.4 Power-On/Off Timing
</td></tr>
<tr><td>Correction</td><td>
Table 38.16 Power-On/Off Timing
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>Vcc voltage at power off</td><td>VCCL</td><td>0</td><td>1.0</td><td>V</td><td>38.4</td></tr>
</table>


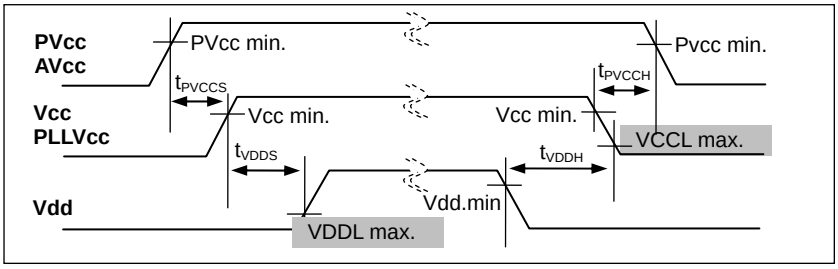
Figure 38.4 Power-On/Off Timing
</td></tr>
<tr><td>Adds by Rev.B</td><td>38-14</td><td>38.3.1 Power-On/Off Timing</td><td>Replacement (Specify sign and figure)</td><td>


Figure 38.4 Power-On/Off Timing
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</table>

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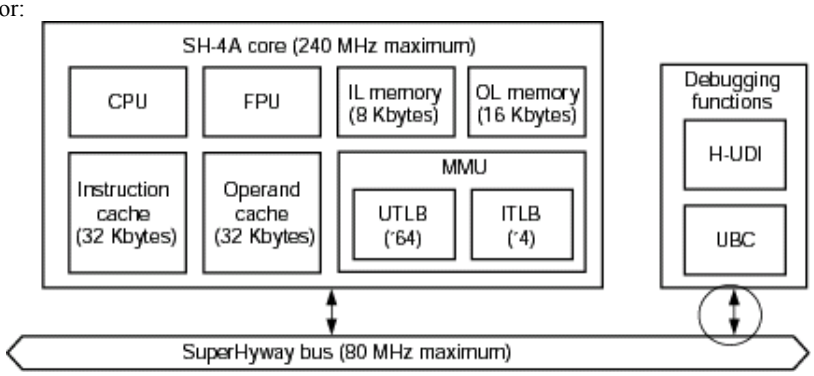
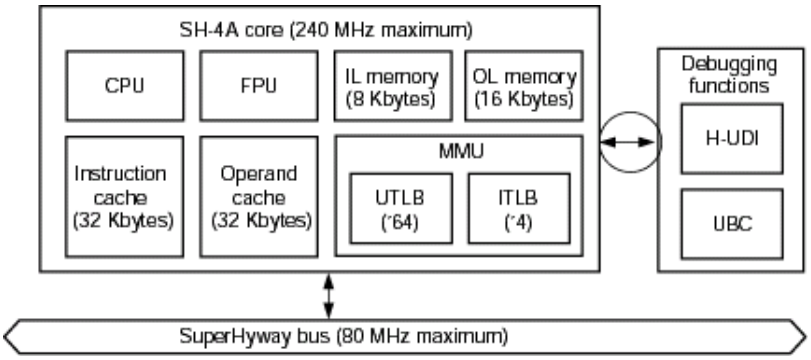
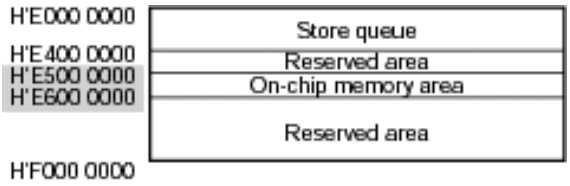
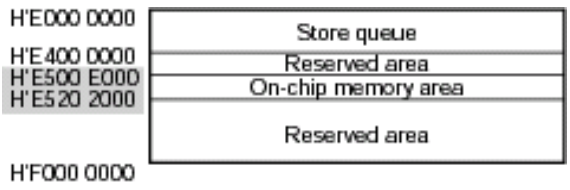
Error: Maximum transfer rate: 3.3 MHz</td></tr>
<tr><td>Correct: Maximum transfer rate: 3.3 Mbps</td></tr>
<tr><td>Table 1.1 Specifications Overview: Description of RSPI changed.
Error: Maximum transfer rate: 10 MHz</td></tr>
<tr><td>Correct: Maximum transfer rate: 10 Mbps</td></tr>
<tr><td rowspan="2">Adds by Rev.C</td><td rowspan="2">1-6</td><td rowspan="2">Table 1.1 Specifications Overview</td><td>Table 1.1 Specifications Overview: Description of DRO changed.
Error: Maximum transfer speed: 10 MHz</td></tr>
<tr><td>Correct: Maximum transfer speed: 20 Mbps(when 16bits is selected)</td></tr>
<tr><td rowspan="2">Adds by Rev.C</td><td rowspan="2">1-8</td><td rowspan="2">Figure 1.1 Block Diagram</td><td>Figure 1.1 Block Diagram: Incorrect description corrected.
O in a figure shows the corrected part.
Error:
 
</td></tr>
<tr><td>Correct:
 
</td></tr>
<tr><td rowspan="2">Adds by Rev.C</td><td rowspan="2">7-6</td><td rowspan="2">Figure 7.4 P4 Area</td><td>Figure 7.4 P4 Area: Incorrect description corrected.
Error:
 
</td></tr>
<tr><td>Correct:
 
</td></tr>
<tr><td>Adds by Rev.C</td><td>7-6</td><td>7.1.1 (1) (d) P4 Area</td><td>Incorrect description corrected (the 4th line).
Error: The area from H'E500 0000 to H'E5FF FFFF comprises addresses for accessing the on-chip memory.
Correct: The area from H'E500 E000 to H'E520 1FFF comprises addresses for accessing the on-chip memory.</td></tr>
</table>

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Adds by Rev.C	7-6	7.1.1 (1) (d) P4 Area	Incorrect description corrected (the 12th line). Error: The area from H'F300 0000 to H'F37F FFFF is used for direct access to instruction TLB data array. Correct: The area from H'F300 0000 to H'F3FF FFFF is used for Direct access to instruction TLB data array. Incorrect description corrected (the 18th line). Error: The area from H'F600 0000 to H'F60F FFFF is used for direct access to the unified TLB address array. Correct: The area from H'F600 0000 to H'F6FF FFFF is used for direct access to the unified TLB address array. Incorrect description corrected (the 20th line). Error: The area from H'F700 0000 to H'F70F FFFF is used for direct access to unified TLB data array. Correct: The area from H'F700 0000 to H'F7FF FFFF is used for direct access to unified TLB data array.
Adds by Rev.C	7-40	7.6.6 (2) UTLB Data Array 2	Incorrect description corrected (the 2nd line). Error: The UTLB data array is allocated to addresses H'F780 0000 to H'F78F FFFF in the P4 area. Correct: The UTLB data array is allocated to addresses H'F780 0000 to H'F7FF FFFF in the P4 area.
Adds by Rev.C	9-1	9.1 IL Memory/ OL Memory	Incorrect description corrected (the 3rd line). Error: The SH-4A includes three types of memory modules for storage of instructions and data: OL memory, IL memory, and U memory. Correct: The SH-4A includes two types of memory modules for storage of instructions and data: OL memory and IL memory.
Adds by Rev.C	9-9	9.3.4 OL Memory Block Transfer	Incorrect description corrected (the 10th line). Error: In either case, transfer rate is fixed to 32 bytes. Correct: In either case, transfer size is fixed to 32 bytes. Incorrect description corrected (the 11th line). Error: In either case, other pages and cache can be accessed during block transfer, but the CPU will stall if the page which is being transferred is accessed before data transfer ends. Correct: In either case, other pages and cache can be accessed during block transfer, if the page is accessed during data transfer, the CPU will stall until block transfer ends.
Adds by Rev.C	10-1	10.1.1 (2) The MD0 pin	Incorrect description corrected (the 3rd line). Error: In single chip mode, only the internal ROM is used. Correct: In single chip mode, only the internal ROM and RAM is used.
Adds by Rev.C	12-8	12.3.2 Flash Access Status Register	Description of the bit 7 (ROMAE bit) in the Flash Access Status Register (FASTAT) corrected (the 25th line). Error: A block erase, block program, or lock bit program command is issued to ROM when the user boot MAT is selected. Correct: A block erase, program, or lock bit program command is issued to ROM when the user boot MAT is selected.
Adds by Rev.C	12-9	12.3.3 ROM MAT Select Register	Setting value of the bit 15 to 8 (KEY bit) in the ROM MAT Select Register (ROMMAT) corrected. Error: R: R W: *1 Note: *1 Write data is not retained. Correct: R: 0 W: W
Adds by Rev.C	12-13	12.3.6 Flash P/E Mode Entry Register	Setting value of the bit 15 to 8 (FEKEY bit) in the Flash P/E Mode Entry Register (FENTRYR) corrected. Error: R: R W: *1 Note: *1 Write data is not retained. Correct: R: 0 W: W
Adds by Rev.C	12-15	12.3.7 Flash Protect Register	Setting value of the bit 15 to 8 (FPKEY bit) in the Flash Protect Register (FPROTR) corrected. Error: R: R W: *1 Note: *1 Write data is not retained. Correct: R: 0 W: W

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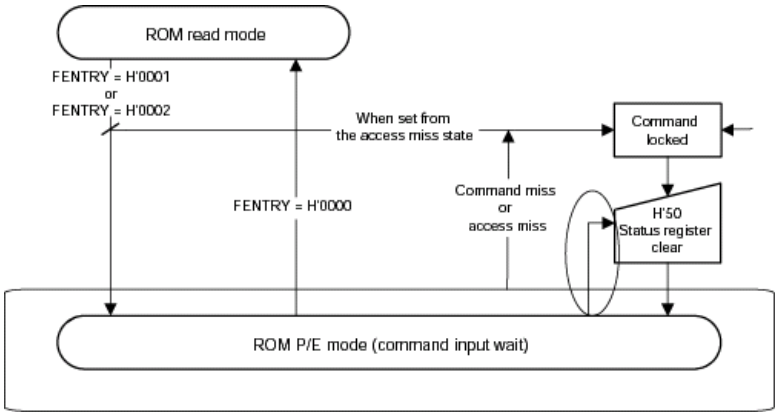
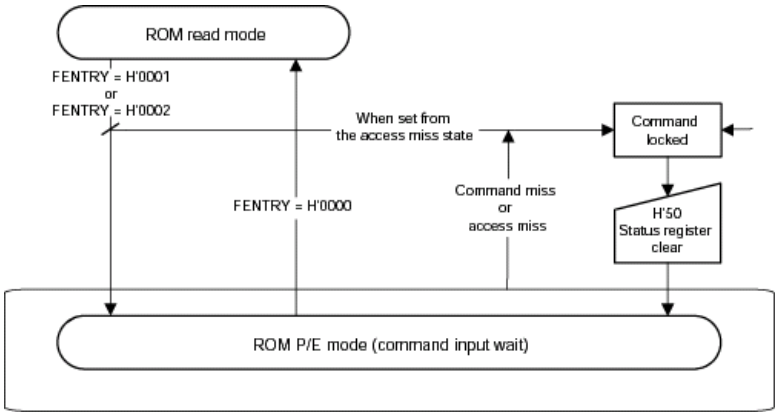
Adds by Rev.C	12-16	12.3.8 Flash Reset Register	Setting value of the bit 15 to 8 (FRKEY bit) in the Flash Reset Register (FRESETR) corrected. Error: R: R W: *1 Note: *1 Write data is not retained. Correct: R: 0 W: W
Adds by Rev.C	12-18	Table 12.3 Comparison of Programming Modes	Table 12.3 Comparison of Programming Modes: Notes deleted. Deleted: Notes: *1 A specified block can be erased after the key code is authenticated. *2 After the MCU is started in the embedded program stored MAT and the boot program provided by Renesas Technology Corp. is executed, execution starts from the location indicated by the reset vector of the user boot MAT.
Adds by Rev.C	12-20	Table 12.5 FCU Command Format	Table 12. 5 FCU Command Format: Incorrect description corrected. Error: Number of Bus Cycle Correct: Number of Command Cycle*1 Notes: *1 The number of command cycles is the number of peripheral bus write accesses to program/erase address.
Adds by Rev.C	12-23	Figure 12.8 Command State Transitions in ROM Read Mode and P/E Mode	Figure 12.8 Command State Transitions in ROM Read Mode and P/E Mode: Incorrect description corrected. O in a figure shows the deleted part. Error:  Correct: 
Adds by Rev.C	12-24	12.6.3 FCU Command Usage	Incorrect description corrected (the 11th line). Error: If the FRDY bit is held in the "0" state for a period longer than the program/erase time or the suspend delay time(see section 38, Electrical Characteristics), Correct: If the FRDY bit is held in the "0" state for a period longer than the program/erase time (see section 38, Electrical Characteristics),
Adds by Rev.C	15-3	15.1.1 Interrupt Request Sources in INTC	Incorrect description corrected (the 2nd line). Error: The INTC manages non-maskable interrupt (NMI interrupt) and general interrupt (IRQ interrupt) and on-chip peripheral module interrupt requests in exceptional handling. Correct: The INTC manages non-maskable interrupt (NMI interrupt) and general interrupt (IRQ interrupt and on-chip peripheral module interrupt requests in exceptional handling).

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Adds by Rev.C	15-62	15.7.2 To Clear IRQ Interrupt Requests When Level Detection is Selected	Incorrect description corrected (the 2nd line). Error: To clear IRQ interrupt requests that are set up for level detection, write "1" to the INTMSK.IRQn (n = 0 to 7) bit register IM07 to IM00 bits that correspond to the requests to be cleared. Correct: To clear IRQ interrupt requests that are set up for level detection, write "1" to the INTMSK.IRQn (n = 0 to 7) bit that correspond to the requests to be cleared.
Adds by Rev.C	15-63	15.7.3 To Clear IRQ Interrupt Requests When Edge Detection is Selected	Incorrect description corrected (the 2nd line). Error: To clear IRQ interrupt requests that are set up for edge detection, write "0" to the INTREQ.IRQn (n = 0 to 7) bit that correspond to the requests to be cleared. Correct: To clear IRQ interrupt requests that are set up for edge detection, write "0" to the INTREQ.IRQn (n = 0 to 7) bit that correspond to the requests to be cleared after reading"1".
Adds by Rev.C	17-4	17.3.2 Watchdog Timer Control/Status Register	Incorrect description corrected (the 3rd line). Error: Although the WDTCSR register is initialized by a hardware reset, the count value is retained when a reset due to a counter overflow occurs in watchdog timer mode. The value will be H'0000 0000 after a hardware reset. Correct: The WDTCSR register is reset by the RESET# pin and initialized to "H'0000 0000". Although the value set prior to the reset will be retained for resets due to counter overflows in watchdog timer mode, the WOVF bit is set to "1". The value set prior to the reset will be retained for resets due to H-UDI.
			Setting value of the bit 4 (WOVF bit) in the Watchdog Timer Control/Status Register (WDTCSR) corrected. Error: W: W Correct: W: *1 Note: *1 Only writing "0" is valid. If "1" is written, the previous value will be retained.
			Setting value of the bit 3 (IOVF bit) in the Watchdog Timer Control/Status Register (WDTCSR) corrected. Error: W: W Correct: W: *1 Note: *1 Only writing "0" is valid. If "1" is written, the previous value will be retained.
Adds by Rev.C	17-5	17.3.3 Watchdog Timer Base Stop Time Register	Setting value of the bit 31 to 24 (WDTBSTKEY bit) in the Watchdog Timer Base Stop Time Register (WDTBST) corrected. Error: R: R Correct: R: 0
Adds by Rev.C	17-7	17.4.1 Using Watchdog Timer Mode	Incorrect description corrected (the 5th line). Error: 4. In watchdog timer mode, the application must periodically clear the WDTCNT counter so that the WDTCNT counter does not overflow. See section 17.4.4, Clearing the WDT Counter, for the procedure for clearing this counter. Correct: 4. In watchdog timer mode, the application must periodically clear the WDTCNT or the WDTBCNT counter so that the WDTCNT counter does not overflow. See section 17.4.4, Clearing the WDT Counter, for the procedure for clearing this counter.
Adds by Rev.C	18-33	18.3.9 (2) Port A Control Register 3	Description of the bit 2 to 0 (PA8MD bit) in the Port A Control Register 3 (PACR3) corrected (the 5th line). Error: 011: DDB08 output (DRI) Correct: 011: DDB08 input (DRI)
Adds by Rev.C	18-41	18.3.11 (4) Port C Control Register 1	Description of the bit 14 to 12 (PC3MD bit) in the Port C Control Register 1 (PCCR1) corrected (the 6th line). Error: 100: SSL20 output (RSPI) Correct: 100: SSL20 input/output (RSPI)
			Description of the bit 10 to 8 (PC2MD bit) in the Port C Control Register 1 (PCCR1) corrected (the 6th line). Error: 100: RSPCK2 output (RSPI) Correct: 100: RSPCK2 input/output (RSPI)
Adds by Rev.C	18-51	18.3.14 (1) Port F Control Register 2	Description of the bit 6 to 4 (PF5MD bit) in the Port F Control Register 2 (PFCR2) corrected (the 3rd line). Error: 001: SCL output (IIC3) Correct: 001: SCL input/output (IIC3)
			Description of the bit 2 to 0 (PF4MD bit) in the Port F Control Register 2 (PFCR2) corrected (the 3rd line). Error: 001: SDA output (IIC3) Correct: 001: SDA input/output (IIC3)
Adds by Rev.C	18-54	18.3.15 (2) Port G Control Register 1	Description of the bit 14 to 12 (PG3MD bit) in the Port G Control Register 1 (PGCR1) corrected (the 5th line). Error: 011: SSL00 output (RSPI) Correct: 011: SSL00 input/output (RSPI)

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Adds by Rev.C	18-67	18.3.18 (3) Port K Control Register 2	Description of the bit 10 to 8 (PK6MD bit) in the Port K Control Register 2 (PKCR2) corrected (the 5th line). Error: 100: TXD3 input/output (SCIF) Correct: 100: TXD3 output (SCIF)
Adds by Rev.C	18-69	18.3.18 (4) Port K Control Register 1	Description of the bit 2 to 0 (PK0MD bit) in the Port K Control Register 1 (PKCR1) corrected (the 4th line). Error: 010: SSL10 output (RSPI) Correct: 010: SSL10 input/output (RSPI)
Adds by Rev.C	18-73	18.3.20 (1) Port M Control Register 4	Description of Notes in the Port M Control Register 4 (PMCR4) corrected. Error: Note: Set PM12 to PM15 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported. Correct: Note: Set PM0 to PM15 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported.
Adds by Rev.C	18-74	18.3.20 (2) Port M Control Register 3	Description of Notes in the Port M Control Register 3 (PMCR3) corrected. Error: Note: Set PM8 to PM11 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported. Correct: Note: Set PM0 to PM15 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported.
Adds by Rev.C	18-75	18.3.20 (3) Port M Control Register 2	Description of Notes in the Port M Control Register 2 (PMCR2) corrected. Error: Note: Set PM4 to PM7 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported. Correct: Note: Set PM0 to PM15 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported.
Adds by Rev.C	18-76	18.3.20 (4) Port M Control Register 1	Description of Notes in the Port M Control Register 1 (PMCR1) corrected. Error: Note: Set PM0 to PM3 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported. Correct: Note: Set PM0 to PM15 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported.
Adds by Rev.C	18-77	18.3.21 (1) Port N Control Register 2	Description of Notes in the Port N Control Register 2 (PNCR2) corrected. Error: Note: Set PN4 to PN7 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported. Correct: Note: Set PN0 to PN7 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported.
Adds by Rev.C	18-78	18.3.21 (2) Port N Control Register 1	Description of Notes in the Port N Control Register 1 (PNCR1) corrected. Error: Note: Set PN0 to PN3 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported. Correct: Note: Set PN0 to PN7 as all analog input pins or all general ports. Setting and using them as a mixture of analog input pins and general ports is not supported.
Adds by Rev.C	20-15	20.3.7 DMAi Channel Control Register	Description of the bit 20 (TS2 bit) in the DMAi Channel Control Register (DMiCHCR) corrected (the 15th line). Error: Note: 16-bit and 32-bit accesses are possible between External address space, IL memory/OL memory, SHwyRAM, and ROM only. Correct: Note: 16-byte and 32-byte accesses are possible between External address space, IL memory/OL memory, SHwyRAM, and ROM only.

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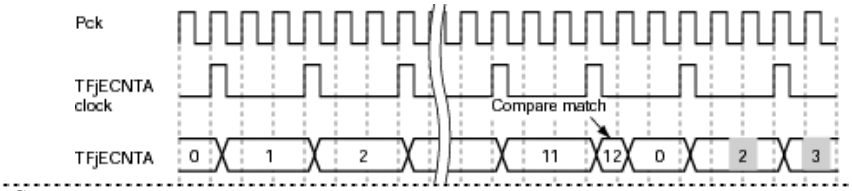
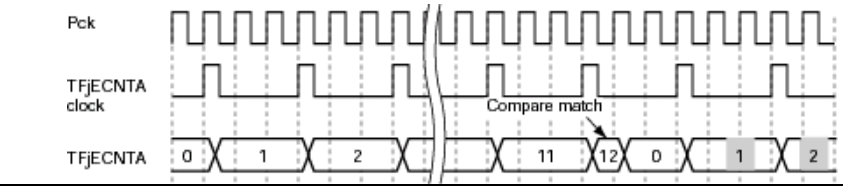
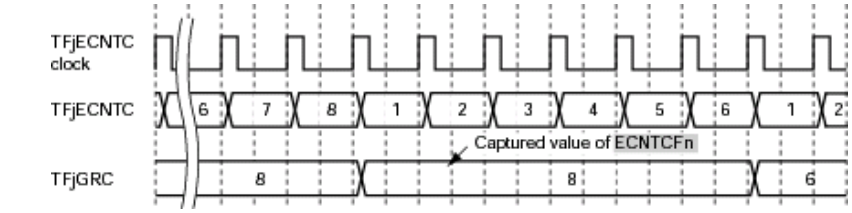
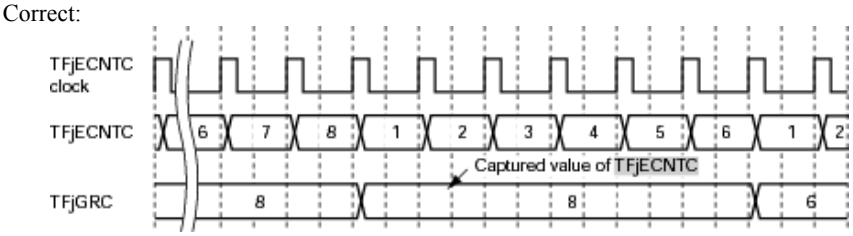
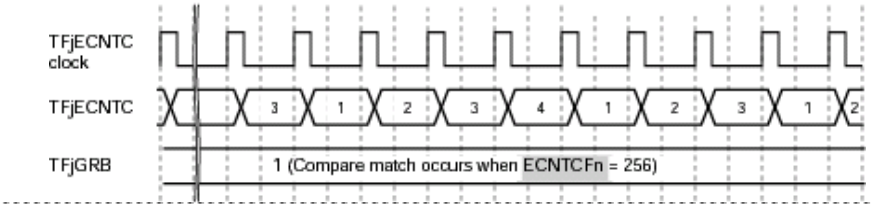
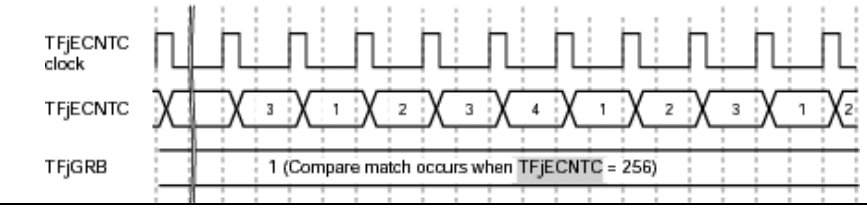
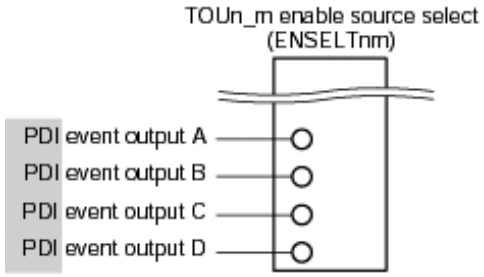
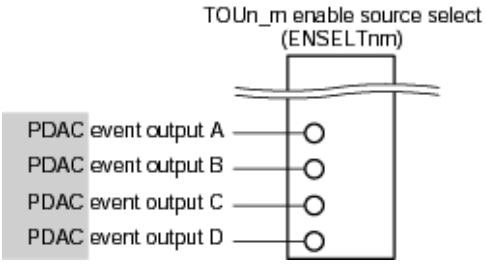
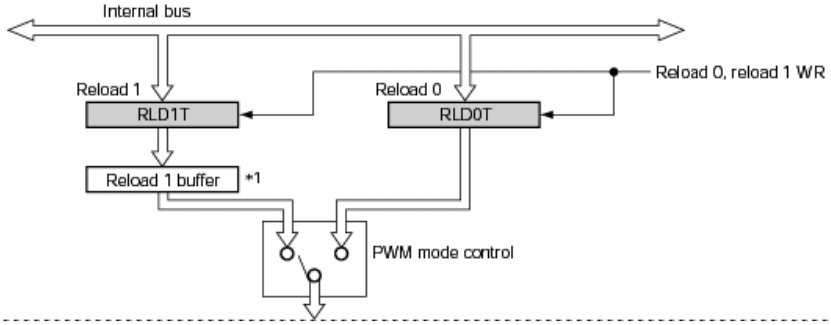
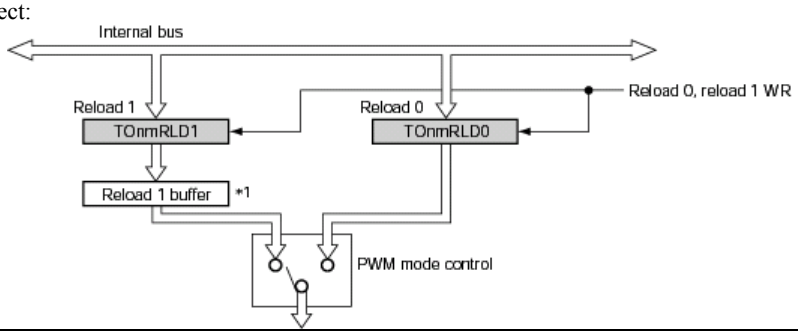
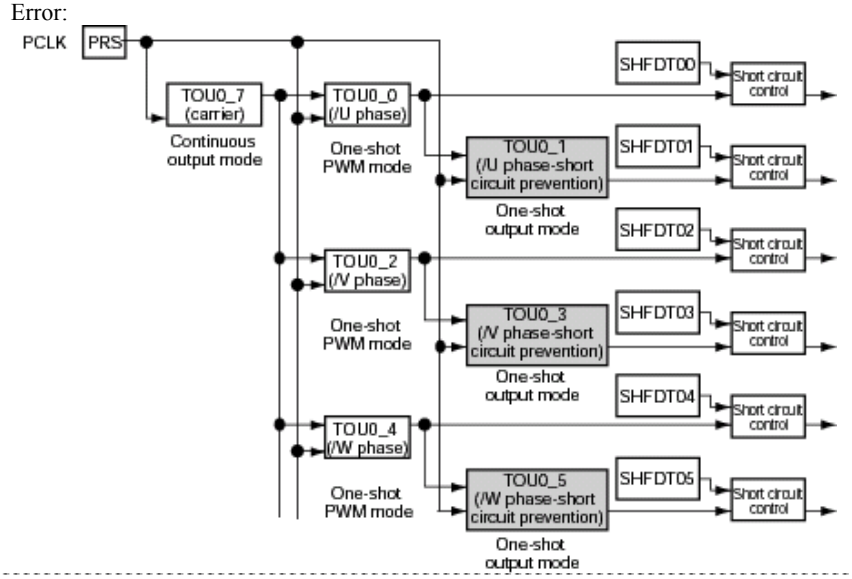
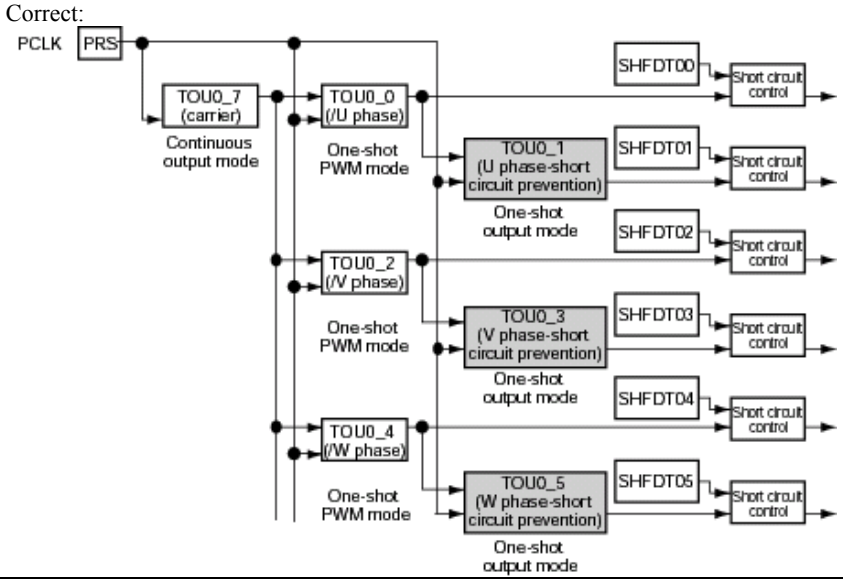
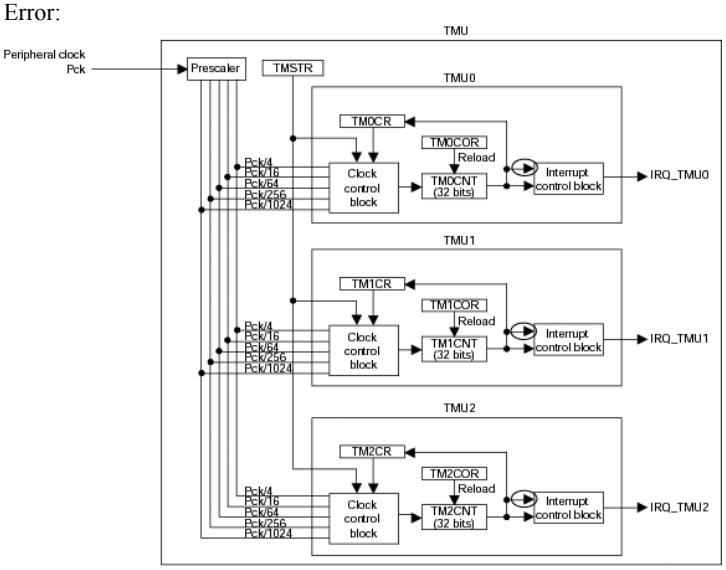
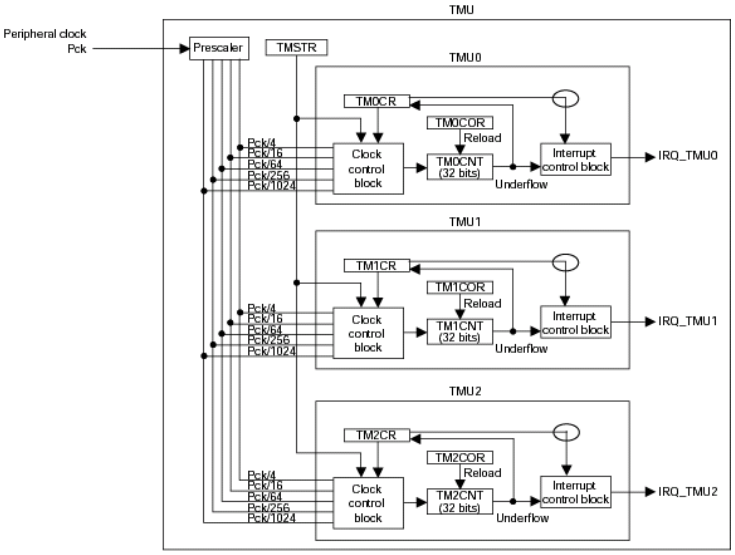
Descriptions of Transfer source and destination changed.
<table>
<tr><th>On-chip Peripheral Module</th><th>DMA Transfer Request Sources</th><th>Setting Value for CnMRID Bit</th><th>Transfer Source</th><th>Transfer Destination</th></tr>
<tr><td>RSPI</td><td>RSPI0 transmit buffer empty</td><td>H’11</td><td>Any*</td><td>Transmit buffer</td></tr>
<tr><td></td><td>RSPI0 receive buffer full</td><td>H’12</td><td>Receive buffer</td><td>Any*</td></tr>
<tr><td></td><td>RSPI1 transmit buffer empty</td><td>H’15</td><td>Any*</td><td>Transmit buffer</td></tr>
<tr><td></td><td>RSPI1 receive buffer full</td><td>H’16</td><td>Receive buffer</td><td>Any*</td></tr>
<tr><td></td><td>RSPI2 transmit buffer empty</td><td>H’19</td><td>Any*</td><td>Transmit buffer</td></tr>
<tr><td></td><td>RSPI2 receive buffer full</td><td>H’1A</td><td>Receive buffer</td><td>Any*</td></tr>
</table>
<table>
<tr><th>On-chip Peripheral Module</th><th>DMA Transfer Request Sources</th><th>Setting Value for CnMRID Bit</th><th>Transfer Source</th><th>Transfer Destination</th></tr>
<tr><td>RSPI</td><td>RSPI0 transmit buffer empty</td><td>H’11</td><td>Any</td><td>SP0DR</td></tr>
<tr><td></td><td>RSPI0 receive buffer full</td><td>H’12</td><td>SP0DR</td><td>Any</td></tr>
<tr><td></td><td>RSPI1 transmit buffer empty</td><td>H’15</td><td>Any</td><td>SP1DR</td></tr>
<tr><td></td><td>RSPI1 receive buffer full</td><td>H’16</td><td>SP1DR</td><td>Any</td></tr>
<tr><td></td><td>RSPI2 transmit buffer empty</td><td>H’19</td><td>Any</td><td>SP2DR</td></tr>
<tr><td></td><td>RSPI2 receive buffer full</td><td>H’1A</td><td>SP2DR</td><td>Any</td></tr>
</table></td></tr>
<tr><td>Adds by Rev.C</td><td>21-20</td><td>21.6.2 ATU-IIIS Clock Bus Control Register</td><td>Description of the bit 1 to 0 (CB5EG bit) in the ATU-IIIS Clock Bus Control Register (ATCBCNT) deleted (the 7th line).
Deleted: When the multiplied-and-corrected clock is selected as the source for line 5 of the clock bus, the setting of these bits is invalid.</td></tr>
<tr><td>Adds by Rev.C</td><td>21-28</td><td>21.7 Overview of Prescalers</td><td>Incorrect description corrected (the 12th line).
Error: Synchronization of a prescaler is not possible after it has started or its division ratio has been changed.
Correct: Synchronization of the prescalers is not possible when its division ratio has been changed after the prescalers have started.</td></tr>
<tr><td>Adds by Rev.C</td><td>21-33</td><td>21.11.1 TAi Control Register</td><td>Description of the bit 2 to 0 (CKSELA bit) in the TAi Control Register (TAiCR) corrected (the 5th line).
Error: Clock-bus line 5 supplies externally input clock B (TCLKB) or the multiplied-and-corrected clock output by timer B.
Correct: Clock-bus line 5 supplies externally input clock B (TCLKB).</td></tr>
<tr><td>Adds by Rev.C</td><td>21-34</td><td>21.11.2 TAiI/O Control Register 1</td><td>Description of the bit 11 to 0 (IOA5 to IOA0 bit) in the TAiI/O Control Register 1 (TAiIO1) corrected (the 11th line).
Error: When the noise canceler is disabled, the selected edge is simply extracted from the external inputs (TIA00 to TIA05 and TIA10 to TIA15).
Correct: Edge extraction is executed to a signal after noise removal. When the noise canceler is disabled, the selected edge is simply extracted from the external inputs (TIA00 to TIA05 and TIA10 to TIA15).</td></tr>
<tr><td>Adds by Rev.C</td><td>21-42</td><td>21.11.8 TAik Noise Canceler Counter</td><td>Incorrect description deleted (the 33th line).
Deleted: When the NCEA bits are cleared to 0 while the counter is being incremented, counting continues until the values in the counter and the noise canceler register match or a level change on the externally input signal is detected.</td></tr>
<tr><td>Adds by Rev.C</td><td>21-49</td><td>21.13 Overview of Timer F</td><td>Incorrect description corrected (the 4th line).
Error: Counts the number of edges input to the external input pin (TIFjA) period.
Correct: Counts the number of edges input to the external input pin (TIFjA) in a specified period.</td></tr>
</table>

Rev.	Page	Part	Contents
Adds by Rev.C	21-54	21.14.2 TF Noise Canceller Control Register	Description of the bit 3 to 0 (NCEF3 to NCEF0 bit) in the TF Noise Canceller Control Register (TFNCCR) corrected (the 31th line). Error: If a noise change is detected, this change is regarded as noise and the noise canceller does not change the signal after a noise cancel regarding that no level change of input signal occurred. Correct: If a noise change is detected until a compare match occurs, this change is regarded as noise and the noise canceller does not change the signal after a noise cancel regarding that no level change of input signal occurred.
Adds by Rev.C	21-73	Figure 21.14 Operation Example of Edge Count in Given Time	Figure 21.14 Operation Example of Edge Count in Given Time: Value of TFjECNTA corrected. Error:  Correct: 
Adds by Rev.C	21-78	Figure 21.19 Operation Example of Measurement of PWM Input Waveform Timing	Figure 21.19 Operation Example of Measurement of PWM Input Waveform Timing: Description of TFjGRC corrected. Error:  Correct: 
Adds by Rev.C	21-79	Figure 21.20 Operation Example of Rotation Speed/Pulse Measurement	Figure 21.20 Operation Example of Rotation Speed/Pulse Measurement: Description of TFjGRB corrected. Error:  Correct: 
Adds by Rev.C	21-83	21.16 Overview of Timer G	Incorrect description corrected (the 4th line). Error: The generated pulse is used to activate the A/D converter or interrupt trigger. Correct: The generated pulse is used to activate as the starting/interrupt trigger of the A/D converter.

Rev.	Page	Part	Contents
Adds by Rev.C	21-100	Figure 21.27 TOU Enable Circuit Configuration Diagram	Figure 21.27 TOU Enable Circuit Configuration Diagram: Description of TOUn_m enable source corrected. Error:  Correct: 
Adds by Rev.C	21-112	21.20.16 TOUnPWM Output-Prohibit Control Register	Setting value of the bit 15 to 8 (ATUKEY bit) in the TOUnPWM Output-Prohibit Control Register (TOnPODISCR) corrected. Error: R: R Correct: R: 0
Adds by Rev.C	21-128	Figure 21.28 Operation Example of PWM Output Mode	Figure 21.28 Operation Example of PWM Output Mode: Notes corrected. Error: *2 The value of the reload 1 register is reloaded in the counter. Correct: *2 The value of the reload 1 buffer is reloaded in the counter.
Adds by Rev.C	21-129	21.21.1 (2) Reload Register Updating in PWM Output Mode	Incorrect description corrected (the 7th line). Error: Normally this operation is performed all at once, with a 32-bit word access starting at the reload 1 register address. Correct: Normally this operation is performed all at once, with a 32-bit access starting at the reload 1 register address.
Adds by Rev.C	21-129	Figure 21.29 PWM Circuit Diagram	Figure 21.29 PWM Circuit Diagram: Description of reload register corrected. Error:  Correct: 
Adds by Rev.C	21-142	Figure 21.39 Operation Example of One-Shot PWM Output Mode (Reload 0 Register: H'FFFF)	Figure 21.39 Operation Example of One-Shot PWM Output Mode (Reload 0 Register: H'FFFF): Notes corrected. Error: *1 The value of the reload 1 register is reloaded in the counter because the reload 1 register is set to H'FFFF. Correct: *1 The value of the reload 1 register is reloaded in the counter because the reload 0 register is set to H'FFFF.

<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th>Contents</th></tr>
<tr><td>Adds by Rev.C</td><td>21-150</td><td>21.21.7 (1) Disabling PWM Output by Using a Signal on an External Pin</td><td>Incorrect description corrected (the 10th line).
Error: Disabling PWM output when a signal is input on PWMOFFn A. Write an appropriate setting value ("000", "001", "010", "011", "10X" or "11X") to the POSTn bits in the TOnPOCR register.
Correct: Disabling PWM output when a signal is input on PWMOFFn A. Write an appropriate setting value ("001", "010", "011", "10X" or "11X") to the POSTn bits in the TOnPOCR register..</td></tr>
<tr><td>Adds by Rev.C</td><td>21-158</td><td>Figure 21.49 Timer Configuration Diagram</td><td>Figure 21.49 Timer Configuration Diagram: Description of TOU0_1,TOU0_3,TOU0_5 corrected.
Error:
 

Correct:
 
</td></tr>
</table>

<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th>Contents</th></tr>
<tr><td rowspan="3">Adds by Rev.C</td><td rowspan="3">22-1</td><td rowspan="3">Figure 22.1 Block Diagram of TMU</td><td>Figure 22.1 Block Diagram of TMU: Incorrect description corrected. O in a figure shows the corrected part.
Error:
 
</td></tr>
<tr><td>Correct:
 
</td></tr>
<tr><td></td></tr>
<tr><td>Adds by Rev.C</td><td>23-14</td><td>23.3.7 SCi Serial Status Register</td><td>Description of the bit 5 (TDFE bit) in the SCi Serial Status Register (SCiFSR) corrected (the 10th line).
Error: 1: Indicates that the number of transmit data items written to the SCiFTDR register is less than the specified transmit trigger count*2.
Correct: 1: Indicates that the number of transmit data items written to the SCiFTDR register is less than or equal to the specified transmit trigger count*2.</td></tr>
<tr><td rowspan="3">Adds by Rev.C</td><td rowspan="3">23-16</td><td rowspan="3">23.3.7 SCi Serial Status Register</td><td>Description of the bit 1 (RDF bit) in the SCi Serial Status Register (SCiFSR) corrected (the 8th, 20th lines).
Error: 1: Indicates that the number of SCiFRDR register receive data items is greater than the specified receive trigger count</td></tr>
<tr><td>Correct: 1: Indicates that the number of SCiFRDR register receive data items is greater than or equal to the specified receive trigger count</td></tr>
<tr><td>Error: RDF is set to "1" when a quantity of receive data more than the specified receive trigger number is stored in the SCiFRDR register*2
Correct: RDF is set to "1" when a quantity of receive data more than or equal to the specified receive trigger number is stored in the SCiFRDR register*2</td></tr>
</table>

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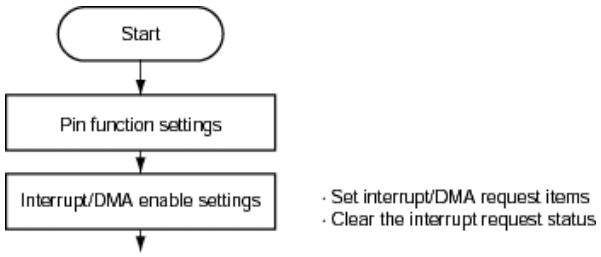
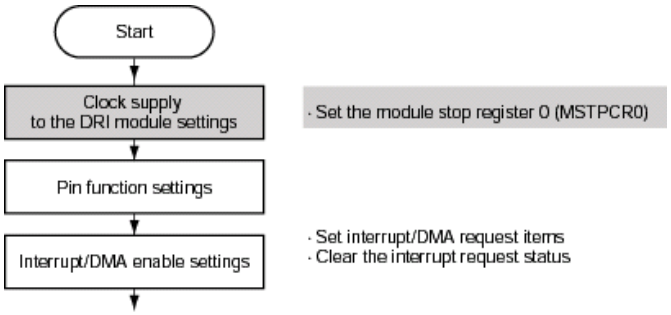
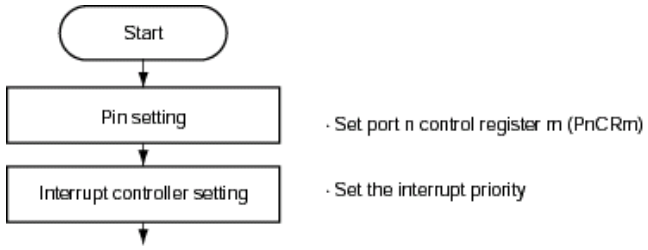
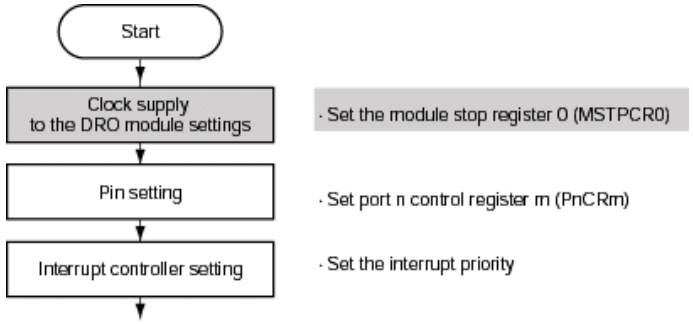
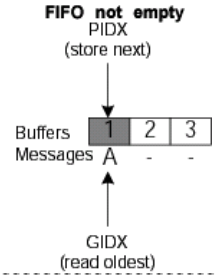
Adds by Rev.C	23-23	23.3.9 SCi FIFO Control Register	Description of the bit 10 to 8 (RSTRG bit) in the SCi FIFO Control Register (SCiFCR) corrected (the 2nd line). Error: When the quantity of receive data in the SCi receive FIFO data register (SCiFRDR) becomes more than the number shown below, RTSi# signal is set to "H" level.. Correct: When the quantity of receive data in the SCi receive FIFO data register (SCiFRDR) becomes more than or equal to the number shown below, RTSi# signal is set to "H" level.
			Description of the bit 7 to 6 (RTRG bit) in the SCi FIFO Control Register (SCiFCR) corrected (the 3rd line). Error: The RDF flag is set to "1"when the quantity of receive data stored in the SCi receive FIFO register (SCiFRDR) is increased more than the set trigger number shown below. Correct: The RDF flag is set to "1" when the quantity of receive data stored in the SCi receive FIFO register(SCiFRDR) is increased more than or equal to the set trigger number shown below.
Adds by Rev.C	23-24	23.3.9 SCi FIFO Control Register	Description of the bit 5 to 4 (TTRG bit) in the SCi FIFO Control Register (SCiFCR) corrected (the 4th line). Error: The TDFE flag is set to "1" when the quantity of transmit data in the SCi transmit FIFO data register (SCiFTDR) becomes less than the set trigger number shown below. Correct: The TDFE flag is set to "1" when the quantity of transmit data in the SCi transmit FIFO data register (SCiFTDR) becomes less than or equal to the set trigger number shown below.
Adds by Rev.C	23-36	23.4.2 (3) Transmitting and Receiving Data	Incorrect description corrected (the 6th line). Error: 2. When data is transferred from the SCiFTDR register to the SCiTSR register and transmission is started, consecutive transmit operations are performed until there is no transmit data left in the SCiFTDR register. When the number of transmit data bytes in the SCiFTDR register falls below the transmit trigger number set in the SCiFIFO control register (SCiFCR), the TDFE flag is set. If the TIE bit in the SCi serial control register (SCiSR) is set to "1" at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated. Correct: 2. When data is transferred from the SCiFTDR register to the SCiTSR register and transmission is started, consecutive transmit operations are performed until there is no transmit data left in the SCiFTDR register. When the number of transmit data bytes in the SCiFTDR register falls below the transmit trigger number set in the SCiFIFO control register (SCiFCR), the TDFE flag is set. If the TIE bit in the SCi serial control register (SCiSCR) is set to "1" at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated.
Adds by Rev.C	23-46	23.5 SCIFi Interrupt	Incorrect title corrected (the 1st line). Error: 23.5 SCIF Interrupts Correct: 23.5 SCIFi Interrupt Sources and DMAC
Adds by Rev.C	24-62	24.4.13 Interrupt Sources	Incorrect description corrected (the 3rd line). Error: The receive buffer full interrupt is assigned to vector address sp_rxint, the transmit buffer empty interrupt to sp_txint,and the mode fault and overrun interrupts to sp_errint. Correct: The receive buffer full interrupt is assigned to vector address SPRIn, the transmit buffer empty interrupt to SPTIn,and the mode fault and overrun interrupts to SPEIn.

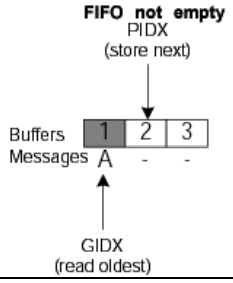
<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th>Contents</th></tr>
<tr><td>Adds by Rev.C</td><td>24-62</td><td>Table 24.12 RSPIi Interrupt Sources Interrupt Condition</td><td>Table 24.12 RSPIi Interrupt Sources Interrupt Condition: Item of Name and Abbreviation deleted.
Error:
<table>
<tr><th>Name</th><th>Interrupt Source</th><th>Abbreviation</th><th>Interrupt Condition</th></tr>
<tr><td>sp_rxint</td><td>Receive buffer full</td><td>RXI</td><td>(SPiCR.SPRIE = 1) & (SPiSR.SPRF = 1)</td></tr>
<tr><td>sp_txint</td><td>Transmit buffer empty</td><td>TXI</td><td>(SPiCR.SPTIE = 1) & (SPiSR.SPTEF = 1)</td></tr>
<tr><td rowspan="2">sp_errint</td><td>Mode fault MOI</td><td>MOI</td><td>(SPiCR.SPEIE = 1) & (SPiSR.MODF = 1)</td></tr>
<tr><td>Overrun</td><td>OVI</td><td>(SPiCR.SPEIE = 1) & (SPiSR.OVRF = 1)</td></tr>
</table>
Correct:
<table>
<tr><th>Interrupt Source</th><th>Interrupt Condition</th></tr>
<tr><td>Receive buffer full</td><td>(SPiCR.SPRIE = 1) & (SPiSR.SPRF = 1)</td></tr>
<tr><td>Transmit buffer empty</td><td>(SPiCR.SPTIE = 1) & (SPiSR.SPTEF = 1)</td></tr>
<tr><td>Mode fault MOI</td><td>(SPiCR.SPEIE = 1) & (SPiSR.MODF = 1)</td></tr>
<tr><td>Overrun</td><td>(SPiCR.SPEIE = 1) & (SPiSR.OVRF = 1)</td></tr>
</table></td></tr>
<tr><td>Adds by Rev.C</td><td>25-16</td><td>25.4.2 Master Transmit Operation</td><td>Incorrect description corrected (the 9th line).
Error: 3. After confirming that TDRE flag in the ICSR register has been set, write the transmit data (the first byte data show the slave address and R/W#) to the ICDRT register. At this time, TDRE flag is automatically cleared to "0", and data is transferred from the ICDR register to the ICDRS register. TDRE flag is set again.
Correct: 3. After confirming that TDRE flag in the ICSR register has been set, write the transmit data (the first byte data show the slave address and R/W#) to the ICDRT register. At this time, TDRE flag is automatically cleared to "0", and data is transferred from the ICDRT register to the ICDRS register. TDRE flag is set again.</td></tr>
<tr><td>Adds by Rev.C</td><td>25-23</td><td>25.4.6 (3) Receive Operation</td><td>Incorrect description corrected (the 18th line).
Error: Notes: 3. Check if the BC bit in the ICMR register is set to "1" and then set the RCVD bit in the ICCR1 register to "1".
Correct: Notes: 3. Check if the BC bit in the ICMR register is set to "1xx" and then set the RCVD bit in the ICCR1 register to "1".</td></tr>
<tr><td>Adds by Rev.C</td><td>25-25</td><td>Figure 25.18 I²C Bus Interface 3 Reset Procedure Example Using the IICRST BIT</td><td>Figure 25.18 I²C Bus Interface 3 Reset Procedure Example Using the IICRST BIT:
Incorrect description corrected (the 9th line).
Error: (4) Wait until the bus is in the bus released state. The bus released state can be recognized by a variety of means, including reading the I/O ports corresponding to SCL and SDA (the PF5PR and PF4PR bits in the PFPRL register).
Correct: (4) Wait until the bus is in the bus released state. The bus released state can be recognized by a variety of means, including reading the I/O ports corresponding to SCL and SDA (the PF5PR and PF4PR bits in the PFPR register).</td></tr>
<tr><td>Adds by Rev.C</td><td>25-33</td><td>25.8.8 Register Initialization with the IICRST Bit</td><td>Incorrect description corrected (the 3rd line).
Error: In master transmit mode and master receive mode, the ICSR register TDRE flag is set to "1" when "1" is written to the IICRST bit.
Correct: In master transmit mode and slave transmit mode, the ICSR register TDRE flag is set to "1" when "1" is written to the IICRST bit.</td></tr>
<tr><td>Adds by Rev.C</td><td>26-15</td><td>Table 26.4 Mailbox Configuration</td><td>Table 26.4 Mailbox Configuration: Incorrect description corrected.
Error: Notes 4. The corresponding bits in the CiMKIVLR register for mailboxes [56] to [63] are disabled. Set 0 to these bits.
Correct: Notes 4. The corresponding bits in the CiMKIVLR1 register for mailboxes [56] to [63] are disabled. Set 0 to these bits.</td></tr>
<tr><td>Adds by Rev.C</td><td>26-34</td><td>26.3.9 CANi Message Control Register j</td><td>Incorrect description corrected (the 12th line).
Error: Receive mailbox setting enabled (When the TRMREQ bit is "1" and the RECREQ bit is "0")
Correct: Receive mailbox setting enabled (When the TRMREQ bit is "0" and the RECREQ bit is "1")</td></tr>
<tr><td>Adds by Rev.C</td><td>26-57</td><td>26.3.20 CANi Error Interrupt Factor Judge Register</td><td>Description of the bit 7 (BLIF bit) in the CANi Error Interrupt Factor Judge Register (CiEIFR) corrected (the 4th line).
Deleted: After the BLIF bit is set to "1", 32 consecutive dominant bits are detected again under either of the following conditions:</td></tr>
</table>

<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th>Contents</th></tr>
<tr><td>Adds by Rev.C</td><td>27-2</td><td>Table 27.1 Overview of the ADC</td><td>Table 27.1 Overview of the ADC: Incorrect description corrected.
Error:<table><tr><th>Item</th><th>Description</th></tr><tr><td>Support for scan conversion end interrupt (ADI), interrupt conversion end interrupt (ADID), and DMA transfer function</td><td>On completion of scanning for scan conversion, a scan conversion end interrupt request (ADI) can be generated or the DMAC can be started.</td></tr></table>Correct:<table><tr><th>Item</th><th>Description</th></tr><tr><td>Support for scan conversion end interrupt (ADI), interrupt conversion end interrupt, and DMA transfer function</td><td>On completion of scanning for scan conversion, a scan conversion end interrupt request (AD0I, AD1I) can be generated or the DMAC can be started.</td></tr></table></td></tr>
<tr><td rowspan="3">Adds by Rev.C</td><td>27-9</td><td rowspan="2">27.4.1 (1) A/D0 Data Registers 0 to 7 and A/D1 Data Registers 0 to 7</td><td>Incorrect description corrected (the 5th, 7th lines).
Error: The other bits are reserved. They are always read as "0", and the write value should always be "0".
Correct: The other bits are reserved. They are always read as "0".</td></tr>
<tr><td>27-9
27-10</td><td>Description of the Reserved bits in the A/D0 Data Registers 0 to 7 (AD0DR0 to AD0DR7) and A/D1 Data Registers 0 to 7 (AD1DR0 to AD1DR7) deleted (the 2nd line).
Deleted: The write value should always be "0".
Setting value of the Reserved bits in the A/D0 Data Registers 0 to 7 and A/D1 Data Registers 0 to 7 corrected.
Error: W: 0
Correct: W: -</td></tr>
<tr><td>Adds by Rev.C</td><td>27-11</td><td>27.4.1 (2) A/D0 Data Registers 8 to 15</td><td>Incorrect description corrected (the 4th line).
Error: The other bits are reserved. They are always read as "0", and the write value should always be "0".
Correct: The other bits are reserved. They are always read as "0".
Description of the Reserved bits in the A/D0 Data Registers 8 to 15 (AD0DR8 to AD0DR15) deleted (the 2nd line).
Deleted: The write value should always be "0".
Setting value of the Reserved bits in the A/D0 Data Registers 8 to 15 corrected.
Error: W: 0
Correct: W: -</td></tr>
<tr><td>Adds by Rev.C</td><td>27-12</td><td>27.4.1 (3) A/D0 Data Register DIAG0 and A/D1 Data Register DIAG1</td><td>Incorrect description corrected (the 4th line).
Error: The other bits are reserved. They are always read as "0", and the write value should always be "0".
Correct: The other bits are reserved. They are always read as "0".
Description of the Reserved bits in the A/D0 Data Register DIAG0 and A/D1 Data Register DIAG1 (AD0DRD and AD1DRD) deleted (the 2nd line).
Deleted: The write value should always be "0".
Setting value of the Reserved bits in the A/D0 Data Register DIAG0 and A/D1 Data Register DIAG1 (AD0DRD and AD1DRD) corrected.
Error: W: 0
Correct: W: -</td></tr>
<tr><td>Adds by Rev.C</td><td>27-15</td><td>27.4.3 A/Di Control Extended Register</td><td>Description of the bit 11 (DIAGM bit) in the A/Di Control Extended Register (ADiCER) corrected (the 12th line).
Error: To prevent incorrect operation, the DIAGM bit must be switched only while the ADSCSCT bit in the ADREF register is set to "0".
Correct: To prevent incorrect operation, the DIAGM bit must be switched only while the ADSCACT bit in the ADiREF register is set to "0".</td></tr>
<tr><td>Adds by Rev.C</td><td>27-41</td><td>Figure 27.9 External Trigger Input Timing</td><td>Figure 27.9 External Trigger Input Timing: Legend corrected.
Error: tD4: Time until the falling of the ADSCACT bit after the rising of the ADiTRG# pin is sampled
Correct: tD4: Time until the rising of the ADSCACT bit after the falling of the ADiTRG# pin is sampled</td></tr>
<tr><td>Adds by Rev.C</td><td>28-29</td><td>28.3.13 DRIi Transfer Control Register</td><td>Description of the bit 1 (DBST bit) in the DRIi Transfer Control Register (DRIiTRMCNT) corrected (the 4th line).
Error: To prevent loss of DRI transfer data within the DRI module, the module includes a 32 bits by 4 stage intermediate buffer, and this DBST bit will be "1" in the state where there is data present in this intermediate buffer.
Correct:To prevent loss of DRI transfer data within the DRI module, the module includes a 32 bits by 4 stage intermediate buffer, and this DBST bit will be "1" in the state where there is data present in this intermediate buffer. On the other hand, the DBST bit is a value "0" when there is no data in the intermediate buffer.</td></tr>
</table>

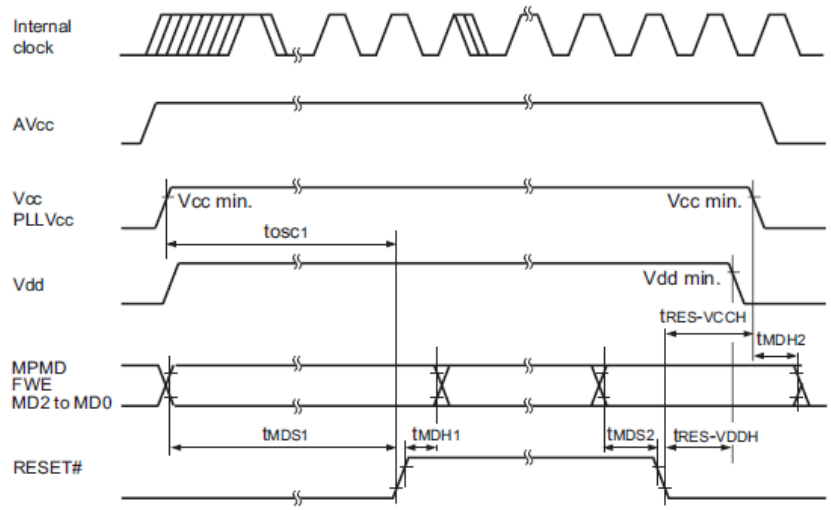
Rev.	Page	Part	Contents
Adds by Rev.C	28-32	28.3.14 DRIi Special Mode Register	Description of the bit 3 (SPMEN bit) in the DRIi Special Mode Register (DRIiSPMOD) corrected (the 6th line). Error: DRIi data acquisition control register (DRIiDCAPCNT) 1. DSDSL (input data bus width) bits Correct: DRIi data acquisition control register (DRIiDCAPCNT) 1. DWDSL (input data bus width) bits
Adds by Rev.C	28-36	28.3.15 DRIi Data Acquisition Control Register	Description of the bit 10 (DWRPR bit) in the DRIi Data Acquisition Control Register (DRIiDCAPCNT) corrected (the 3rd,8th,9th lines). Error: DEXLS Correct: DEXSL
Adds by Rev.C	28-43	28.3.20 DRIi Data Acquisition Event Count Setting Register	Incorrect description corrected (the 5th line). Error: When special mode is selected, this register must be set to a value that meets the conditions listed in table 28.6 according to the setting of the DRIi data acquisition control register (DRIiDCAPCNT) DSDSL (input data bus width selection) bit. Correct: When special mode is selected, this register must be set to a value that meets the conditions listed in table 28.6 according to the setting of the DRIi data acquisition control register (DRIiDCAPCNT) DWDSL (input data bus width selection) bit.
Adds by Rev.C	28-65	Figure 28.8 DRI Initialization Flowchart	Figure 28.8 DRI Initialization Flowchart: "Clock supply to the DRI module settings" added. Error:  Correct: 
Adds by Rev.C	28-66	28.4.2 (1) One-shot mode	Incorrect description corrected. Error: From that point on, the counter is decremented each time the event selected by the DECmCTSL (DECm count event selection) bits occurs. Correct: From that point on, the counter is decremented each time the event selected by the DECmCS (DECm count event selection) bits occurs.

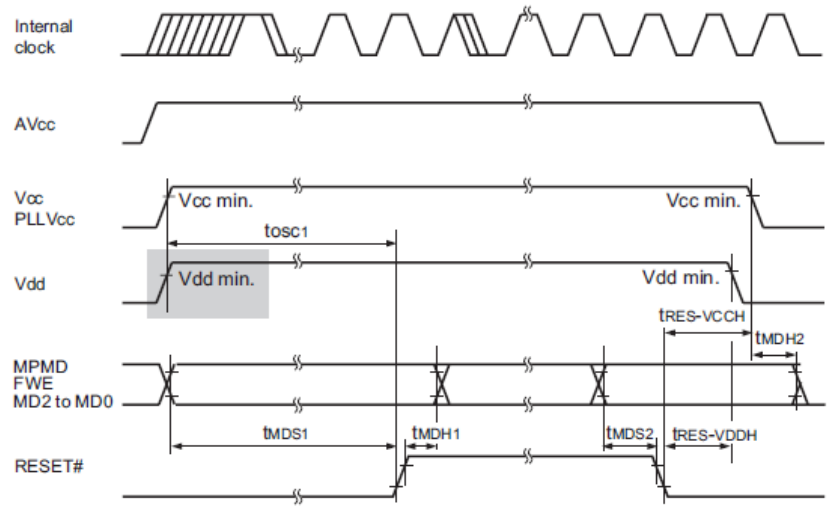
Rev.	Page	Part	Contents
Adds by Rev.C	29-12	Figure 29.3 DRO Setup Example	Figure 29.3 DRO Setup Example: "Clock supply to the DRO module settings" added. Error:  Correct: 
Adds by Rev.C	30-8	30.4.4 PDAC Status Register	Setting value of the bit 7 (DWOUT bit) in the PDAC Status Register (PDISTATUS) corrected. Error: W: W Correct: W: -
			Setting value of the bit 6 to 4 (DWMON bit) in the PDAC Status Register (PDISTATUS) corrected. Error: W: W Correct: W: -
Adds by Rev.C	30-58	30.8 Usage Notes	Notes added. Added: To use the PDAC, set the PDAC bit in the module stop register 0 (MSTPCR0) to "0" to enable PDAC and PSEL operations, and then set the PDAC related register. Otherwise, the clocks are not supplied to the PDAC module and PDAC operation is disabled even though the PDAC related register is set.
Adds by Rev.C	32-15	32.4.2 FlexRay Lock Register	Description of the bit 7 to 0 (CLK7 to CLK0 bit) in the FlexRay Lock Register (FRLCK) corrected (the 2nd line). Error: To leave CONFIG state by writing bits CMD3 to CMD1 in the FRSUCC1 register (commands READY), the write operation has to be directly preceded by two write accesses to the Configuration Lock Key (unlock sequence). Correct: To leave CONFIG state by writing bits CMD3 to CMD0 in the FRSUCC1 register (commands READY), the write operation has to be directly preceded by two write accesses to the Configuration Lock Key (unlock sequence).
Adds by Rev.C	32-18	32.5.1 FlexRay Error Interrupt Register	Description of the bit 9 (IIBA bit) in the FlexRay Error Interrupt Register (FREIR) corrected (the 16th line). Error: (2) The CPU writes to any register of the Input Buffer while the IBSYH bit in the FRIBCR register is set to "1". 0: No illegal CPU access to Output Buffer occurred 1: Illegal CPU access to Output Buffer occurred Correct: (2) The CPU writes to any register of the Input Buffer while the IBSYH bit in the FRIBCR register is set to "1". 0: No illegal CPU access to Input Buffer occurred 1: Illegal CPU access to Input Buffer occurred
Adds by Rev.C	32-65	32.6.8 FlexRay GTU Configuration Register 1	Description of the bit 19 to 0 (UT19 to UT0 bit) in the FlexRay GTU Configuration Register 1 (FRGTUC1) corrected (the 2nd line). Error: Configures the duration of the communication cycle in microticks. Valid value are 640 to 64000 uT. Correct: Configures the duration of the communication cycle in microticks. Valid value are 640 to 640000 uT.
Adds by Rev.C	32-76	32.7.1 FlexRay CC Status Vector Register	Description of the bit 29 to 24 (PSL5 to PSL0 bit) in the FlexRay CC Status Vector Register (FRCCSV) corrected (the 5th line). Error: Set to B'000100 when leaving HALT state. Correct: Set to B'000000 when leaving HALT state.

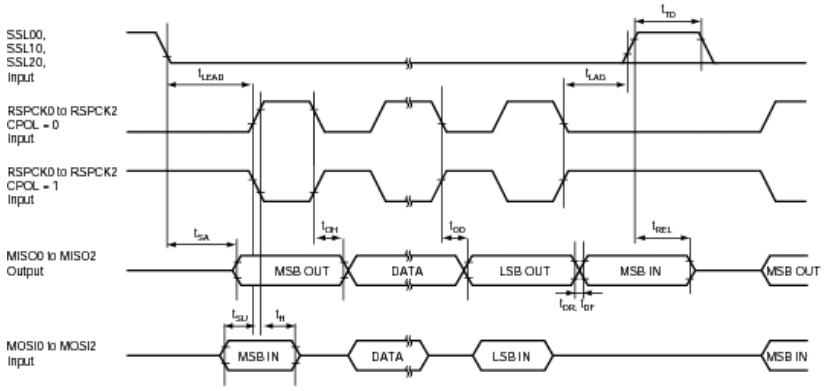
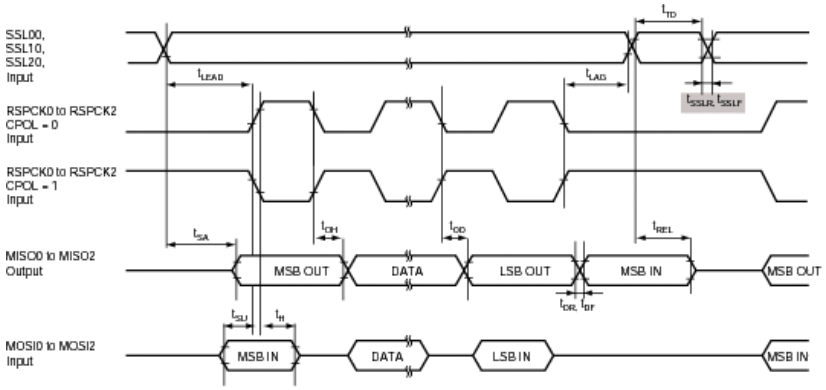
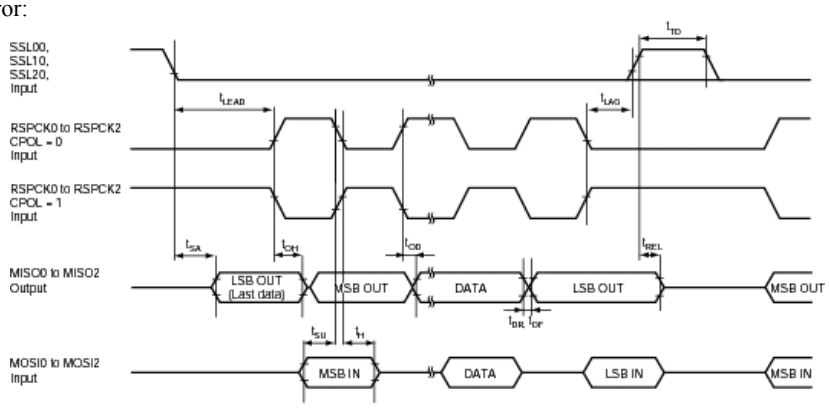
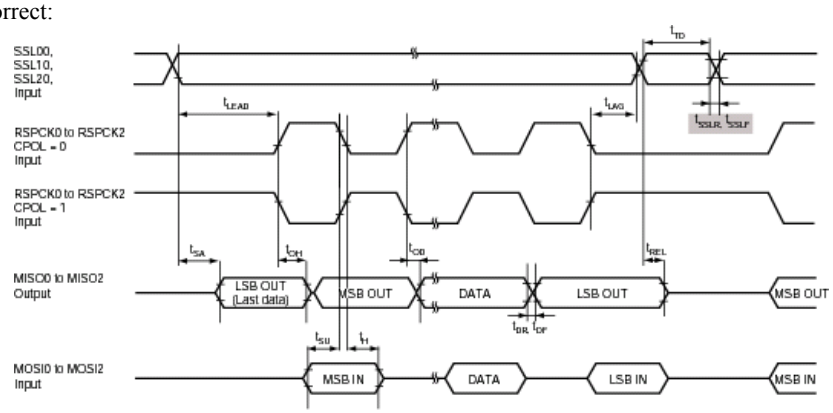
<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th>Contents</th></tr>
<tr><td>Adds by Rev.C</td><td>32-144</td><td>Figure 32.6 Overall State Diagram of FlexRay Communication Controller</td><td>Figure 32.6 Overall State Diagram of FlexRay Communication Controller: Description corrected.
Error: HW Reset Power ON FlexRay Module Initialization (FR bit = 1)
Correct: HW Reset Power ON FlexRay Module Initialization.</td></tr>
<tr><td>Adds by Rev.C</td><td>32-144</td><td>32.16.1 Communication Controller State Diagram</td><td>Incorrect description corrected (the 3rd line).
Error: State transitions are controlled by externals pins RESET, FRXA, and FRXB by the POC state machine, and by the CHI Command Vector (bits CMD3 to CMD0 in the FRSUCC1 register), and also by the FR bit in the FRR register.
Correct: State transitions are controlled by externals pins RESET, FRXA, and FRXB by the POC state machine, and by the CHI Command Vector (bits CMD3 to CMD0 in the FRSUCC1 register).</td></tr>
<tr><td>Adds by Rev.C</td><td>32-166</td><td>Figure 32.10 FIFO Status: Empty, Not Empty, Overrun</td><td>Figure 32.10 FIFO Status: Empty, Not Empty, Overrun: Description corrected.
Error:
 

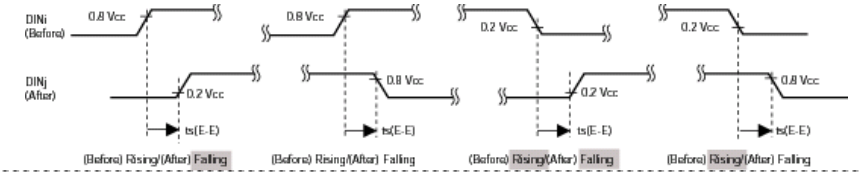
Correct:
 
</td></tr>
<tr><td>Adds by Rev.C</td><td>33-5</td><td>33.4 Usage Notes</td><td>Description added.
Added: Execute read and write accesses to the register area of a module in the module stopped state after supplying the clock to the corresponding module.</td></tr>
<tr><td>Adds by Rev.C</td><td>36-5</td><td>36.4.1 AUDR Enable Register</td><td>Setting value of the bit 15 to 8 (AUDREKEY bit) in the AUDR Enable Register (AUDRENB) corrected.
Error: R: R
Correct: R: 0</td></tr>
<tr><td>Adds by Rev.C</td><td>36-9</td><td>36.5.3 (1) Input Format</td><td>Description of the SIZ[1:0] bits in DIR command corrected.
Error:
<table>
<tr><th>Bit Name</th><th>Function</th><th>Description</th></tr>
<tr><td>SIZ[1:0]</td><td>Access size specification</td><td>00: Byte (8bit)
01: Word (16bit)
10: Long word (32bit)
11: Illegal value</td></tr>
</table>
Correct:
<table>
<tr><th>Bit Name</th><th>Function</th><th>Description</th></tr>
<tr><td>SIZ[1:0]</td><td>Access size specification</td><td>00: Byte (8bit)
01: Word (16bit)
10: Long word (32bit)
11: Setting prohibited</td></tr>
</table></td></tr>
</table>

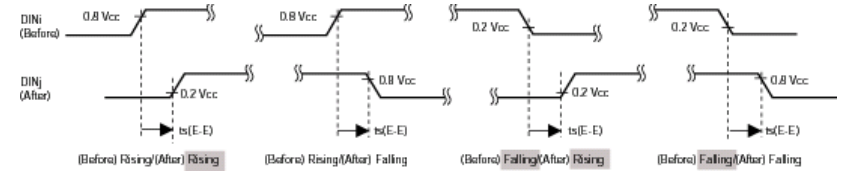
<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th>Contents</th></tr>
<tr><td>Adds by Rev.C</td><td>38-8</td><td>Table 38.7
DC Characteristics-
Output Voltage:
When 3.3 V is Used with Driving Ability Set to "Normal Output"</td><td>
Table 38.7 DC Characteristics - Output Voltage: When 3.3 V is Used with Driving Ability Set to "Normal Output": Description corrected.
Error:
<table>
<tr><th colspan="2">Item</th><th>Symbol</th><th>Min.</th><th>Unit</th></tr>
<tr><td rowspan="2">Output high-level voltage (normal output)*</td><td>PA0 to PA15, PB0 to PB6, PC0 to PC15, PD0 to PD15, PE0 to PE15, PF0 to PF5, PG0 to PG7</td><td>VOH</td><td>Vcc –0.5</td><td>V</td></tr>
<tr><td>PH0 to PH15, PJ0 to PJ15, PK0 to PK14, PL0 to PL9</td><td></td><td>PVcc –0.5</td><td>V</td></tr>
</table>
Correct:
<table>
<tr><th colspan="2">Item</th><th>Symbol</th><th>Min.</th><th>Unit</th></tr>
<tr><td rowspan="2">Output high-level voltage (normal output)*</td><td>PA0 to PA15, PB0 to PB6, PC0 to PC15, PD0 to PD15, PE0 to PE15, PF0 to PF5, PG0 to PG7</td><td>VOH</td><td>Vcc –1.1</td><td>V</td></tr>
<tr><td>PH0 to PH15, PJ0 to PJ15, PK0 to PK14, PL0 to PL9</td><td></td><td>PVcc –1.1</td><td>V</td></tr>
</table>
Error:
<table>
<tr><th colspan="2">Item</th><th>Symbol</th><th>Max.</th><th>Unit</th></tr>
<tr><td rowspan="2">Output low-level voltage (normal output)*</td><td>PA0 to PA15, PB0 to PB6, PC0 to PC15, PD0 to PD15, PE0 to PE15, PF0 to PF5, PG0 to PG7</td><td>VOL</td><td>0.4</td><td>V</td></tr>
<tr><td>PH0 to PH15, PJ0 to PJ15, PK0 to PK14, PL0 to PL9</td><td></td><td>0.4</td><td>V</td></tr>
</table>
Correct:
<table>
<tr><th colspan="2">Item</th><th>Symbol</th><th>Max.</th><th>Unit</th></tr>
<tr><td rowspan="2">Output low-level voltage (normal output)*</td><td>PA0 to PA15, PB0 to PB6, PC0 to PC15, PD0 to PD15, PE0 to PE15, PF0 to PF5, PG0 to PG7</td><td>VOL</td><td>0.9</td><td>V</td></tr>
<tr><td>PH0 to PH15, PJ0 to PJ15, PK0 to PK14, PL0 to PL9</td><td></td><td>0.9</td><td>V</td></tr>
</table>
</td></tr>
<tr><td>Adds by Rev.C</td><td>38-14</td><td>Table 38.16
Power-On/Off Timing</td><td>
Table 38.16 Power-On/Off Timing: Description of item corrected.
Error:
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>Vdd holding time at Vcc shutdown</td><td>tVDDH</td><td>-</td><td>0</td><td>us</td><td>38.4</td></tr>
</table>
Correct:
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>Vcc holding time at Vdd shutdown</td><td>tVDDH</td><td>-</td><td>0</td><td>us</td><td>38.4</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th>Contents</th></tr>
<tr><td>Adds by Rev.C</td><td>38-15</td><td>Figure 38.5
Operation Mode and Oscillation Timing at Power-On/Off</td><td>Figure 38.5 Operation Mode and Oscillation Timing at Power-On/Off: Symbol added.
Error:
 

Correct:
 
</td></tr>
<tr><td>Adds by Rev.C</td><td>38-33</td><td>Table 38.26 RSPI Timing</td><td>Table 38.26 RSPI Timing: Description of Figures corrected.
Error:
<table>
<tr><th colspan="2">Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td rowspan="2">SSL rise/fall time</td><td>Output</td><td rowspan="2">t_{SSLR}, t_{SSLF}</td><td>-</td><td>8</td><td>ns</td><td rowspan="2">38.28, 38.29</td></tr>
<tr><td>Input</td><td>-</td><td>1</td><td>us</td></tr>
</table>
Correct:
<table>
<tr><th colspan="2">Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td rowspan="2">SSL rise/fall time</td><td>Output</td><td rowspan="2">t_{SSLR}, t_{SSLF}</td><td>-</td><td>8</td><td>ns</td><td rowspan="2">38.28 to 38.31</td></tr>
<tr><td>Input</td><td>-</td><td>1</td><td>us</td></tr>
</table></td></tr>
</table>

Rev.	Page	Part	Contents
Adds by Rev.C	38-35	Figure 38.30 RSPI Timing (Slave, CPHA = "0")	Figure 38.30 RSPI Timing (Slave, CPHA = "0"): Waveform of SSL corrected. tSSLR and tSSLF added. Error:  Correct: 
Adds by Rev.C	38-36	Figure 38.31 RSPI Timing (Slave, CPHA = "1")	Figure 38.31 RSPI Timing (Slave, CPHA = "1"): Waveform of SSL corrected. tSSLR and tSSLF added. Error:  Correct: 

<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th>Contents</th></tr>
<tr><td>Adds by Rev.C</td><td>38-38</td><td>Table 38.29 DRI Timing (When Special Mode is On)</td><td>
Table 38.29 DRI Timing (When Special Mode is On): Description of Min. corrected.
Error:
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>Minimum DIN edge count at DINI initialization level in delayed reset mode (minimum width at initialization level)</td><td>tWDLYDIN1</td><td>8 tc(CAP)*1</td><td>-</td><td></td><td>38.33 to 38.36</td></tr>
</table>
Correct:
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>Minimum DIN edge count at DINI initialization level in delayed reset mode (minimum width at initialization level)</td><td>tWDLYDIN1</td><td>8 tc(DCAP)*1</td><td>-</td><td></td><td>38.33 to 38.36</td></tr>
</table>
</td></tr>
<tr><td>Adds by Rev.C</td><td>38-39</td><td>Figure 38.34 Edge Detection Timing (Edge Interval to Prevent DRI Internal Simultaneous Edge Detection Timing)</td><td>
Figure 38.34 Edge Detection Timing (Edge Interval to Prevent DRI Internal Simultaneous Edge Detection Timing): Description corrected.
Error:


Correct:


</td></tr>
<tr><td>Adds by Rev.C</td><td>G-114</td><td>Table G.1 Register Assignments</td><td>
Table G.1 Register Assignments: Description corrected.
Error:
<table>
<tr><th rowspan="2">Address</th><th>+0 Address</th><th>+1 Address</th><th>+2 Address</th><th>+3 Address</th><th rowspan="2">Access Size</th></tr>
<tr><th>31 to 24 bit</th><th>23 to 16 bit</th><th>15 to 8 bit</th><th>7 to 0 bit</th></tr>
<tr><td>H'FFFF E958</td><td>TOU33 Reload Register (TO33RLD)</td><td></td><td></td><td></td><td>32</td></tr>
</table>
Correct:
<table>
<tr><th rowspan="2">Address</th><th>+0 Address</th><th>+1 Address</th><th>+2 Address</th><th>+3 Address</th><th rowspan="2">Access Size</th></tr>
<tr><th>31 to 24 bit</th><th>23 to 16 bit</th><th>15 to 8 bit</th><th>7 to 0 bit</th></tr>
<tr><td>H'FFFF E958</td><td colspan="4">TOU33 Reload Register(TO33RLD)</td><td>32</td></tr>
</table>
</td></tr>
</table>