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RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A781B/E	Rev.	2.00
Title	SH7450 Group, SH7451 Group Hardware Manual Errata Rev.B		Information Category	Technical Notification		
Applicable Product	SH7450 Group, SH7451 Group	Lot No.	Reference Document	SH7450 Group, SH7451 Group Hardware Manual REV.1.00 (REJ09B0454-0100)		

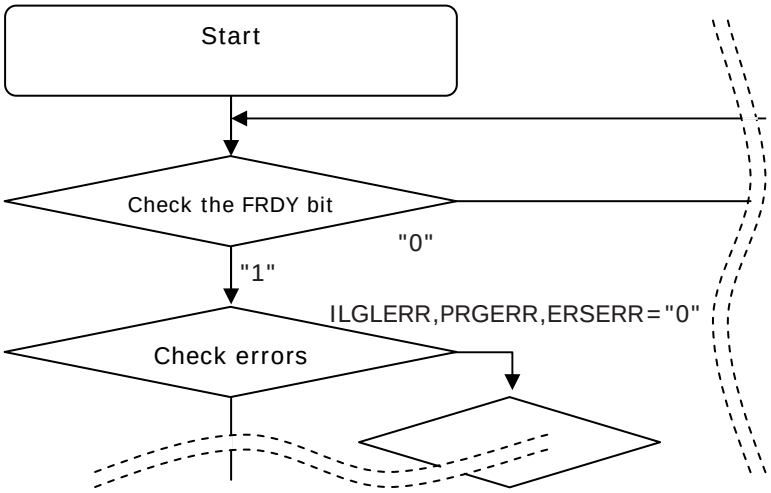
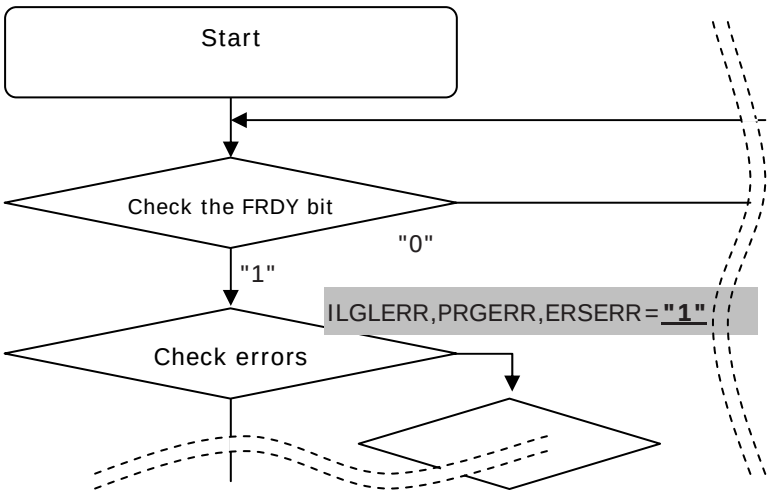
Since we changed the following contents of "TN-SH7-A781 A/J:SH7450 Group and SH7451 Group hardware manual Errata Rev.A(Technical update published on September 6, 2010)", we announce you.

[The contents of change]

- Rearrange chapter number and section number of written items in ascending order. (The contents of each item is the same)
- Specify sign and figure in "Fig.38.4 Power-On/Off Timing". (Each regulation is the same)

Appending Document:"SH7450 Group and SH7451 Group hardware manual REV.1.00" errata REV.B – 2sheets

* In the following, the portion of net credit (■) or an underline is a portion with an addition/change.

Rev.	Page	Part		Contents
Adds by REV.A.	11-1	Section 11 Address Space	Error	Figures 11.1 to 11.6 show this MCU address space. This MCU has a 32-bit (4-Gbyte) physical address space. Internal ROM, internal RAM (SHwyRAM), external address spaces are mapped onto the highest 512 Mbytes (H'0000 0000 to H'1FFF FFFF). IL memory, OL memory, and other internal resources are mapped onto the lowest 512 Mbytes (H'E000 0000 to H'FFFF FFFF).
			Correction	Figures 11.1 to 11.6 show this MCU address space. This MCU has a 32-bit (4-Gbyte) physical address space. Internal ROM, internal RAM (SHwyRAM), external address spaces are mapped onto the **lowest** 512 Mbytes (H'0000 0000 to H'1FFF FFFF). IL memory, OL memory, and other internal resources are mapped onto the **highest** 512 Mbytes (H'E000 0000 to H'FFFF FFFF).
Adds by REV.A.	12-25	Section 12 ROM 12.6.3 FCU Command Usage Figure 12.10 Procedure for Transition to ROM Read Mode	Error	
			Correction	
Adds by REV.A.	25-33	Section 25 I2C Bus Interface 3 (IIC3) 25.8 Usage Notes 25.8.10	Add	25.8.10 regarding master receive mode of I2C-bus interface mode When stop condition generation or start condition regeneration overlaps with the falling edge of the ninth clock cycle of the SCL signal, an additional cycle is output after the ninth clock cycle. After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of the SCL signal and generate a stop condition or regenerate a start condition. Confirm the falling edge of the ninth clock cycle of the SCL signal as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

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38.2 DC Characteristics

Low level input voltage</td><td>Error</td><td>
Table 38.3 DC Characteristics - Input Level Voltage: When 5 V is Used
<table>
<tr><th colspan="3">Item</th><th>Symbol</th><th colspan="3">Rating</th><th>Unit</th></tr>
<tr><th></th><th></th><th></th><th></th><th>Min.</th><th>Typ.</th><th>Max.</th><th></th></tr>
<tr><td>Low level input voltage</td><td>Pins without threshold value switching function</td><td>EXTAL</td><td>VIL</td><td>0</td><td></td><td>0.25 Vcc</td><td>V</td></tr>
</table>
</td></tr>
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<tr><td>Low level input voltage</td><td>Pins without threshold value switching function</td><td>EXTAL</td><td>VIL</td><td>0</td><td></td><td>0.125 Vcc</td><td>V</td></tr>
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38.3 AC Characteristics

38.3.1 Power-On/Off Timing</td><td>Error</td><td>
Table 38.16 Power-On/Off Timing
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr>
<tr><td>PVcc voltage at power off</td><td>VCCL</td><td>0</td><td>1.0</td><td>V</td><td>38.4</td></tr>
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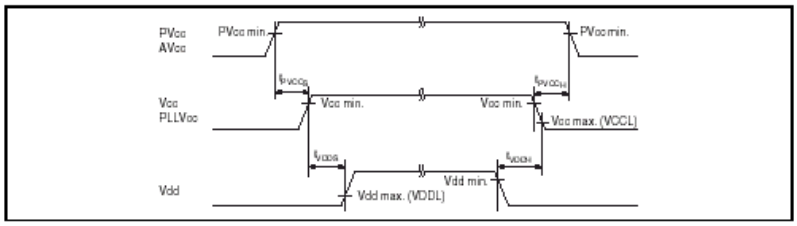

Figure 38.4 Power-On/Off Timing
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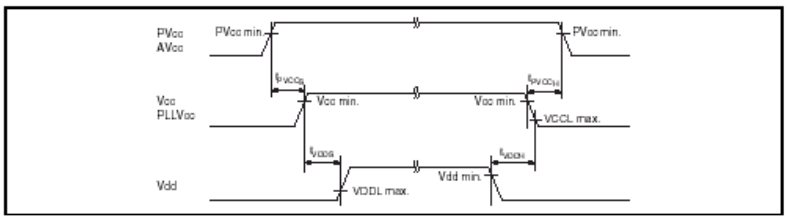

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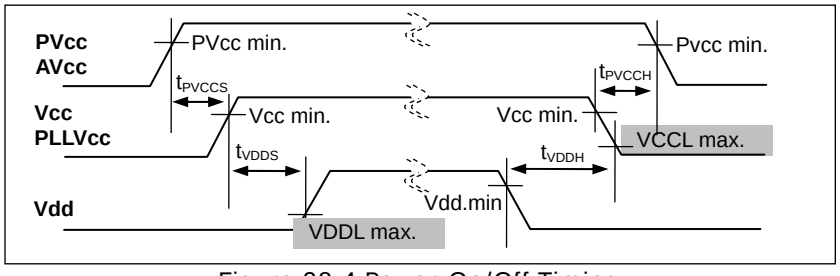
38.3 AC Characteristics

38.3.1 Power-On/Off Timing</td><td>Replacement (Specify sign and figure)</td><td>


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