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RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A781A/E	Rev.	1.00
Title	SH7450 Group, SH7451 Group Hardware Manual Errata Rev.A		Information Category	Technical Notification		
Applicable Product	SH7450 Group, SH7451 Group	Lot No.	Reference Document	SH7450 Group, SH7451 Group Hardware Manual REV.1.00 (REJ09B0454-0100)		

Since we corrected the contents of "SH7450 group and SH7451 group hardware manual REV.1.00 (Publish in January, 2010)", we announce you.

Please use attached errata for "SH7450 group and SH7451 group hardware manual REV.1.00" in the case of use.

Appending Document:"SH7450 group and SH7451 group hardware manual REV.1.00" errata Rev.A ... 2 sheets.

<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th></th><th>Contents</th></tr>
<tr><td rowspan="2">REV.A</td><td rowspan="2">11-1</td><td rowspan="2">Section 11
Address Space</td><td>Error</td><td>Figures 11.1 to 11.6 show this MCU address space. This MCU has a 32-bit (4-Gbyte) physical address space. Internal ROM, internal RAM (SHwyRAM), external address spaces are mapped onto the highest 512 Mbytes (H'0000 0000 to H'1FFF FFFF). IL memory, OL memory, and other internal resources are mapped onto the lowest 512 Mbytes (H'E000 0000 to H'FFFF FFFF).</td></tr>
<tr><td>Correction</td><td>Figures 11.1 to 11.6 show this MCU address space. This MCU has a 32-bit (4-Gbyte) physical address space. Internal ROM, internal RAM (SHwyRAM), external address spaces are mapped onto the <u>lowest</u> 512 Mbytes (H'0000 0000 to H'1FFF FFFF). IL memory, OL memory, and other internal resources are mapped onto the <u>highest</u> 512 Mbytes (H'E000 0000 to H'FFFF FFFF).</td></tr>
<tr><td rowspan="2">REV.A</td><td rowspan="2">38-4</td><td rowspan="2">Section 38
Electrical Characteristics

38.2 DC Characteristics

Low level input voltage</td><td>Error</td><td>Table 38.3 DC Characteristics - Input Level Voltage: When 5 V is Used
<table><tr><th colspan="3">Item</th><th>Symbol</th><th>Rating</th><th></th><th></th><th>Unit</th></tr><tr><th></th><th></th><th></th><th></th><th>Min.</th><th>Typ.</th><th>Max.</th><th></th></tr><tr><td>Low level input voltage</td><td>Pins without threshold value switching function</td><td>EXTAL</td><td>VIL</td><td>0</td><td></td><td>0.25 Vcc</td><td>V</td></tr></table></td></tr>
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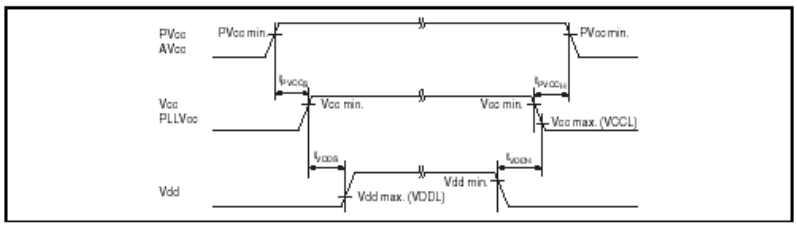
<tr><td rowspan="2">REV.A</td><td rowspan="2">38-14</td><td rowspan="2">Section 38
Electrical Characteristics

38.3 AC Characteristics

38.3.1 Power-On/Off Timing</td><td>Error</td><td>Table 38.16 Power-On/Off Timing
<table><tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr><tr><td>PVcc voltage at power off</td><td>VCCL</td><td>0</td><td>1.0</td><td>V</td><td>38.4</td></tr></table>  Figure 38.4 Power-On/Off Timing</td></tr>
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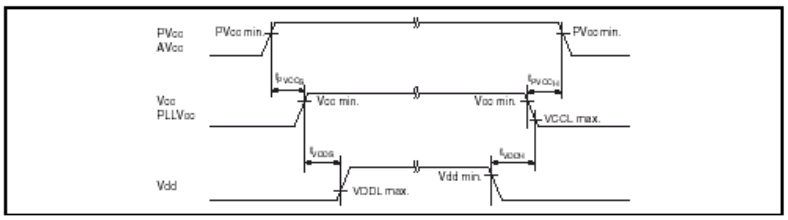
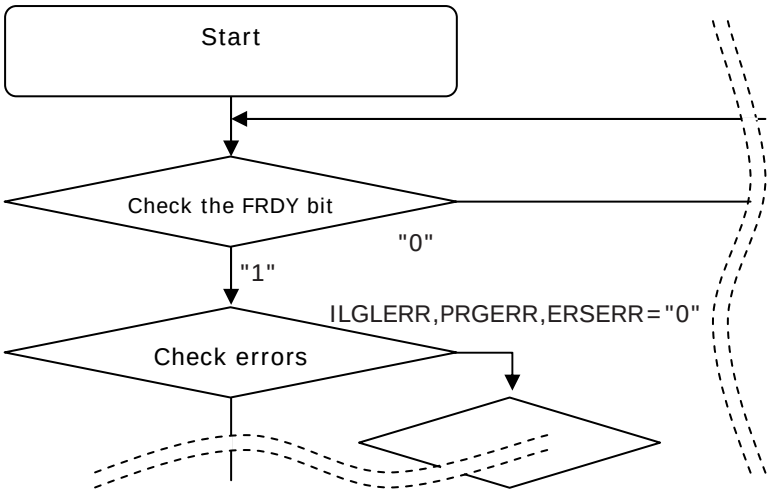
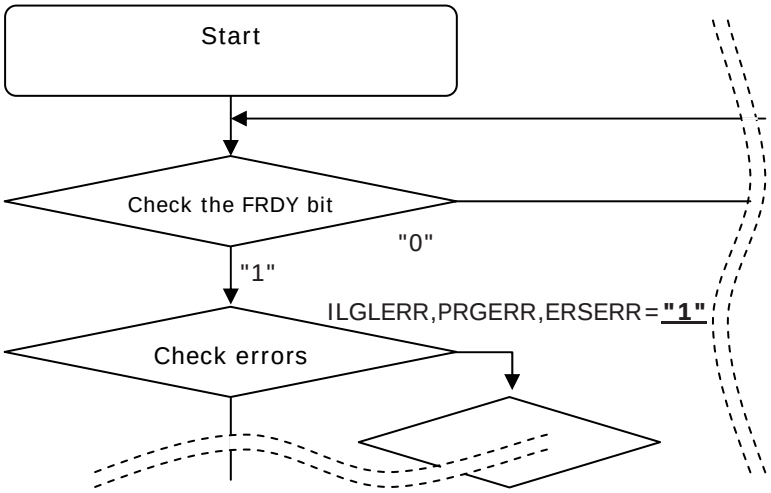
<table><tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figures</th></tr><tr><td>Vcc voltage at power off</td><td>VCCL</td><td>0</td><td>1.0</td><td>V</td><td>38.4</td></tr></table>  Figure 38.4 Power-On/Off Timing</td></tr>
</table>

<table>
<tr><th>Rev.</th><th>Page</th><th>Part</th><th></th><th>Contents</th></tr>
<tr><td>REV.A</td><td>25-33</td><td>Section 25
I2C Bus
Interface 3
(IIC3)

25.8 Usage
Notes

25.8.10</td><td>Add</td><td>25.8.10 regarding master receive mode of I2C-bus interface mode
When stop condition generation or start condition regeneration overlaps with the falling edge of the ninth clock cycle of the SCL signal, an additional cycle is output after the ninth clock cycle.
After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of the SCL signal and generate a stop condition or regenerate a start condition. Confirm the falling edge of the ninth clock cycle of the SCL signal as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.</td></tr>
<tr><td rowspan="2">REV.A</td><td rowspan="2">12-25</td><td rowspan="2">Section 12 ROM

12.6.3 FCU
Command
Usage

Figure 12.10
Procedure for
Transition to
ROM Read Mode</td><td>Error</td><td> 
</td></tr>
<tr><td>Correction</td><td> 
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