To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	MCU			No	TN-SH7-420A/E	Rev	1
THEME	On SH7065 usage notices of MMT		Classification of Information	1. Spec change 2. Supplement of Documents (3.) Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	HD64F7065AF60 HD6437065AF60 HD64E7060S	Lot No. ALL	Reference Documents	SH7065 Hardware manual Rev.4.0 (ADE-602-166C)		Effective Date Permanent	

1. Additional notices onto「usage notice」

Two notices ((3), and (4) written below) are added to「11.6 Usage Notice」in hardware manual.

(3) Pay attention to the notices below, when a value is written into the Timer General Register U (TGRU), Timer General Register V (TGRV), Timer General Register W (TGRW), and in case of written into free operation address (*).

• Incase of Count UP: Do not write a value「Previous value of TGRU + Td」into TGRU.

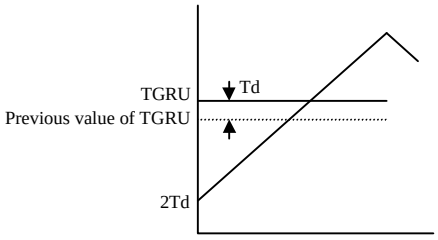
• Incase of Count DOWN: Do not write a value「Previous value of TGRU - Td」into TGRU.

In the same manner to TGRV, and TGRW.

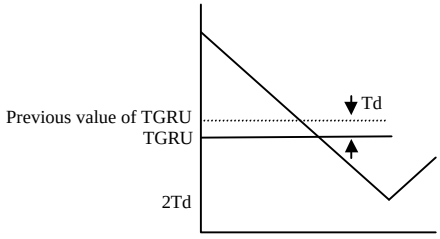
When a value「Previous value of TGRU + Td」is written (in case of Count DOWN「Previous value of TGRU - Td」), the output of PUOA/PUOB, PVOA/PVOB, PWOA/PWOB (corresponding to U, V, W phase) may not be output for 1 cycle.

Below figures show the error case.

*: when addresses, H'FFFF049C, H'FFFF04AC, H'FFFF04BC are used as register address for TBRU,TBRV, TBRW, respectively.



Case of count Up



Case of count Down

(4) On a writing operation into Timer Period Data Register(TPDR), and Timer Dead Time Data Register(TDDR), when MMT is operating.

• Do not revise TPDR register when MMT is operating. Always use a buffer-write operation through TPBR register.

• Do not revise TDDR register once an operation of MMT is invoked. When TDDR is revised, a wave may not be output for as much as 1 cycle (full count period of 16 bits in TDCNT), because a value cannot be written into TDCNT, which is compared to a value set in TDDR.