HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	15 November 2000	No.	TN-SH7-278A/E
THEME	SH3, SH3-DSP An error in writing of "Mask All Interrupts (MAI) bit"		
CLASSIFICATION	☐ Spec. change ☐ Limitation on Use ■ Supplement of Documents		
PRODUCT NAME	SH7707, SH7709, SH7709A, SH7729		
REFERENCE DOCUMENTS	Hardware Manual s SH7707: ADE-602-137 Rev.1.0, SH7709: ADE-602-123B Rev.2.0 , SH7709A: ADE-602-187B Rev.3.0, SH7729: ADE-602-157A Rev.2.0	Effective Date From	Eternity Now

Hardware Manuals for SH7707,SH7709,SH7709A and SH7729 have following error of description.

SH7707 Manual(Rev1.0 or older): 6.3.3 Interrupt Control Register1 (ICR1)
SH7709 Manual(Rev2.0 or older): 6.3.3 Interrupt Control Register1 (ICR1)
SH7709A Manual(Rev3.0 or older): 6.3.3 Interrupt Control Register1 (ICR1)
SH7729 Manual(Rev2.0 or older): 6.3.3 Interrupt Control Register1 (ICR1)

Error:

Bit 15-Mask All Interrupts (MAI): Mask NMI interrupts when set to 1. Also selects whether or not all interrupt requests are masked when a low level is being input to the NMI pin.

Bit 15: MAI	**Description**	
0	All interrupt requests are not masked	(Initial value)
1	All interrupt requests are masked	

Correction:

Bit 15-Mask All Interrupts (MAI): When it is set to 1, all interrupt requests are masked when a low level is being input to the NMI pin. And it also mask NMI interrupt in standby mode.

Bit 15: MAI	**Description**	
0	When NMI pin is low level, all interrupt requests are not masked	(Initial value)
1	When NMI pin is low level, all interrupt requests are masked	