To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPD

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Product Category	MPU&MCU		Document No.	TN-SH7-A473B/E	Rev.	2.0
Title	A SH3 and SH3-DSP usage notice on the IRQ edge interrupt		Information Category	Technical Notification		
Applicable Product	SH7729R SH7709S SH7706 SH7727	Lot No. All Lots	Reference Document	SH7729R hardware manual (REJ09B0091-0500O Rev.5.00) SH7709S hardware manual (REJ09B0081-0500O Rev.5.00) SH7706 hardware manual (REJ09B0146-0400O Rev.4.00) SH7727 hardware manual (ADE-602-209C Rev.4.0)		

SH7709S, SH7729R, SH7727 and SH7706 have followed usage notice on the IRQ edge interrupt mode.

This technical update supplements “TN-SH7-473A/E” by the underlined part as follows.

1. Phenomenon

When the Interrupt Request Register 0 (IRR0) is read and the IRQnR bits (n=0~5) are set at the same time, the read value of the IRQnR bits are “0”, however the IRQnR bits are read as “1” internally. Thus the IRQnR bits will be cleared when they will be written as “0”.

Our original specification was that the IRQnR bits are cleared only when they are read after they are set to “1”. However this particular case does not meet the original specification.

The errata will be the problem in the following sequence.

(1) IRR0 is read in the IRQn interrupt handler

(2) IRQm(m is not equal n) edge interrupt is input at the same time with (1)

(3) The read value of the IRQnR is “1” and the read value of the IRQmR is “0” at the read (1)

(4) Write H’00 in the IRR0 in order to clear the IRQnR bit.

(5) The IRQnR bit and the IRQmR bit are cleared (the write at (4) does not intend to clear the IRQmR bits)

(6) The IRQm interrupt is cleared because of the write at (4)

2. Work around

When you use the IRQ interrupt as edge mode, please use the following note.

Note:

When clearing an IRQ5R - IRQ0R bit to 0, checking that perform read-out from IRR0 before writing, and the bit concerned to clear is set to 1, and then write 0. In this case, 0 should be written only to the bits to be cleared and 1 to the other bits. The contents of the bits to which 1 is written do not change.