To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU	Document No.	TN-SH7-A604A/E	Rev.	1.00
Title	SDRAM Initialization Sequence Setting Procedure for SH7261/SH7201 Products		Information Category	Technical Notification	
Applicable Products	SH7261/SH7201 products	Lot No. All lots	Reference Document	SH7261 Group Hardware Manual Rev.1.00 REJ09B0320-0100 SH7201 Group Hardware Manual Rev.1.00 REJ09B0321-0100	

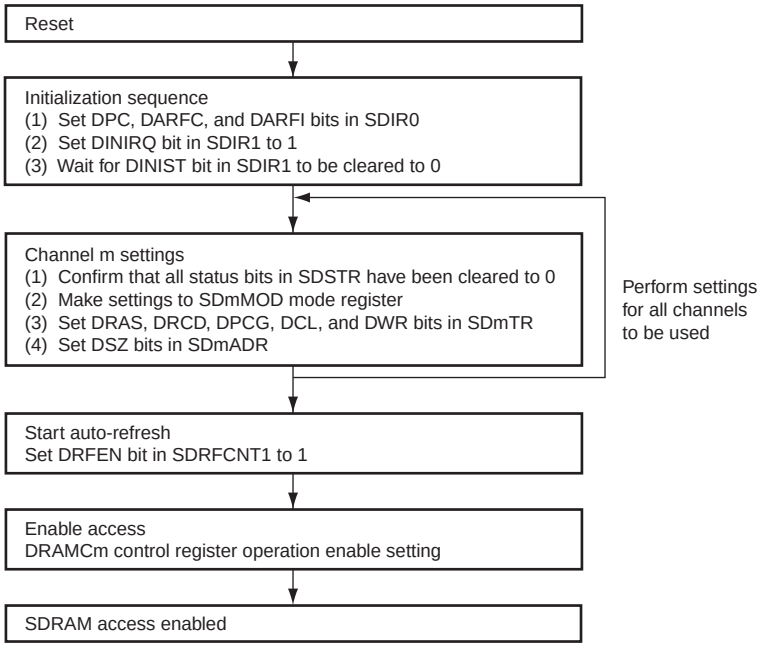
We would like to inform you of the discrepancy found between the specification of the SDRAM initialization sequence described in the SH7261 Group Hardware Manual (Rev. 1.0) and SH7201 Group Hardware Manual (Rev. 1.0) and the operation of this LSI.

The SH7261 Group and SH 7201 Group products include the initialization sequencer function for initializing SDRAM. The initialization sequence is performed after a reset or after a recovery from deep-power-down mode. The initialization sequence after a reset is performed in accordance with the procedure in figure 9.24 in (a) SDRAMC Setting Procedure in (12) SDRAMC Setting Examples in section 9.5.2, SDRAM Interface. In the initialization sequence performed after a reset, the discrepancy between the specification and the operation of this LSI was found. In the initialization sequence, the precharge-all-banks command (PRA) is issued for SDRAM according to the specification. However, when operating this LSI in accordance with the procedure in figure 9.24, the precharge-select-banks command (PRE) is issued (bank 0 is selected at this time). Although a high level must be output from the A12 pin to issue the PRA, a low level is output. This causes the PRE to be issued.

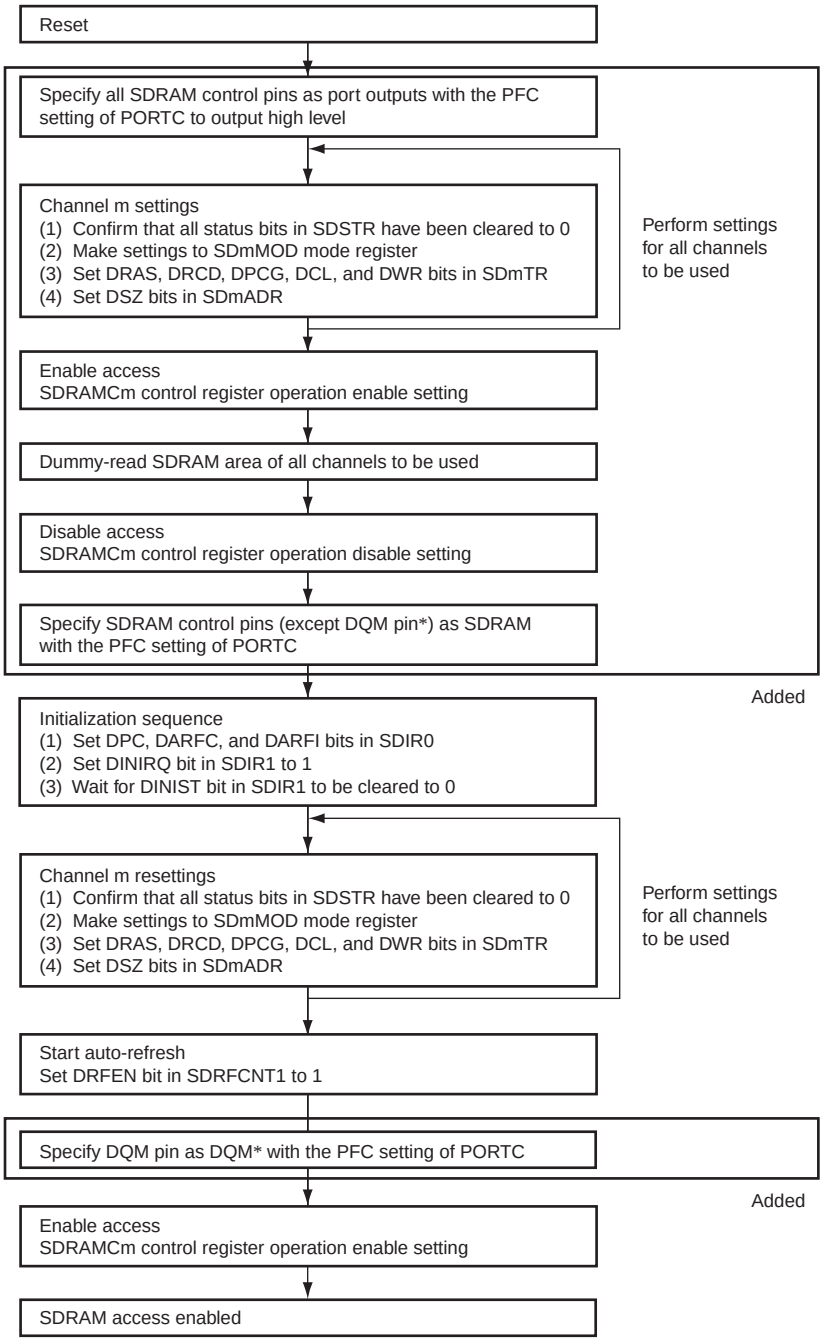
The SDRAM setting procedure is described as below to issue the PRA appropriately in the initialization sequence after a reset.

Figure 9.24 SDRAMC Setting Procedure (page 266 for SH7261 and page 262 for SH7201)

[Before Correction]



[After Correction]



Note: * It is recommended that the DQM pin be driven high before the initialization sequence for some SDRAM. In this case, the setting may be necessary.

The PRA can be issued in the initialization sequence after a reset as described in the specification by following the above setting procedure.

In addition, it is recommended that the DQM pin be driven high before the initialization sequence for some SDRAM. The setting to support this is added to this SDRAM setting procedure.

Note that the specification of the power-up sequence may vary depending on the SDRAM used. Study the SDRAM specifications in detail before making system settings.