RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU			Document No.	TN-RZ*-A054A/E	Rev.	1.00
Title	RZ/T1 Group User's Manual: Hardware Restriction on the write value of RSPI status register			Information Category	Technical Notification		
Applicable Product	RZ/T1 Group	Lot No.		Reference Document	RZ/T1 Group User's Manual: Hardware Rev1.40 R01UH0483EJ0140 Rev.1.40		
		All lots					

There is a restriction on the write value of the RSPI Status Register (SPSR) of RSPIa. When the wrong value is set, unintentional transmission occurs or the RSPI Data Register (SPDR) value is undefined. The following describes restriction and correction of User's Manual Hardware.

1. Condition:

   When the bit 5 or bit 7 of reserved bits of the SPSR is set to 0 while the SPE bit of the

   RSPI Control Register (SPCR) is 1 (RSPI function is enabled).

2. Phenomenon

   When the bit 5 of the SPSR register is set to 0, there is a possibility that unintentional transmission occurs.

   And when the bit 7 is set to 0, there is a possibility that the SPDR register value is undefined.

3. Workaround

   The write value should be 1 on the bit 5 and bit 7 of the SPSR register.

   And although it has no effect on the operation, the write value should be 0 on the bit 4 and bit 6.

4.   Correction

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[Current description]
36.2.4 RSPI Status Register (SPSR)

Bit	Symbol	Bit Name	Description	R/W
b4	—	Reserved	This bit is read as 0.	R
b5	—	Reserved	The read value is undefined.	R
b6	—	Reserved	This bit is read as 0.	R
b7	—	Reserved	The read value is undefined.	R

[Correct description]
36.2.4 RSPI Status Register (SPSR)

Bit	Symbol	Bit Name	Description	R/W
b4	—	Reserved	This bit is read as 0. **The write value should be 0.**	R**/(W)**
b5	—	Reserved	The read value is undefined. **The write value should be** 1.	R**/(W)**
b6	—	Reserved	This bit is read as 0. **The write value should be 0.**	R**/(W)**
b7	—	Reserved	The read value is undefined. **The write value should be 1.**	R**/(W)**