Date: May 15, 2024

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0134A/E	Rev.	1.00
Title	RZ/G2N Additional Explanations for Pin Multiplex		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2N	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 Dedicated document for Pin Multiplex of RZ/G2N (EPMP-IMB-20-0059)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Additional explanations for "RZ/G Series, 2nd Generation User's Manual: Rev.1.11 Dedicated document for Pin Multiplex of RZ/G2N.

Note: The pin function list reflected the changes of this technical update is attached to this document.

[Priority level]

Importance: "Normal"

Urgency: "Normal"

[Products]

RZ/G2N

[Section number and title]

Dedicated document for Pin Multiplexing [RZ/G2N]

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. (Dedicated section). Pin Multiplexing [RZ/G2N],

(*1) after negate PRESET#, pin state is L output and then change to High output.
regarding transition timing, please refer to the Reset section of H/W manual.

(*3) output value is H or L. this value depends on each chip.
(*4) depends on MD21,MD20,MD11,MD10,MDT[1:0] setting
(*5) depends on MD21,MD20,MD11,MD10,MDT[1:0] setting, in case JTAG interface is selected, "pullup" is selected.
In case of other settings, "*"(pullup on/off is controlable in PFC register. Initial state is pullup off) is selected.
(*10) The initial value is [drv2:drv1] = H'3.
(*11) The initial value is [drv3:drv2:drv1] = H'7.
(*16) In case of MD[4:1] = B'001x or B'101x (x: don't care), pin states of the QSPI1_SPCLK and QSPI1_SSL are as follows;
– During RPC_RESET# is low level, QSPI1_SPCLK is low output and QSPI1_SSL is high output.
– During RPC_RESET# is high level, QSPI1_SPCLK is high output and QSPI1_SSL is Hi-Z.

[pullup/pulldown control definition of pin]
pullup* : pullup on/off is controlable in PFC register. Initial state is pullup on
* : pullup on/off is controlable in PFC register. Initial state is pullup off
- : no pullup/pulldown
pulldown* : pulldown on/off is controlable in PFC register. Initial state is pulldown on

[symbol definition in "Handling when the Pin is not in Use"]
- : pin must be in use

Pin condition at PRESET#=L (PRESET#=L時の端子状態)		Pin condition after power-on reset deasert				IO	drivability	pull-up/down controlled	schmitt	Power		Handling when the Pin is not in Use
		MD[4:1]=0000		MD[4:1]=others								
initial pin setting	state	initial pin setting	state	initial pin setting	state					Domain	Voltage	
USB3HS0_DP	Z	USB3HS0_DP	Z	USB3HS0_DP	Z					VDDQ33_USB3HS0	3.3V	open
USB3HS0_DM	Z	USB3HS0_DM	Z	USB3HS0_DM	Z					VDDQ33_USB3HS0	3.3V	open
USB3HS0_ID	Z	USB3HS0_ID	Z	USB3HS0_ID	Z					VDDQ33_USB3HS0	3.3V	open
USB3HS0_VBUS	Z	USB3HS0_VBUS	Z	USB3HS0_VBUS	Z					-	-	open
										VDD09_USB3HS0	0.8V	Power input
										VDDQ33_USB3HS0	3.3V	Power input
										VDDQ33_USB3HSH	3.3V	Power input
USB_EXTAL	I	USB_EXTAL	I	USB_EXTAL	I	I	-	-	-	VDDQ18	1.8V	open
USB_XTAL	O	USB_XTAL	O	USB_XTAL	O	O	-	-	-	VDDQ18	1.8V	open
ID0	Z	ID0	Z	ID0	Z					VDDQ33_USB2	3.3V	open
VBUS0	Z	VBUS0	Z	VBUS0	Z					-	-	open
DP0	z	DP0	z	DP0	z					VDDQ33_USB2	3.3V	open
DM0	Z	DM0	Z	DM0	Z					VDDQ33_USB2	3.3V	open
TXRTUNE0	-	TXRTUNE0	-	TXRTUNE0	-					-	-	open
										VDD09_USB20	0.8V	Power input
										VDDQ33_USB2H0	3.3V	Power input
										VDDQ33_USB2	3.3V	Power input
ID1	Z	ID1	Z	ID1	Z					VDDQ33_USB2	3.3V	open
DP1	Z	DP1	Z	DP1	Z					VDDQ33_USB2	3.3V	open

Current (to):

(*1) after negate PRESET#, pin state is L output and then change to High output.
regarding transition timing, please refer to the Reset section of H/W manual.

(*3) output value is H or L. this value depends on each chip.
(*4) depends on MD21,MD20,MD11,MD10,MDT[1:0] setting
(*5) depends on MD21,MD20,MD11,MD10,MDT[1:0] setting, in case JTAG interface is selected, "pullup" is selected.
In case of other settings, "*"(pullup on/off is controlable in PFC register. Initial state is pullup off)
is selected.
(*10) The initial value is [drv2:drv1] = H'3.
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– During RPC_RESET# is low level, QSPI1_SPCLK is low output and QSPI1_SSL is high output.
– During RPC_RESET# is high level, QSPI1_SPCLK is high output and QSPI1_SSL is Hi-Z.

[pullup/pulldown control definition of pin]
pullup* : pullup on/off is controlable in PFC register. Initial state is pullup on
* : pullup on/off is controlable in PFC register. Initial state is pullup off
- : no pullup/pulldown
pulldown* : pulldown on/off is controlable in PFC register. Initial state is pulldown on
[symbol definition in "Handling when the Pin is not in Use"]
- : pin must be in use

(*17) The USB data pins have their own pull pull-up/down control function.
Affected pins are as follows: USB3HS0_DP and USB3HS0_DM and DPn, DMn DMn. (n=0, 1). For more information,
see Chapters 60.2, 60.7 to 60.8 and Chapters 61.2 to 61.3.
The processing of the USB USB-Data pins on the PCB must be designed in accordance with the PCB guidelines described
in "Design Guidelines for Serial Interface Printed Circuit Boards with RZ/G2 Series Products".
Please contact Renesas Electronics Corporation for details about the Design Guidelines.

Pin condition at PRESET#=L (PRESET#=L時の端子状態)		Pin condition after power-on reset deasert				IO	drivability	pull-up/down controlled	schmitt	Power		Handling when the Pin is not in Use
		MD[4:1]=0000		MD[4:1]=others								
initial pin setting	state	initial pin setting	state	initial pin setting	state					Domain	Voltage	
USB3HS0_DP	Z	USB3HS0_DP	Z	USB3HS0_DP	Z			(*17)		VDDQ33_USB3HS0	3.3V	open
USB3HS0_DM	Z	USB3HS0_DM	Z	USB3HS0_DM	Z			(*17)		VDDQ33_USB3HS0	3.3V	open
USB3HS0_ID	Z	USB3HS0_ID	Z	USB3HS0_ID	Z					VDDQ33_USB3HS0	3.3V	open
USB3HS0_VBUS	Z	USB3HS0_VBUS	Z	USB3HS0_VBUS	Z					-	-	open
										VDD09_USB3HS0	0.8V	Power input
										VDDQ33_USB3HS0	3.3V	Power input
										VDDQ33_USB3HSH	3.3V	Power input
USB_EXTAL	I	USB_EXTAL	I	USB_EXTAL	I	I	-	-	-	VDDQ18	1.8V	open
USB_XTAL	O	USB_XTAL	O	USB_XTAL	O	O	-	-	-	VDDQ18	1.8V	open
ID0	Z	ID0	Z	ID0	Z					VDDQ33_USB2	3.3V	open
VBUS0	Z	VBUS0	Z	VBUS0	Z					-	-	open
DP0	z	DP0	z	DP0	z			(*17)		VDDQ33_USB2	3.3V	open
DM0	Z	DM0	Z	DM0	Z			(*17)		VDDQ33_USB2	3.3V	open
TXRTUNE0	-	TXRTUNE0	-	TXRTUNE0	-					-	-	open
										VDD09_USB20	0.8V	Power input
										VDDQ33_USB2H0	3.3V	Power input
										VDDQ33_USB2	3.3V	Power input
ID1	Z	ID1	Z	ID1	Z					VDDQ33_USB2	3.3V	open
DP1	Z	DP1	Z	DP1	Z			(*17)		VDDQ33_USB2	3.3V	open
DM1	Z	DM1	Z	DM1	Z			(*17)		VDDQ33_USB2	3.3V	open

[Description]

Note (*17) for the USB data pins is added.

[Reason for Correction]

General error correction.

To avoid misunderstanding about IP pins internal pull-up/pull-down control.

End of Document -