Date: Jun. 2, 2022

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0089A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, V3.0, G2N and G2E Specification Changes for DU Electrical Characteristics		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Specification Changes for “RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 73.13 Display Unit (DU)

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“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 73.13. DU, Page 73-60,73-61 Table 73.13.2 Display Signal Timing, tDD3, tDD3f and related descriptions are removed.

Current (from):

Table 73.13.2 Display Signal Timing

Conditions: VDDQ33 = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] / ± 0.3 V[RZ/G2E],
GND = VSS = 0 V,
Tc = -40 to +115 °C, [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 20 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Display input control signal*1 setup time	tDS	5	—	—	ns	Figure 73.13.2 (relative to DOTCLKIN) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
Display input control signal*1 hold time	tDH	3	—	—	ns	
DOTCLKOUT output cycle time	tDCYC	20	—	200	ns	Figure 73.13.3 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		13.3	—	200	ns	Figure 73.13.3 [RZ/G2E]
DOTCLKOUT output high level width	tDCKH	5	—	—	ns	Figure 73.13.3
Display output control signal*1 output delay time (Relative to DOTCLKOUT rising edge*3)	tDD	2	—	8.5	ns	Figure 73.13.3 (relative to DOTCLKOUT) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		2	—	11	ns	Figure 73.13.3 (relative to DOTCLKOUT) [RZ/G2E]
Display output control signal*1 output delay time (Relative to DOTCLKOUT falling edge*4)	tDDf	1.5	—	9.0	ns	Figure 73.13.4 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		1.5	—	11.5	ns	Figure 73.13.4 [RZ/G2E]
Display digital data*1 output delay time (Relative to DOTCLKOUT rising edge*3)	tDD	2	—	8.5	ns	Figure 73.13.3 (relative to DOTCLKOUT) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		2	—	11	ns	Figure 73.13.3 (relative to DOTCLKOUT) [RZ/G2E]

Correction (to):

Table 73.13.2 Display Signal Timing

Conditions: VDDQ33 = 3.3 V ± 0.2 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] / ± 0.3 V[RZ/G2E],
GND = VSS = 0 V,
Tc = -40 to +115 °C, [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 20 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Display input control signal*1 setup time	tDS	5	—	—	ns	Figure 73.13.2 (relative to DOTCLKIN) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
Display input control signal*1 hold time	tDH	3	—	—	ns	
DOTCLKOUT output cycle time	tDCYC	20	—	200	ns	Figure 73.13.3 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		13.3	—	200	ns	Figure 73.13.3 [RZ/G2E]
DOTCLKOUT output high level width	tDCKH	5	—	—	ns	Figure 73.13.3
Display output control signal*1 output delay time (Relative to DOTCLKOUT rising edge*3)	tDD	2	—	8.5	ns	Figure 73.13.3 (relative to DOTCLKOUT) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		2	—	11	ns	Figure 73.13.3 (relative to DOTCLKOUT) [RZ/G2E]
Display output control signal*1 output delay time (Relative to DOTCLKOUT falling edge*4)	tDDf	1.5	—	9.0	ns	Figure 73.13.4 [RZ/G2N]
Display digital data*1 output delay time (Relative to DOTCLKOUT rising edge*3)	tDD	2	—	8.5	ns	Figure 73.13.3 (relative to DOTCLKOUT) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		2	—	11	ns	Figure 73.13.3 (relative to DOTCLKOUT) [RZ/G2E]

Current (from):

Display digital data*1 output delay time (Relative to DOTCLKOUT falling edge*4)	tDDf	1.5	—	9.0	ns	Figure 73.13.4 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
		1.5	—	11.5	ns	Figure 73.13.4 [RZ/G2E]
Display output control signal*1 output delay time 3*5 (Relative to DOTCLKOUT falling edge)	tDD3f	1.5	—	8.5	ns	Figure 73.13.6 [RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
Display digital data*1 output delay time 3*5 (Relative to DOTCLKOUT falling edge)	tDD3f	1.5	—	8.5	ns	Figure 73.13.6 [RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
Display output control signal*1 output delay time 3*6 (Relative to DOTCLKOUT rising edge)	tDD3	1.5	—	9.0	ns	Figure 73.13.7 [RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
Display digital data*1 output delay time 3*6 (Relative to DOTCLKOUT rising edge)	tDD3	1.5	—	9.0	ns	Figure 73.13.7 [RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
EXHSYNC# input low level width	tEXHLW	4tDCYC	—	—	ns	Figure 73.13.5 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
EXHSYNC# input high level width	tEXHHW	4tDCYC	—	—	Ns	
EXVSYNC# input low level width	tEXVLW	3HC	—	—	tDCYC	
ODDF# setup time 1*2	tOD1	(ys+yw) × HC	—	—	tDCYC	
ODDF# setup time 2*2	tOD2	1HC	—	—	tDCYC	

Notes: 1. For correspondence between these signals and pin names, refer to Table 73.9.4.
2. ys, yw and HC in Min value of ODDF# setup time 1 and ODDF# setup time 2 (tOD1 and tOD2);
ys: From rise of VSYNC to display start position in the vertical direction of the display screen (unit: raster line)
yw: Vertical display period of display screen (unit: raster line)
HC: Horizontal scan period (unit: dot clock)
3. Set bit 25 in ESCRn to B'0(Initial value). (n = 3[RZ/G2H, RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0], n = 0 and 1[RZ/G2E])
4. Set bit 25 in ESCRn to B'1. (n = 3[RZ/G2H, RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0], n = 0 and 1[RZ/G2E])
5. Signal is output on the falling edge.
Set the falling edge in OTARn. (n = 3[RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0])
Set bit 25 in ESCRn to B'0(Initial value). (n = 3[RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0])
6. Data is output on the falling edge.
Set the falling edge in OTARn. (n = 3[RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0])
Set bit 25 in ESCRn to B'1. (n = 3[RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0])

Correction (to):

Display digital data*1 output delay time (Relative to DOTCLKOUT falling edge*4)	tDDf	1.5	—	9.0	ns	Figure 73.13.4 [RZ/G2N]
EXHSYNC# input low level width	tEXHLW	4tDCYC	—	—	ns	Figure 73.13.5 [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
EXHSYNC# input high level width	tEXHHW	4tDCYC	—	—	Ns	
EXVSYNC# input low level width	tEXVLW	3HC	—	—	tDCYC	
ODDF# setup time 1*2	tOD1	(ys+yw) × HC	—	—	tDCYC	
ODDF# setup time 2*2	tOD2	1HC	—	—	tDCYC	

Notes: 1. For correspondence between these signals and pin names, refer to Table 73.13.4.
2. ys, yw and HC in Min value of ODDF# setup time 1 and ODDF# setup time 2 (tOD1 and tOD2).

   ys: From rise of VSYNC to display start position in the vertical direction of the display screen (unit: raster line)
   yw: Vertical display period of display screen (unit: raster line)
   HC: Horizontal scan period (unit: dot clock)
3. Set bit 25 in ESCRn to B'0(Initial value). (n = 3[RZ/G2H, RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0], n = 0 and 1[RZ/G2E])
4. Set bit 25 in ESCRn to B'1. (n = 3 [RZ/G2N])

[Description]

Remove specification of tDDf (except RZ/G2N), tDD3f and tDD3 (for all product) and notes about tDDf (except RZ/G2N), tDD3f and tDD3 (for all product) specification.

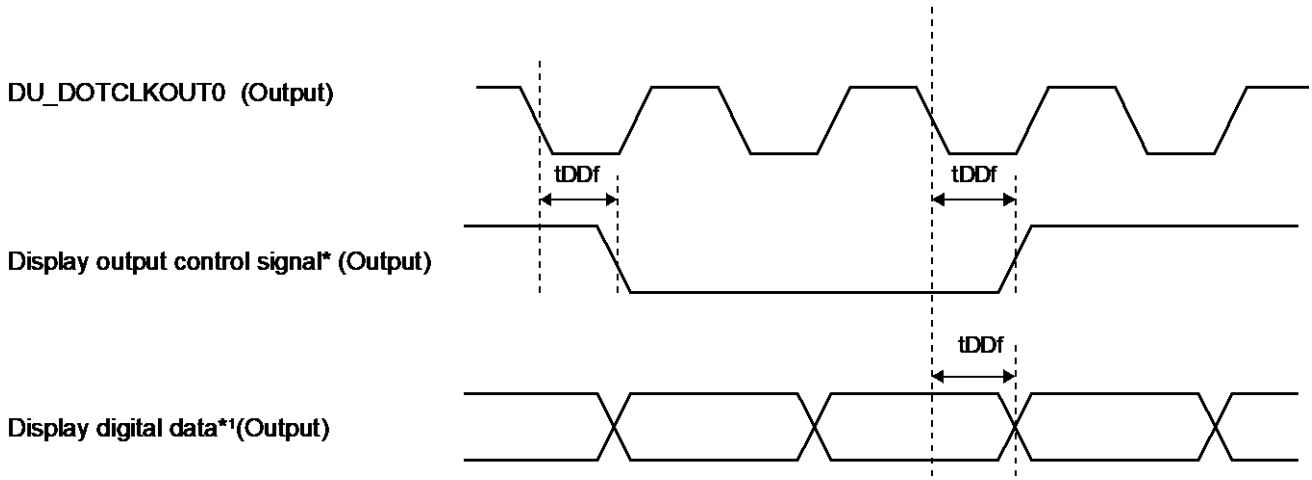
[Reason for Correction]

Since the value of tDDf (except RZ/G2N), tDD3f and tDD3 (for all product) are reference value (design value), remove them from User's Manual.

[Correction]

2. Section 73.13. DU, Page 73-65, 73-66, Table 73.13.2 Display Signal Timing, tDD3, tDD3f and related descriptions are removed.

Current (from):



Note: * For pin names corresponding to these signals, refer to Table 73.13.4.

Figure 73.13.4 Display Signal Timing (Relative to DOTCLKOUT falling edge)
[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E]

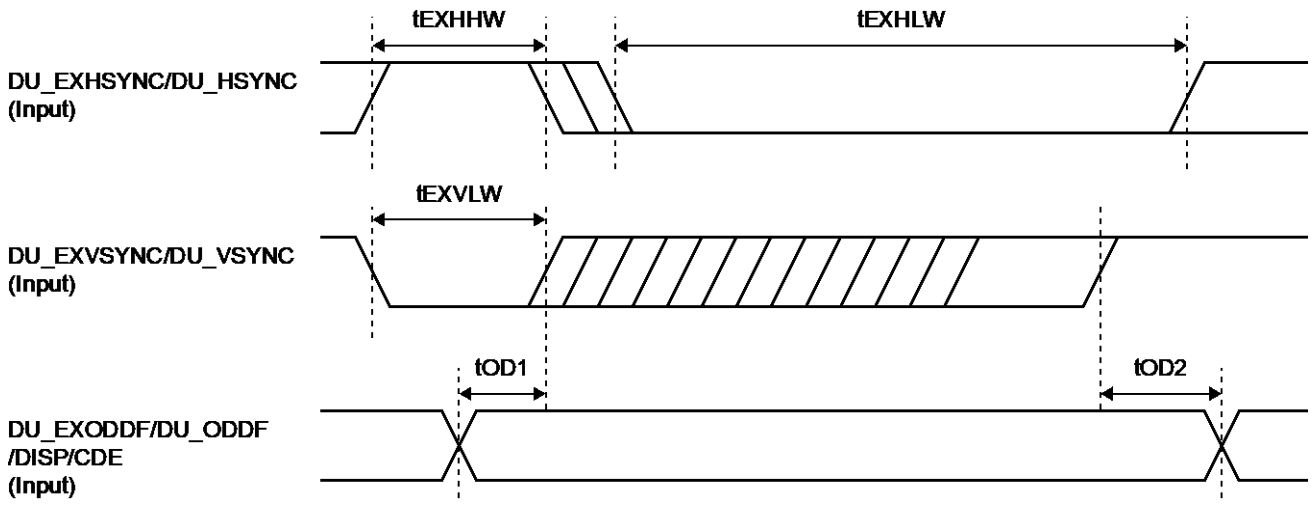
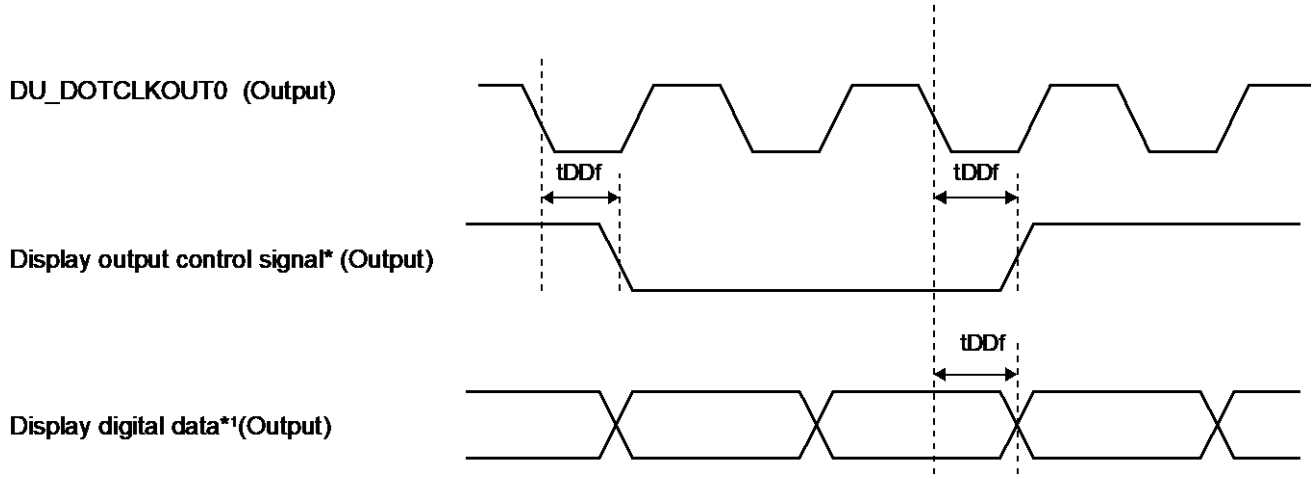


Figure 73.13.5 TV Sync Mode Display Signal Timing [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Correction (to):



Note: * For pin names corresponding to these signals, refer to Table 73.13.4.

Figure 73.13.4 Display Signal Timing (Relative to DOTCLKOUT falling edge) [RZ/G2N]

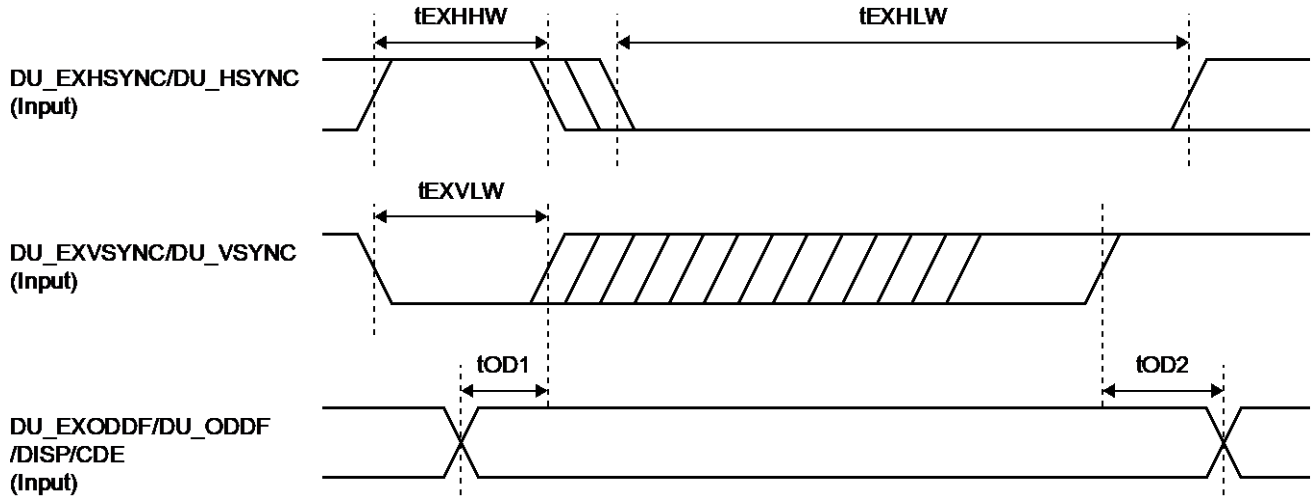
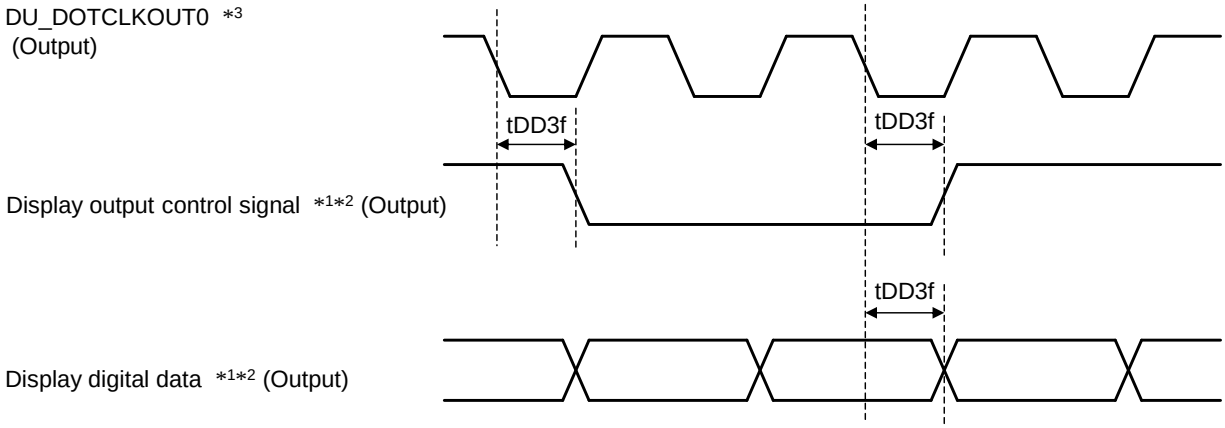


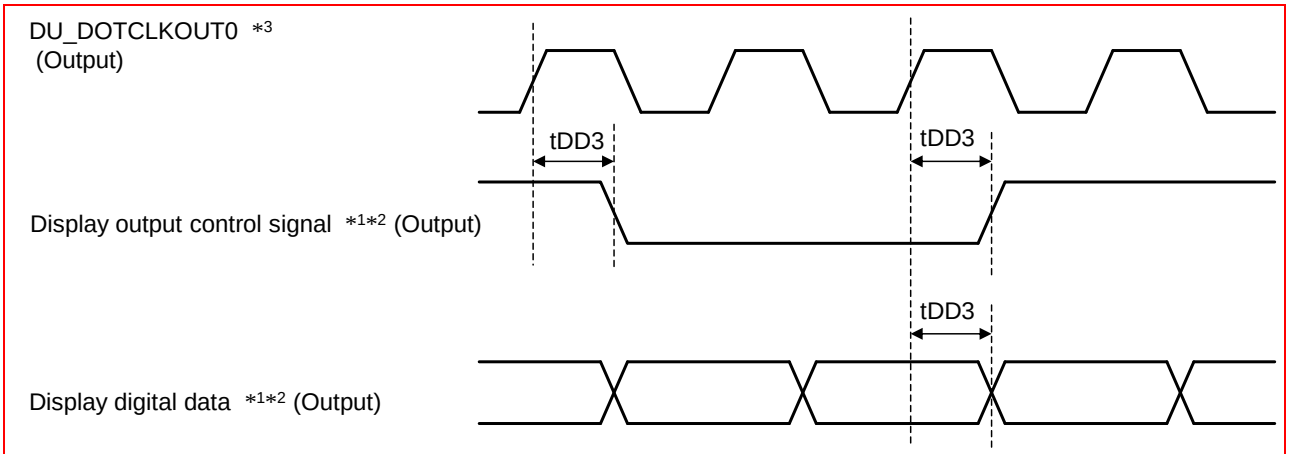
Figure 73.13.5 TV Sync Mode Display Signal Timing [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Current (from):



Notes: 1. For pin names corresponding to these signals, refer to table 73.13.4.
2. Set the falling edge in OTARn. (n = 3[RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0])
3. Set bit 25 in ESCRn to B'0(Initial value). (n = 3[RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0])

Figure 73.13.6 Display Signal Timing (Relative to DOTCLKOUT falling edge) [RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]



Notes: 1. For pin names corresponding to these signals, refer to table 73.13.4.
2. Set the falling edge in OTARn. (n = 3[RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0])
3. Set bit 25 in ESCRn to B'1. (n = 3[RZ/G2N], n = 2[RZ/G2M V1.3, RZ/G2M V3.0])

Figure 73.13.7 Display Signal Timing (Relative to DOTCLKOUT rising edge) [RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Correction (to):

— (Removed)

[Description]

Remove figure about tDDf (except RZ/G2N), tDD3f and tDD3 (for all product) specification.

[Reason for Correction]

Since the value of tDDf (except RZ/G2N), tDD3f and tDD3 (for all product) are reference value (design value), remove them from User's Manual.

End of Document -