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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0127A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Limitation of section 56.SPI Multi I/O Bus Controller (RPC-IF)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, RZ/G2M V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 (R01UH0808EJ0111)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Limitation of section 56.SPI Multi I/O Bus Controller (RPC-IF).

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 56. SPI Multi I/O Bus Controller (RPC-IF)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 56. RPC-IF, Page 56-105, 56.4.7 Frequency change (1) RPCCKCR

Current (from):

56.4.5 Software Reset after Module Stop operation

Be sure to supply software reset to this module after module stop is deactivated. Note that RPC_RESET# pin state is L while software reset is activated. Guarantee the reset period and accessible period after reset which are required in the connected devices.

56.4.6 DMA transfer

In read operation by DMA transfer, external address space read mode is available. The read address (source address in DMAC) is the memory area (H'0800_0000 – H'0BFF_FFFF) by Auto-Request mode. In High Speed response mode (PHYCNT.HS = 1), DRCR.RBURST should be set to B'1_1111 and access address alignment from RPC to flash memory should be 256Byte align. Accessing to register area during DMA transfer is prohibited during High Speed response mode.
In write operation, refer to 56.3.13.

56.4.7 Frequency change

(1) RPCCKCR

When the operation frequency changes by setting RPCCKCR in CPG, read after write operation on this register is necessary to guarantee the setting to be applied.

56.4.8 QSPI1 pins switched to high impedance [RZ/G2M V1.3] (not RZ/G2M V3.0)

Applying QSPI0 single boot (Mode pins MD[4:1] = 0100) the QSPI1 terminals are switched to high impedance. In case using a second QSPI flash device on the QSPI1 interface for 8-bit access later on, apply QSPI1_SPCLK with external pull-down and QSPI1_IOn [n = 3 to 0] with external pull-up resistors to the signal lines.

Correct (to):

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Be sure to supply software reset to this module after module stop is deactivated. Note that RPC_RESET# pin state is L while software reset is activated. Guarantee the reset period and accessible period after reset which are required in the connected devices.

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In write operation, refer to 56.3.13.

56.4.7 Frequency change

(1) RPCCKCR

When the operation frequency changes by setting RPCCKCR in CPG, read after write operation on this register is necessary to guarantee the setting to be applied.
And before changing RPCCKCR setting, set CMNCR.MOIIOx (x = 0, 1, 2, 3) register to B'11 (Hi-Z).

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[Description]
Add limitation when change operation frequency of this module.

[Reason for Correction]
Addition of limitation

- End of Document -