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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0132A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Limitation of section 56. SPI Multi I/O Bus Controller (RPC-IF)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 (R01UH0808EJ0111)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Limitation of section 56. SPI Multi I/O Bus Controller (RPC-IF) to avoid unexpected register read result and correcting read read-write attribute mismatch.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 56. SPI Multi I/O Bus Controller (RPC-IF)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 56. SPI Multi I/O Bus Controller (RPC-IF), Page 56-105, 56.4.9 Notes on RPC register area reading after read transfer with PHYCNT.HS=1 and read cache.

Current (from):

56.4.5 Software Reset after Module Stop operation

Be sure to supply software reset to this module after module stop is deactivated. Note that RPC_RESET# pin state is L while software reset is activated. Guarantee the reset period and accessible period after reset which are required in the connected devices.

56.4.6 DMA transfer

In read operation by DMA transfer, external address space read mode is available. The read address (source address in DMAC) is the memory area (H'0800_0000 – H'0BFF_FFFF) by Auto-Request mode. In High Speed response mode (PHYCNT.HS = 1), DRCR.RBURST should be set to B'1_1111 and access address alignment from RPC to flash memory should be 256Byte align. Accessing to register area during DMA transfer is prohibited during High Speed response mode.
In write operation, refer to 56.3.13.

56.4.7 Frequency change

56.4.7.1.1 RPCCKCR

When the operation frequency changes by setting RPCCKCR in CPG, read after write operation on this register is necessary to guarantee the setting to be applied.

56.4.8 QSPI1 pins switched to high impedance [RZ/G2M V1.3] (not RZ/G2M V3.0)

Applying QSPI0 single boot (Mode pins MD[4:1] = 0100) the QSPI1 terminals are switched to high impedance. In case using a second QSPI flash device on the QSPI1 interface for 8-bit access later on, apply QSPI1_SPCLK with external pull-down and QSPI1_IOn [n = 3 to 0] with external pull-up resistors to the signal lines.

Correct (to):

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56.4.9 Notes on RPC register area reading after read transfer with PHYCNT.HS=1 and read cache

When PHYCNT.HS=1, even if read access to RPC register area, read cache side address is also checked cache hit or not. And if Read cache is hit by this read access to RPC register area, read result becomes logical OR of register area data and read cache data. So, read data may be broken in this case.

For example, in the case of DREAR.EAV[7:0]=H'00, read cache treats register area address with PHYCNT.HS=1 as (2) and (3) in following **Table 56.18**.

And, when use PHYCNT.HS=1 setting, DMAC is used for read access to Memory area address. So, if last 256Byte address of DMAC transfer does not match with (4) and (5) in following Table 56.18, it is not applicable for this issue. Because, if that address is not matched, other address is stored in read cache after DMAC transfer.

In the case of last 256Byte address of DMAC transfer is matched, this issue can be avoided by PHYCNY.HS=0 or DRCR.RCF=1 before reading RPC register area.

Table 56.18 Example of Address relationship with DREAR.EAV[7:0]=H'00

No.	Explanation of related address	Address
(1)	Register Area address	H'EE20_0XXX
(2)	Read cache address with DREAR.EAC = 000b at Register Area address	H'0020_0XXX
(3)	Read cache address with DREAR.EAC = 001b at Register Area address	H'0220_0XXX
(4)	Memory area address to store H'0020_0XXX address in Read cache	H'0820_0XXX
(5)	Memory area address to store H'0220_0XXX address in Read cache	H'0A20_0XXX

[Description]

Limitation of memory area access when PHYCNT.HS = 1.

[Reason for Correction]

Add limitation for specific usage

- End of Document -