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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0080A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Document Corrections for Video Input Module (VIN)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.01 (R01UH0808EJ0101)		

This technical update describes document corrections of RZ/G Series, 2nd Generation product.

[Summary]

Document corrections for “RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.01”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZG2H

RZG2M V1.3

RZG2M V3.0

RZG2N

RZG2E

[Section number and title]

30. Video Input Module (VIN)

[Correction]

1. Section 30. VIN, Page 30-19, 30.1.4 Register Configuration. Correction of Note for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E.

Current (from):

30.1.4 Register Configuration

Table 30.10 through Table 30.13 show the VIN register configuration for each channel.

Notes: Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted.

Values read from addresses other than those listed below are undefined. The access size is no supported except for 32 bits.

* For the internal update mode, refer to the description of the VUP bit in the main control register (VnMC).

Δ: The internal update mode supports VnMC.CLP[1:0], VnMC.DPINE, VnMC.FOC, VnMC.LUTE bit only.

Correction (to):

30.1.4 Register Configuration

Table 30.10 through Table 30.13 show the VIN register configuration for each channel.

Notes: Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined. The access size is no supported except for 32 bits.

* For the internal update mode, refer to the description of the VUP bit in the main control register (VnMC).

Δ: The internal update mode supports VnMC.CLP[1:0], VnMC.DPINE, VnMC.FOC, VnMC.LUTE, VnMC.ISPE, VnMC.SCLE bit only.

[Description]

VnMC.ISPE and VnMC.SCLE are affected by “VnMC.VUP”.

[Reason for Correction]

The note was missing when the register was added.

2. Section 30. VIN, Page 30-147, 30.3.13 Transition to Module Standby Mode and 30.3.14 Cancellation of Module Standby Mode and Restarting of Video Input Module. Correction of Note for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E.

Correction (from):

30.3.13 Transition to Module Standby Mode

1. Clear the module enable (ME) bit in the main control register (VnMC) and the continuous frame capture (CC) bit and the single frame capture (SC) bit in the frame capture register (VnFC) to 0 to stop the video input module.
2. Confirm that the capture active (CA) bit in the module status register (VnMS) is cleared to 0*.
3. Stop the clock supply.

Note: * The camera device should be kept operation until the CA bit in VnMS set to 0.

30.3.14 Cancellation of Module Standby Mode and Restarting of Video Input Module

1. Start the clock supply.
2. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
3. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

Correction (to);

30.3.13 Transition to Module Standby Mode

1. Execute capture stop procedure described in section 30.3.18 if VIN is in capture operation.
2. Set MSTPm bit to 1 in RMSTPCRn of the clock pulse generator (CPG_MSTPRST) module.
3. Confirm that MSTPSTm bit to 1 in MSTPSRn of the clock pulse generator (CPG_MSTPRST) module.

For detail of registers of the clock pulse generator (CPG_MSTPRST) module, refer to section 12

30.3.14 Cancellation of Module Standby Mode

1. Set MSTPm bit to 0 in RMSTPCRn of the clock pulse generator (CPG_MSTPRST) module.
2. Confirm that MSTPSTm bit to 0 in MSTPSRn of the clock pulse generator (CPG_MSTPRST) module.
3. Set SRTm bit to 1 in the software reset register n (SRCRn) of the clock pulse generator (CPG_MSTPRST) module.
4. Set SRTCLRm to 1 in software reset clearing register n (SRSTCLRn) of the clock pulse generator (CPG_MSTPRST) module.

For detail of registers of the clock pulse generator (CPG_MSTPRST) module, refer to section 12.

[Description]

- Change the description of the capture stop sequence to section 30.3.18 which defines the sequence and change the clock supply stop to a specific procedure.
- Change start the clock supply to a specific procedure and remove descriptions of capture start.

[Reason for Correction]

To be consistent with the sequences defined in the other sections.

3. Section 30. VIN, Page 30-156, 30.3.17 Initialization Procedure. Correction of descriptions for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E.

Correction (from):

30.3.17 Initialize Procedure

The Initialization procedure of VIN is as followings.

(1) Case of inputting images from CSI-2 module

It is possible to run VIN initial procedure either before or after CSI2 initial procedure.

[VIN initial procedure]

1. Set VIN registers.
2. Set the VSYNC field toggle mode enable (FTEV) bit in the Video n data mode register 2 (VnDMR2) to 1. The VSYNC field toggle mode transition period (VLV[3:0]) bit in the VnDMR2 shall be set to 4'h0.
3. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
4. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

[CSI2 initial procedure]

1. Set the Link and PHY of CSI-2 module registers*[1].
2. Start camera device.
3. Confirm PHY of CSI-2 module starts.

(2) Case of inputting images from Digital Pins

1. Set pin function controller (PFC) registers*[2].
2. Start camera device.
3. Set SRTm bit to 1 in the software reset register n (SRCRn) of the clock pulse generator (CPG) module*[4].
4. Set SRTCLRm to 1 in software reset clearing register n (SRSTCLRn) of clock pulse generator (CPG) module*[4].
5. Set VIN registers.
6. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
7. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

(3) Case of inputting images from CSI-2 module and Digital Pins

It is possible to run VIN initial procedure either before or after CSI2 initial procedure.

[VIN initial procedure]

1. Set pin function controller (PFC) registers*[2].
2. Start camera side device of Digital Pins side.
3. Set SRTm bit to 1 in the software reset register n (SRCRn) of the clock pulse generator (CPG) module*[4].
4. Set SRTCLRm to 1 in software reset clearing register n (SRSTCLRn) of clock pulse generator (CPG) module*[4].
5. Set VIN registers.
6. Set the VSYNC field toggle mode enable (FTEV) bit in the Video n data mode register 2 (VnDMR2) to 1. The VSYNC field toggle mode transition period (VLV[3:0]) bit in the VnDMR2 shall be set to 4'h0*[3].
7. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.

8. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

[CSI2 initial procedure]

1. Set the Link and PHY of CSI-2 module registers*[1].
2. Start camera device of MIPI-CSI-2 side.
3. Confirm PHY of CSI-2 module starts.

Notes: 1. For detail, see section 29.

2. For detail, see section 8.

3. This setting is necessary to the channel which input images from CSI29-2 module.

4. For detail, see section 12.

Correction (to):

30.3.17 Initialize Procedure

The Initialization and capture start procedure of VIN is as followings.

(1) Case of inputting images from CSI-2 module

It is possible to run VIN initial procedure either before or after CSI2 initial procedure.

[VIN initial procedure]

1. Set VIN registers.
2. Set the VSYNC field toggle mode enable (FTEV) bit in the Video n data mode register 2 (VnDMR2) to 1. The VSYNC field toggle mode transition period (VLV[3:0]) bits in VnDMR2 shall be set to 4'h0 *3.
3. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
4. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

[CSI2 initial procedure]

1. Set the Link and PHY of CSI-2 module registers*1.
2. Start camera device.
3. Confirm PHY of CSI-2 module starts.

(2) Case of inputting images from Digital Pins

1. Set pin function controller (PFC) registers*2.
2. Start camera device.
3. Set SRTm bit to 1 in the software reset register n (SRCRn) of the clock pulse generator (CPG_MSTPRST) module*4.
4. Set SRTCLRm to 1 in software reset clearing register n (SRSTCLRn) of clock pulse generator (CPG_MSTPRST) module*4.
5. Set VUP bit in VnMC to 0.
6. Set DPINE bit in VnMC to 1 and keep this bit during the following sequence.
7. Set VUP bit in VnMC to the desired value.
8. Set VIN registers.
9. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
10. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

Notes: 1. For detail, see section 29.

2. For detail, see section 8.
3. This setting is necessary to the channel which input images from CSI-2 module.
4. For detail, see section 12.

[Description]

- Describing capture start operation explicitly in line 1.
- Add steps for changing to digital input port in paragraph (1).
- Removed the paragraph (3).

[Reason for Correction]

- Clarify the sequence.
- If the input interface before switching (may be CSI-2) is not used (and connected to ground) and the VnMC.VUP is set to 1 first, it will not be able to switch to digital input.
- Unnecessary and misleading statements

4. Section 30. VIN, Page 30-158, 30.3.18 Capture Stop Procedure. Correction of descriptions for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E.

Correction (from):

30.3.18 Capture Stop Procedure

The capture stop procedure of VIN is as followings.

(1) Case of inputting images from CSI-2 module

1. Clear the module enable (ME) bit in the main control register (VnMC) and the continuous frame capture (CC) bit and the single frame capture (SC) bit in the frame capture register (VnFC) to 0 to stop the video input module.
2. Confirm that the capture active (CA) bit in the module status register (VnMS) is cleared to 0*3.
3. Set MSTPm bit to 1 in the module stop control register n (RMSTPCRn) of the clock pulse generator (CPG) module*1.
4. Confirm that MSTPSTm bit to 1 in the module stop status register n (MSTPSRn) of the clock pulse generator (CPG) module*1.
5. Set SRTm bit to 1 in the software reset register n (SRCRn) of the clock pulse generator (CPG) module*1.
6. Reset the Link and PHY of CSI-2 module*2.
7. Stop camera device.

(2) Case of inputting images from Digital Pins

1. Clear the module enable (ME) bit in the main control register (VnMC) and the continuous frame capture (CC) bit and the single frame capture (SC) bit in the frame capture register (VnFC) to 0 to stop the video input module.
2. Confirm that the capture active (CA) bit in the module status register (VnMS) is cleared to 0*3.

(3) Case of inputting images from CSI-2 module and Digital Pins

1. Clear the module enable (ME) bit in the main control register (VnMC) and the continuous frame capture (CC) bit and the single frame capture (SC) bit in the frame capture register (VnFC) to 0 to stop the video input module.
2. Confirm that the capture active (CA) bit in the module status register (VnMS) is cleared to 0*3.
3. Set MSTPm bit to 1 in the module stop control register n (RMSTPCRn) of the clock pulse generator (CPG) module*1.
4. Confirm that MSTPSTm bit to 1 in the module stop status register n (MSTPSRn) of the clock pulse generator (CPG) module*1.
5. Set SRTm bit to 1 in the software reset register n (SRCRn) of the clock pulse generator (CPG) module*1.
6. Reset the Link and PHY of CSI-2 module*2.
7. Stop camera device of MIPI-CSI-2 side.

Notes: 1. For detail, see section 12.

2. For detail, see section 29.

3. The camera device should be kept operation until the CA bit in VnMS set to 0.

Correction (to):

30.3.18 Capture Stop Procedure

The capture stop procedure of VIN is as followings.

(1) Case of inputting images from CSI-2 module

1. Clear the module enable (ME) bit in the main control register (VnMC) and the continuous frame capture (CC) bit and the single frame capture (SC) bit in the frame capture register (VnFC) to 0 to stop the video input module.
2. Confirm that the capture active (CA) bit in the module status register (VnMS) is cleared to 0*3.
3. Reset the Link and PHY of CSI-2 module*2.
4. Stop camera device.

(2) Case of inputting images from Digital Pins

1. Clear the module enable (ME) bit in the main control register (VnMC) and the continuous frame capture (CC) bit and the single frame capture (SC) bit in the frame capture register (VnFC) to 0 to stop the video input module.
2. Confirm that the capture active (CA) bit in the module status register (VnMS) is cleared to 0*3.
3. Stop camera device.

Notes: 1. For detail, see section 12.

2. For detail, see section 29.

3. The camera device should be kept operation until the CA bit in VnMS set to 0.

[Description]

- Remove steps for module stop and VIN reset in paragraph (1)
- Add step 3 in paragraph (2).
- Remove the paragraph (3).

[Reason of Correction]

- To be consistent with the sequences defined in the other sections.
- Missing the description.
- Unnecessary and misleading statements.

5. Section 30. VIN, Page 30-159, 30.3.19 Capture Restarting Procedure. Correction of descriptions for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E.

Correction (from):

30.3.19 Capture Restarting procedure

The capture restarting procedure of VIN is as followings.

(1) Case of inputting images from CSI-2 module

It is possible to run VIN initial procedure either before or after CSI2 initial procedure.

[VIN initial procedure]

1. Set SRTCLRm to 1 in software reset clearing register n (SRSTCLRn) of clock pulse generator (CPG) module*[1].
2. Set MSTPm bit to 0 in the module stop control register n (RMSTPCRn) of the clock pulse generator (CPG) module*[1].
3. Confirm that MSTPSTm bit to 0 in the module stop status register n (MSTPSRn) of the clock pulse generator (CPG) module*[1].
4. Set VIN registers.
5. Set the VSYNC field toggle mode enable (FTEV) bit in the Video n data mode register 2 (VnDMR2) to 1. The VSYNC field toggle mode transition period (VLV[3:0]) bit in the VnDMR2 shall be set to 4'h0*[3].
6. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
7. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

[CSI2 initial procedure]

1. Set the Link and PHY of CSI-2 module registers*2.
2. Start camera device.
3. Confirm PHY of CSI-2 module starts.

(2) Case of inputting images from Digital Pins

1. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
2. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

(3) Case of inputting images from CSI-2 module and Digital Pins

It is possible to run VIN initial procedure either before or after CSI2 initial procedure.

[VIN initial procedure]

1. Set SRTCLRm to 1 in software reset clearing register n (SRSTCLRn) of clock pulse generator (CPG) module*[1].
2. Set MSTPm bit to 0 in the module stop control register n (RMSTPCRn) of the clock pulse generator (CPG)
3. Confirm that MSTPSTm bit to 1 in the module stop status register n (MSTPSRn) of the clock pulse generator (CPG) module*[1].
4. Set VIN registers.

5. Set the VSYNC field toggle mode enable (FTEV) bit in the Video n data mode register 2 (VnDMR2) to 1. The VSYNC field toggle mode transition period (VLV[3:0]) bit in the VnDMR2 shall be set to 4'h0*3.

6. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.

7. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

[CSI2 initial procedure]

1. Set the Link and PHY of CSI-2 module registers*2.

2. Start camera device of MIPI-CSI-2 side.

3. Confirm PHY of CSI-2 module starts.

Notes: 1. For detail, see section 12.

2. For detail, see section 29.

3. This setting is necessary to the channel which input images from CSI-2 module.

Correction (to):

30.3.19 Capture Restarting procedure

The capture restarting procedure of VIN is as followings. Note that if the input source changes from the previous capture process, the initialize procedure must be executed.

(1) Case of inputting images from CSI-2 module

It is possible to run VIN initial procedure either before or after CSI2 initial procedure.

[VIN initial procedure]

1. Set VIN registers.
2. Set the VSYNC field toggle mode enable (FTEV) bit in the Video n data mode register 2 (VnDMR2) to 1. The VSYNC field toggle mode transition period (VLV[3:0]) bits in VnDMR2 shall be set to 4'h0*3.
3. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
4. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

[CSI2 initial procedure]

1. Set the Link and PHY of CSI-2 module registers*2.
2. Start camera device.
3. Confirm PHY of CSI-2 module starts.

(2) Case of inputting images from Digital Pins

1. Start camera device.
2. Set SRTm bit to 1 in the software reset register n (SRCRn) of the clock pulse generator (CPG_MSTPRST) module*1.
3. Set SRTCLRm to 1 in software reset clearing register n (SRSTCLRn) of the clock pulse generator (CPG_MSTPRST) module*1.
4. Set VUP bit in VnMC to 0.
5. Set DPINE bit in VnMC to 1 and keep this bit during the following sequence.
6. Set VUP bit in VnMC to the desired value.
7. Set VIN registers.
8. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
9. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

Notes: 1. For detail, see section 12.

2. For detail, see section 29.

3. This setting is necessary to the channel which input images from CSI-2 module.

[Description]

- Add note for changing input interface in line 1.
- Remove steps for release VIN reset and module stop in paragraph (1).
- Add steps for starting camera device, VIN reset and changing to digital input port in paragraph (2).

- Remove the paragraph (3).

[Reason of Correction]

- Clarify the purpose of this sequence.
- To be consistent with the sequences defined in the other sections.
- If the input interface before switching (may be CSI-2) is not used (and connected to ground) and the VnMC.VUP is set to 1 first, it will not be able to switch to digital input. And it is necessary to reset VIN when digital input port is used.
- Unnecessary and misleading statements

6. Section 30. VIN, Page 30-160, 30.3.20 Rest Procedure. Addition of new sub section descriptions for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E.

Correction (from):

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Correction (to):

30.3.20 Reset Procedure

There are two reset sequences.

(1) Power-on Reset

The VIN is in a module-stopped state after power is turned on. The procedure of module stop release described in section 30.3.14 includes the VIN reset process.

(2) Reset when VIN gets Hang Up

If VIN gets hang up such as :

• The capture active (CA) bit in the module status register (VnMS) is not set to 1 after executing the initialize procedure in section 30.3.17 or the capture restarting procedure in section 30.3.19.

• The capture active (CA) bit in the module status register (VnMS) is not cleared to 0 after executing the capture stop procedure described in section 30.3.18.

• The end of frame interrupt status (EFS) bit or field interrupt status (FIS) bit is not set to 1 after more than one V-period of input video sequence.

• Or when it is judged that the VIN is not working.

VIN must be reset as follows :

1. Set SRTm bit to 1 in the software reset register n (SRCRn) of the clock pulse generator (CPG_MSTPRST) module.

2. Set SRTCLRm to 1 in software reset clearing register n (SRSTCLRn) of the clock pulse generator (CPG_MSTPRST) module.

For detail of registers of the clock pulse generator (CPG_MSTPRST), refer to section 12.

[Description]

Add the description of VIN reset sequence.

[Reason of correction]

Clarification of when a reset can be performed.

7. Section 30. VIN, page 30-166, 30.4.1 Specification. Item “The change of the video clock of Digital pin of Table 30.30 Specification, Description are corrected.

Correction (from):

Item	Description
The change of the video clock of Digital pin	VIN doesn’t support changing the video clock of Digital pin during VIN operation. After VIN operation start, if the video clock of Digital pin is changed, follow the following procedures. For detail of RMSTPCR8 and MSTPSR8 and SRSTCLR8, see section 12. [1] Set 1 to the MSTPn bit in RMSTPCR8 n = 807(VIN4), 806(VIN5) (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0) [2] Wait until the MSTPSTn bit in MSTPSR8 is set to 1 n = 807(VIN4), 806(VIN5) (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0) [3] Set 1 to the SRTn bit in SRCR8 n = 807(VIN4), 806(VIN5) (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0) [4] Change the video clock of Digital pin [5] Set 1 to the SRTCLRn bit in SRSTCLR8 n = 807(VIN4), 806(VIN5) (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0) [6] Set 0 to the MSTPn bit in RMSTPCR8n = 807(VIN4), 806(VIN5) RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0) [7] Wait until the MSTPSTn bit in MSTPSR8 is set to 0 n = 807(VIN4), 806(VIN5) (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0) [8] Configure the VIN register

Correction (to):

Item	Description
The change of the video clock of Digital pin	VIN doesn’t support changing the video clock of Digital pin during VIN operation. After VIN operation start, if the video clock of Digital pin is changed, follow the following procedures. For detail of RMSTPCR8 and MSTPSR8 and SRSTCLR8, see section 12. [1] Execute capture stop procedure described in section 30.3.18, if VIN is in capture operation. [2] Execute transition to module standby mode described in section 30.3.13. [3] Change the video clock of Digital pin [4] Execute cancellation of module standby mode described in section 30.3.14. [5] Execute initialization procedure described in section 30.3.17.

[Description]

Change the description of each step to a reference to the section that defines the sequence.

[Reason of correction]

To be consistent with the sequences defined in the other sections.

8. Section 30. VIN, Page 30-167. 30.4.3 Clock to Use, New section added for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E.

Correction (from):

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Correction (to):

30.4.3 Clock to Use

VIN for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N uses following clocks.

- S0D2ϕ 400MHz
- S0D8ϕ 100MHz

VIN for RZ/G2E uses following clocks.

- S1D2ϕ 266.66MHz
- S1D8ϕ 66.66MHz

[Description]

Add the clock lists of VIN.

[Reason of correction]

Clarification of the clock VIN uses.

End of Document -