Date: Aug. 30, 2022

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0095A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Document Correction for CAN-FD		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Document correction for “RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 48. CAN-FD

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(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 48. CAN-FD, Page 48-2, 48.1.1 Functional Overview, Table 48.1,Buffer descriptions. “Transmit FIFO: 3 FIFO per channel” description is removed.

Current (from):

Item	Specification
Buffer	• Individual buffers: 32 buffers (16 buffers × 2 channels) Transmit buffer: 16 buffers per channel Transmit FIFO: 3 FIFO per channel Transmit queue: Single queue per channel (shared with the transmit buffer; up to 16 buffers allocated) • Shared buffers: 128 buffers for all channels Receive buffer: 32 buffers Receive FIFO: 8 FIFO (up to 128 buffers allocated to each) Transmit/receive FIFO buffer: 3 FIFO buffers per channel (up to 128 buffers allocated to each) • ECC included
Reception function	• Receives data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be received. • Sets interrupt enable/disable for each FIFO. • Mirror function (reception of messages transmitted from the own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)
Reception filter function	• Selects receive messages according to 1 receive rule. • Sets the number of receive rules (0 to 128) for each channel. • Acceptance filter processing: Sets ID and mask for each receive rule. • DLC filter processing: Enables DLC filter check for each acceptance rule.
Receive message transfer function	• Routing function Transfers receive messages to arbitrary destinations (can be transferred to up to 8 buffers) Transfer destination: Receive buffer, receive FIFO buffer, and/or transmit/receive FIFO buffer • Label addition function Stores label information together with a message in a receive buffer and FIFO buffer.
Transmission function	• Transmits data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be transmitted. • Sets interrupt enable/disable for each transmit buffer and transmit/receive FIFO buffer. • Selects ID priority transmission or transmit buffer number priority transmission. • Transmit request can be aborted (possible to confirm with a flag) • One-shot transmission function
Interval transmission function	Transmit messages at configurable intervals (transmit mode or gateway mode of transmit/receive FIFO buffers)
Transmit queue function	Transmits all stored messages according to the ID priority.
Transmit history function	Stores the history information of transmission-completed messages Adds the timestamp to the history information (records the 16-bit timer value for the message transmission time).
Gateway function	Transmits a received message automatically.
Bus off recovery mode selection	Selects the method for returning from bus off state. • ISO11898-1 compliant • Automatic entry to channel halt mode at bus-off entry • Automatic entry to channel halt mode at bus-off end • Transition to channel standby mode by program request • Transition to the error-active state by program request (forcible return from the bus off state)

Correction (to):

Item	Specification
Buffer	• Individual buffers: 32 buffers (16 buffers × 2 channels) Transmit buffer: 16 buffers per channel Transmit queue: Single queue per channel (shared with the transmit buffer; up to 16 buffers allocated) • Shared buffers: 128 buffers for all channels Receive buffer: 32 buffers Receive FIFO: 8 FIFO (up to 128 buffers allocated to each) Transmit/receive FIFO buffer: 3 FIFO buffers per channel (up to 128 buffers allocated to each) • ECC included
Reception function	• Receives data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be received. • Sets interrupt enable/disable for each FIFO. • Mirror function (reception of messages transmitted from the own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)
Reception filter function	• Selects receive messages according to 1 receive rule. • Sets the number of receive rules (0 to 128) for each channel. • Acceptance filter processing: Sets ID and mask for each receive rule. • DLC filter processing: Enables DLC filter check for each acceptance rule.
Receive message transfer function	• Routing function Transfers receive messages to arbitrary destinations (can be transferred to up to 8 buffers) Transfer destination: Receive buffer, receive FIFO buffer, and/or transmit/receive FIFO buffer • Label addition function Stores label information together with a message in a receive buffer and FIFO buffer.
Transmission function	• Transmits data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be transmitted. • Sets interrupt enable/disable for each transmit buffer and transmit/receive FIFO buffer. • Selects ID priority transmission or transmit buffer number priority transmission. • Transmit request can be aborted (possible to confirm with a flag) • One-shot transmission function
Interval transmission function	Transmit messages at configurable intervals (transmit mode or gateway mode of transmit/receive FIFO buffers)
Transmit queue function	Transmits all stored messages according to the ID priority.
Transmit history function	Stores the history information of transmission-completed messages Adds the timestamp to the history information (records the 16-bit timer value for the message transmission time).
Gateway function	Transmits a received message automatically.
Bus off recovery mode selection	Selects the method for returning from bus off state. • ISO11898-1 compliant • Automatic entry to channel halt mode at bus-off entry • Automatic entry to channel halt mode at bus-off end • Transition to channel standby mode by program request • Transition to the error-active state by program request (forcible return from the bus off state)

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(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Description]

“Transmit FIFO: 3 FIFO per channel” description is removed from the overview of Buffer item.

[Reason for Correction]

General error correction.

[Correction]

2. Section 48. CAN-FD, Page 48-49, 48.7.5.1 RSCFDnRMNB - Receive Buffer Number Register, Bit NRXMB[7:0] description setting value corrected.

Current (from):

48.7.5 Details of Receive Buffer Related Registers

48.7.5.1 RSCFDnRMNB - Receive Buffer Number Register

Access: RSCFDnRMNB register can be read/written in 32-bit units

RSCFDnRMNBL, RSCFDnRMNBH registers can be read/written in 16-bit units

RSCFDnRMNBLL, RSCFDnRMNBLH, RSCFDnRMNBHL, RSCFDnRMNBHH registers can be read/written in 8-bit units

Address: RSCFDnRMNB: <RSCFDn_base> + H'00A4

RSCFDnRMNBL: <RSCFDn_base> + H'00A4, RSCFDnRMNBH: <RSCFDn_base> + H'00A6

RSCFDnRMNBLL: <RSCFDn_base> + H'00A4, RSCFDnRMNBLH: <RSCFDn_base> + H'00A5, RSCFDnRMNBHL: <RSCFDn_base> + H'00A6, RSCFDnRMNBHH: <RSCFDn_base> + H'00A7

Value after reset: H'0000 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	NRXMB[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	Reserved	All 0	R	These bits are read as the value after reset. The write value should be the value after reset.
7 to 0	NRXMB[7:0]	H'00	R/W	Receive Buffer Number Configuration These bits are used to set the total number of receive buffers of the RS-CANFD module. The maximum value is 16 × (number of channels). Setting these bits all to 0 makes receive buffers unavailable. Set a value of 0 to 96.

Modify the RSCFDnRMNB register only in global reset mode.

Correction (to):

48.7.5 Details of Receive Buffer Related Registers

48.7.5.1 RSCFDnRMNB - Receive Buffer Number Register

Access: RSCFDnRMNB register can be read/written in 32-bit units

RSCFDnRMNBL, RSCFDnRMNBH registers can be read/written in 16-bit units

RSCFDnRMNBLL, RSCFDnRMNBLH, RSCFDnRMNBHL, RSCFDnRMNBHH registers can be read/written in 8-bit units

Address: RSCFDnRMNB: <RSCFDn_base> + H'00A4

RSCFDnRMNBL: <RSCFDn_base> + H'00A4, RSCFDnRMNBH: <RSCFDn_base> + H'00A6

RSCFDnRMNBLL: <RSCFDn_base> + H'00A4, RSCFDnRMNBLH: <RSCFDn_base> + H'00A5, RSCFDnRMNBHL: <RSCFDn_base> + H'00A6, RSCFDnRMNBHH: <RSCFDn_base> + H'00A7

Value after reset: H'0000 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	NRXMB[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	Reserved	All 0	R	These bits are read as the value after reset. The write value should be the value after reset.
7 to 0	NRXMB[7:0]	H'00	R/W	Receive Buffer Number Configuration These bits are used to set the total number of receive buffers of the RS-CANFD module. The maximum value is 16 × (number of channels). Setting these bits all to 0 makes receive buffers unavailable. Set a value of 0 to 32.

Modify the RSCFDnRMNB register only in global reset mode.

[Description]

The setting range described in Description of NRXMB[7:0] is corrected.

[Reason for Correction]

General error correction.

[Correction]

3. Section 48. CAN-FD, Page 48-119, 48.7.13.1 RSCFDnGTSTCFG - Global Test Configuration Register, Bit 22 to 16, RTMPS[6:0], setting value range corrected.

Current (from):

48.7.13 Details of Test Related Registers

48.7.13.1 RSCFDnGTSTCFG - Global Test Configuration Register

Access: RSCFDnGTSTCFG register can be read/written in 32-bit units

RSCFDnGTSTCFGL, RSCFDnGTSTCFGH registers can be read/written in 16-bit units

RSCFDnGTSTCFGLL, RSCFDnGTSTCFGLH, RSCFDnGTSTCFGHL, RSCFDnGTSTCFGHH registers can be read/written in 8-bit units

Address: RSCFDnGTSTCFG: <RSCFDn_base> + H'0468

RSCFDnGTSTCFGL: <RSCFDn_base> + H'0468, RSCFDnGTSTCFGH: <RSCFDn_base> + H'046A

RSCFDnGTSTCFGLL: <RSCFDn_base> + H'0468, RSCFDnGTSTCFGLH: <RSCFDn_base> + H'0469, RSCFDnGTSTCFGHL: <RSCFDn_base> + H'046A, RSCFDnGTSTCFGHH: <RSCFDn_base> + H'046B

Value after reset: H'0000 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	RTMPS[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C1ICBCE	C0ICBCE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	Reserved	All 0	R	When read, the value after reset is returned. When writing to these bits, write the value after reset.
22 to 16	RTMPS[6:0]	H'00	R/W	RAM Test Page Configuration These bits are used to set the RAM test target page number for RAM test. Set a value in the range of H'00 to H'38, inclusive.
15 to 2	Reserved	All 0	R	When read, the value after reset is returned. When writing to these bits, write the value after reset.
1	C1ICBCE	0	R/W	CAN1 Inter-Channel Communication Test Enable Setting this bit to 1 enables the channel 1 inter-channel communication test. 0: CAN1 inter-channel communication test is disabled. 1: CAN1 inter-channel communication test is enabled.
0	C0ICBCE	0	R/W	CAN0 Inter-Channel Communication Test Enable Setting this bit to 1 enables the channel 0 inter-channel communication test. 0: CAN0 inter-channel communication test is disabled. 1: CAN0 inter-channel communication test is enabled.

Modify the RSCFDnGTSTCFG register only in global test mode.

Correction (to):

48.7.13 Details of Test Related Registers

48.7.13.1 RSCFDnGTSTCFG - Global Test Configuration Register

Access: RSCFDnGTSTCFG register can be read/written in 32-bit units

RSCFDnGTSTCFGL, RSCFDnGTSTCFGH registers can be read/written in 16-bit units

RSCFDnGTSTCFGLL, RSCFDnGTSTCFGLH, RSCFDnGTSTCFGHL, RSCFDnGTSTCFGHH registers can be read/written in 8-bit units

Address: RSCFDnGTSTCFG: <RSCFDn_base> + H'0468

RSCFDnGTSTCFGL: <RSCFDn_base> + H'0468, RSCFDnGTSTCFGH: <RSCFDn_base> + H'046A

RSCFDnGTSTCFGLL: <RSCFDn_base> + H'0468, RSCFDnGTSTCFGLH: <RSCFDn_base> + H'0469, RSCFDnGTSTCFGHL: <RSCFDn_base> + H'046A, RSCFDnGTSTCFGHH: <RSCFDn_base> + H'046B

Value after reset: H'0000 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	RTMPS[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C1ICBCE	C0ICBCE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	Reserved	All 0	R	When read, the value after reset is returned. When writing to these bits, write the value after reset.
22 to 16	RTMPS[6:0]	H'00	R/W	RAM Test Page Configuration These bits are used to set the RAM test target page number for RAM test. Set a value in the range of H'00 to H'13, inclusive.
15 to 2	Reserved	All 0	R	When read, the value after reset is returned. When writing to these bits, write the value after reset.
1	C1ICBCE	0	R/W	CAN1 Inter-Channel Communication Test Enable Setting this bit to 1 enables the channel 1 inter-channel communication test. 0: CAN1 inter-channel communication test is disabled. 1: CAN1 inter-channel communication test is enabled.
0	C0ICBCE	0	R/W	CAN0 Inter-Channel Communication Test Enable Setting this bit to 1 enables the channel 0 inter-channel communication test. 0: CAN0 inter-channel communication test is disabled. 1: CAN0 inter-channel communication test is enabled.

Modify the RSCFDnGTSTCFG register only in global test mode.

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[Description]

The setting range described in Description of RTMPS [6:0] is corrected.

[Reason for Correction]

General error correction.

4. Section 48. CAN-FD, Page 48-257, 48.9.14.1 RSCFDnCFDGTSTCFG — Global Test Configuration Register, Bit RTMPS[6:0] description setting value corrected.

Current (from):

48.9.14 Details of Test Related Registers

48.9.14.1 RSCFDnCFDGTSTCFG — Global Test Configuration Register

Access: RSCFDnCFDGTSTCFG register can be read/written in 32-bit units

RSCFDnCFDGTSTCFGL, RSCFDnCFDGTSTCFGH registers can be read/written in 16-bit units

RSCFDnCFDGTSTCFGLL, RSCFDnCFDGTSTCFGLH, RSCFDnCFDGTSTCFGHL, RSCFDnCFDGTSTCFGHH registers can be read/written in 8-bit units

Address: RSCFDnCFDGTSTCFG: <RSCFDn_base> + H'0468

RSCFDnCFDGTSTCFGL: <RSCFDn_base> + H'0468,
RSCFDnCFDGTSTCFGH: <RSCFDn_base> + H'046A

RSCFDnCFDGTSTCFGLL: <RSCFDn_base> + H'0468,
RSCFDnCFDGTSTCFGLH: <RSCFDn_base> + H'0469,
RSCFDnCFDGTSTCFGHL: <RSCFDn_base> + H'046A,
RSCFDnCFDGTSTCFGHH: <RSCFDn_base> + H'046B

Value after reset: H'0000 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	RTMPS[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C1ICBCE	C0ICBCE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	Reserved	All 0	R	When read, the value after reset is returned. When writing to these bits, write the value after reset.
22 to 16	RTMPS[6:0]	H'00	R/W	RAM Test Page Configuration These bits are used to set the RAM test target page number for RAM test. Set a value in the range of H'00 to H'53, inclusive.
15 to 2	Reserved	All 0	R	When read, the value after reset is returned. When writing to these bits, write the value after reset.
1	C1ICBCE	0	R/W	CAN1 Inter-Channel Communication Test Enable Setting this bit to 1 enables the channel 1 inter-channel communication test. 0: CAN1 inter-channel communication test is disabled. 1: CAN1 inter-channel communication test is enabled.
0	C0ICBCE	0	R/W	CAN0 Inter-Channel Communication Test Enable Setting this bit to 1 enables the channel 0 inter-channel communication test. 0: CAN0 inter-channel communication test is disabled. 1: CAN0 inter-channel communication test is enabled.

Modify the RSCFDnCFDGTSTCFG register only in global test mode.

Correction (to):

48.9.14 Details of Test Related Registers

48.9.14.1 RSCFDnCFDGTSTCFG — Global Test Configuration Register

Access: RSCFDnCFDGTSTCFG register can be read/written in 32-bit units

RSCFDnCFDGTSTCFGL, RSCFDnCFDGTSTCFGH registers can be read/written in 16-bit units

RSCFDnCFDGTSTCFGLL, RSCFDnCFDGTSTCFGLH, RSCFDnCFDGTSTCFGHL, RSCFDnCFDGTSTCFGHH registers can be read/written in 8-bit units

Address: RSCFDnCFDGTSTCFG: <RSCFDn_base> + H'0468

RSCFDnCFDGTSTCFGL: <RSCFDn_base> + H'0468,
RSCFDnCFDGTSTCFGH: <RSCFDn_base> + H'046A

RSCFDnCFDGTSTCFGLL: <RSCFDn_base> + H'0468,
RSCFDnCFDGTSTCFGLH: <RSCFDn_base> + H'0469,
RSCFDnCFDGTSTCFGHL: <RSCFDn_base> + H'046A,
RSCFDnCFDGTSTCFGHH: <RSCFDn_base> + H'046B

Value after reset: H'0000 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	RTMPS[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C1ICBCE	C0ICBCE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	Reserved	All 0	R	When read, the value after reset is returned. When writing to these bits, write the value after reset.
22 to 16	RTMPS[6:0]	H'00	R/W	RAM Test Page Configuration These bits are used to set the RAM test target page number for RAM test. Set a value in the range of H'00 to H'1B, inclusive.
15 to 2	Reserved	All 0	R	When read, the value after reset is returned. When writing to these bits, write the value after reset.
1	C1ICBCE	0	R/W	CAN1 Inter-Channel Communication Test Enable Setting this bit to 1 enables the channel 1 inter-channel communication test. 0: CAN1 inter-channel communication test is disabled. 1: CAN1 inter-channel communication test is enabled.
0	C0ICBCE	0	R/W	CAN0 Inter-Channel Communication Test Enable Setting this bit to 1 enables the channel 0 inter-channel communication test. 0: CAN0 inter-channel communication test is disabled. 1: CAN0 inter-channel communication test is enabled.

Modify the RSCFDnCFDGTSTCFG register only in global test mode.

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(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Description]

The setting range described in Description of RTMPS [6:0] is corrected.

[Reason for Correction]

General error correction.

5. Section 48. CAN-FD, Page 48-272, 48.11.3 registers Initialized by Transition to CAN Mode, Table 48.33 Registers Initialized in Global Reset Mode or Channel Reset Mode, RSCFDn(CFD)GTINTSTS1 register, Bit/Flag removed.

Current (from):

48.11.3 Registers Initialized by Transition to CAN Mode

Table 48.33 shows bits and flags initialized by transition to channel reset mode. These bits and flags are also initialized by transition to global reset mode. Table 48.34 shows bits and flags that are only initialized by transition to global reset mode.

Table 48.33 Registers Initialized in Global Reset Mode or Channel Reset Mode

Register	Bit / Flag
RSCFDn(CFD)CmCTR register	(ROM), CRCT, CTMS[1:0], CTME, CHMDC[1:0]
RSCFDn(CFD)CmSTS register	CHLTSTS, EPSTS, BOSTS, TRMSTS, RECSTS, COMSTS, (ESIF), REC[7:0], TEC[7:0]
RSCFDn(CFD)CmERFL register	CRCREG[14:0], ADERR, B0ERR, B1ERR, CERR, AERR, FERR, SERR, ALF, BLF, OVLF, BORF, BOEF, EPF, EWF, BEF
RSCFDnCFDCmFDCTR register	EOCCLR, SOCCLR
RSCFDnCFDCmFDSTS register	SOC[7:0], EOC[7:0], SOCO, EOCO, TDCVF, TDCR[6:0]
RSCFDnCFDCmFDCRC register	CRCREG[20:0]
RSCFDn(CFD)CFCCk register	When transmit/receive FIFO buffer is in transmit mode or gateway mode: CFE
RSCFDn(CFD)CFSTSk register	When transmit/receive FIFO buffer is in transmit mode or gateway mode: CFMC[7:0], CFFLL, CFEMP, CFMLT, CFRXIF, CFTXIF
RSCFDn(CFD)CFTISTS register	CFkTXIF
RSCFDn(CFD)TMCp register	TMOM, TMTAR, TMTR
RSCFDn(CFD)TMSTSp register	TMTARM, TMTRM, TMTRF[1:0], TMTSTS
RSCFDn(CFD)TMTRSTSy register	TMTRSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCFDn(CFD)TMTARSTSy register	TMTARSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCFDn(CFD)TMTCSTSy register	TMTCSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCFDn(CFD)TMTASTSy register	TMTASTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCFDn(CFD)TXQCCm register	TXQE
RSCFDn(CFD)TXQSTSm register	TXQIF, TXQFLL, TXQEMP
RSCFDn(CFD)THLCCm register	THLE
RSCFDn(CFD)THLSTSm register	THLMC[4:0], THLIF, THLELT, THLFLL, THLEMP
RSCFDn(CFD)GTINTSTS0 register	TSIFm, TAIFm, TQIFm, CFTIFm, THIFm (m = 0 or 1)
RSCFDn(CFD)GTINTSTS1 register	TSIFm, TAIFm, TQIFm, CFTIFm, THIFm (m = 4 or 5)

Note: Bits and flags enclosed by () only exist in registers for CAN FD mode.

Correction (to):

48.11.3 Registers Initialized by Transition to CAN Mode

Table 48.33 shows bits and flags initialized by transition to channel reset mode. These bits and flags are also initialized by transition to global reset mode. Table 48.34 shows bits and flags that are only initialized by transition to global reset mode.

Table 48.33 Registers Initialized in Global Reset Mode or Channel Reset Mode

Register	Bit / Flag
RSCFDn(CFD)CmCTR register	(ROM), CRCT, CTMS[1:0], CTME, CHMDC[1:0]
RSCFDn(CFD)CmSTS register	CHLTSTS, EPSTS, BOSTS, TRMSTS, RECSTS, COMSTS, (ESIF), REC[7:0], TEC[7:0]
RSCFDn(CFD)CmERFL register	CRCREG[14:0], ADERR, B0ERR, B1ERR, CERR, AERR, FERR, SERR, ALF, BLF, OVLF, BORF, BOEF, EPF, EWF, BEF
RSCFDnCFDCmFDCTR register	EOCCLR, SOCCLR
RSCFDnCFDCmFDSTS register	SOC[7:0], EOC[7:0], SOCO, EOCO, TDCVF, TDCR[6:0]
RSCFDnCFDCmFDCRC register	CRCREG[20:0]
RSCFDn(CFD)CFCCk register	When transmit/receive FIFO buffer is in transmit mode or gateway mode: CFE
RSCFDn(CFD)CFSTSk register	When transmit/receive FIFO buffer is in transmit mode or gateway mode: CFMC[7:0], CFFLL, CFEMP, CFMLT, CFRXIF, CFTXIF
RSCFDn(CFD)CFTISTS register	CFkTXIF
RSCFDn(CFD)TMCp register	TMOM, TMTAR, TMTR
RSCFDn(CFD)TMSTSp register	TMTARM, TMTRM, TMTRF[1:0], TMTSTS
RSCFDn(CFD)TMTRSTSy register	TMTRSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCFDn(CFD)TMTARSTSy register	TMTARSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCFDn(CFD)TMTCSTSy register	TMTCSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCFDn(CFD)TMTASTSy register	TMTASTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCFDn(CFD)TXQCCm register	TXQE
RSCFDn(CFD)TXQSTSm register	TXQIF, TXQFLL, TXQEMP
RSCFDn(CFD)THLCCm register	THLE
RSCFDn(CFD)THLSTSm register	THLMC[4:0], THLIF, THLELT, THLFLL, THLEMP
RSCFDn(CFD)GTINTSTS0 register	TSIFm, TAIFm, TQIFm, CFTIFm, THIFm (m = 0 or 1)
RSCFDn(CFD)GTINTSTS1 register	—

Note: Bits and flags enclosed by () only exist in registers for CAN FD mode.

[Description]

The description in column "Bit / Flag" of RSCFDn(CFD)GTINTSTS1 register is corrected.

[Reason for Correction]

General error correction.

[Correction]

6. Section 48. CAN-FD, Page 48-289, 48.15.5 RAM Test, The available total RAM size for classical CAN, and CAN FD mode are corrected there size.

Current (from):

48.15.4 Limited Operation Mode (CAN FD Mode Only)

When the enabled data and remote frames are received in limited operation mode, an ACK bit is generated. However, these frames are not transmitted even if the error frame or overload frame transmit condition is detected. When the condition is detected, CANFD waits for the bus idling state to resynchronize CAN communications. The receive error counter (REC) and the transmit error counter (TEC) are not changed if an error occurs.

For transmission, any transmit request can be issued with no limitations.

48.15.5 RAM Test

The RAM test function allows accesses to all CAN RAM addresses.

When the RAM test function is used, the RAM is divided into pages of 256 bytes each. RAM test page is set by the RTMPS[6:0] bits in the RSCFDn(CFD)GTSTCFG register. Data in the set page can be read from and written to the RSCFDn(CFD)RPGACCr register (r = 0 to 63). The available total RAM size is 15360 bytes (H'3C00) in classical CAN mode and 21312 bytes (H'53D0) in CAN FD mode.

48.15.6 Inter-Channel Communication Test

The inter-channel communication test function allows communication test by internally connecting CAN channels to each other. During this test, channels are isolated from the external CAN bus.

Before starting data transmission/reception in channel communication mode, make transmission/reception settings for each channel.

Figure 48.15 shows the connection for inter-channel communication test.

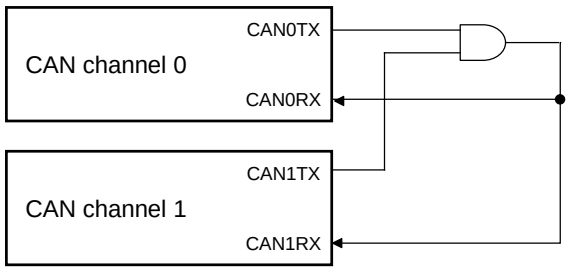

Figure 48.15 Connection for Inter-Channel Communication Test

Correction (to):

48.15.4 Limited Operation Mode (CAN FD Mode Only)

When the enabled data and remote frames are received in limited operation mode, an ACK bit is generated. However, these frames are not transmitted even if the error frame or overload frame transmit condition is detected. When the condition is detected, CANFD waits for the bus idling state to resynchronize CAN communications. The receive error counter (REC) and the transmit error counter (TEC) are not changed if an error occurs.

For transmission, any transmit request can be issued with no limitations.

48.15.5 RAM Test

The RAM test function allows accesses to all CAN RAM addresses.

When the RAM test function is used, the RAM is divided into pages of 256 bytes each. RAM test page is set by the RTMPS[6:0] bits in the RSCFDn(CFD)GTSTCFG register. Data in the set page can be read from and written to the RSCFDn(CFD)RPGACCr register (r = 0 to 63). The available total RAM size is 5056 bytes (H'13C0) in classical CAN mode and 7104 bytes (H'1BC0) in CAN FD mode.

48.15.6 Inter-Channel Communication Test

The inter-channel communication test function allows communication test by internally connecting CAN channels to each other. During this test, channels are isolated from the external CAN bus.

Before starting data transmission/reception in channel communication mode, make transmission/reception settings for each channel.

Figure 48.15 shows the connection for inter-channel communication test.

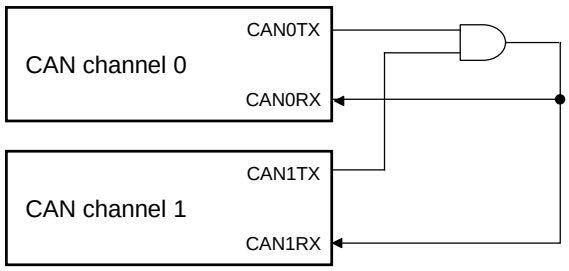

Figure 48.15 Connection for Inter-Channel Communication Test

[Description]

Correction of available total RAM size for classical CAN mode and CAN FD mode.

[Reason for Correction]

General error correction.

[Correction]

7. Section 48 CAN-FD. Page 48-298, 48.16.1.5 Setting Buffers, Correction for Figure 48.20 Buffer Configuration, description concerning buffers are removed, because its values depend on products.

Current (from):

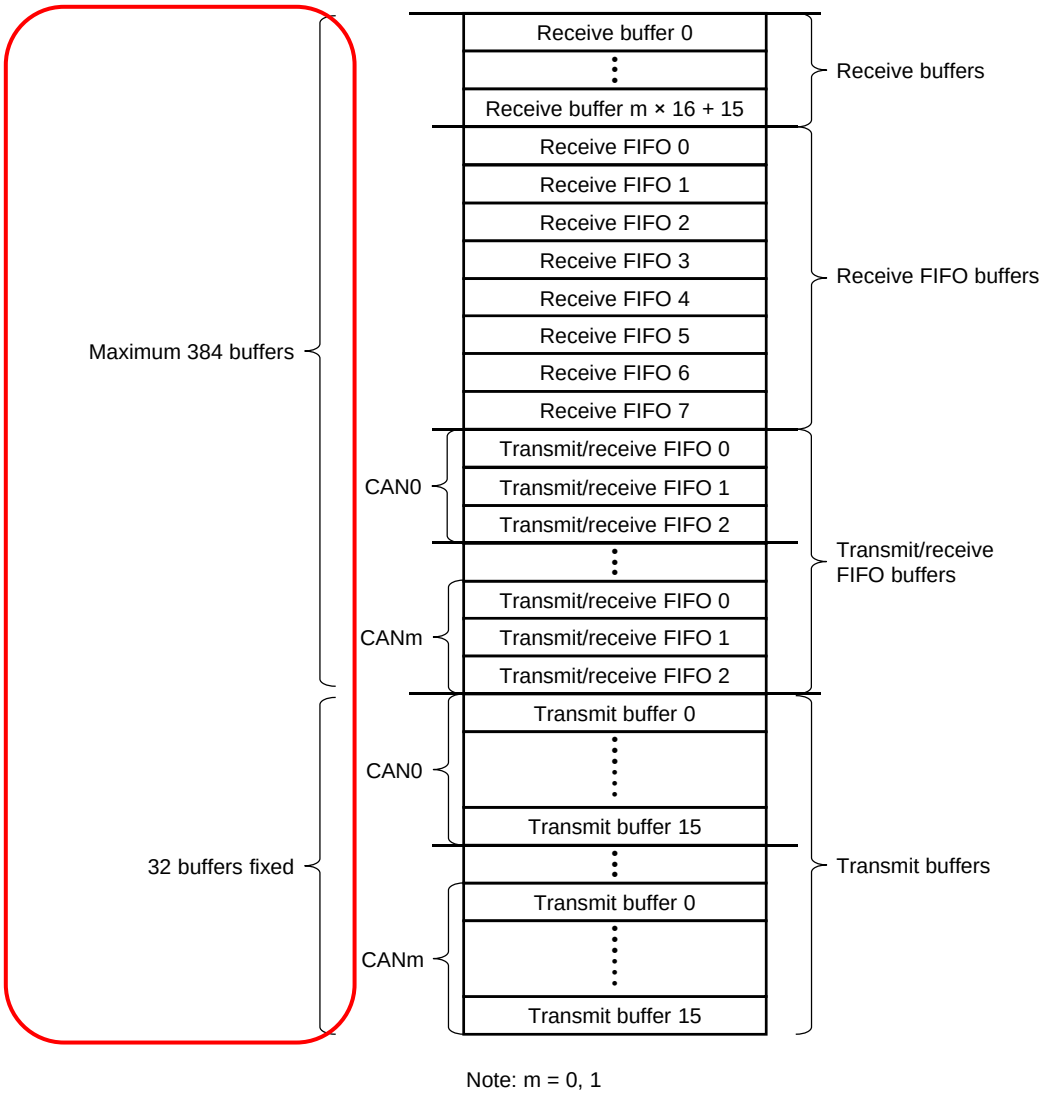

Figure 48.20 Buffer Configuration

Note: Receive buffers, receive FIFO buffers, transmit/receive FIFO buffers, and transmit buffers are located in succession.

Correction (to):

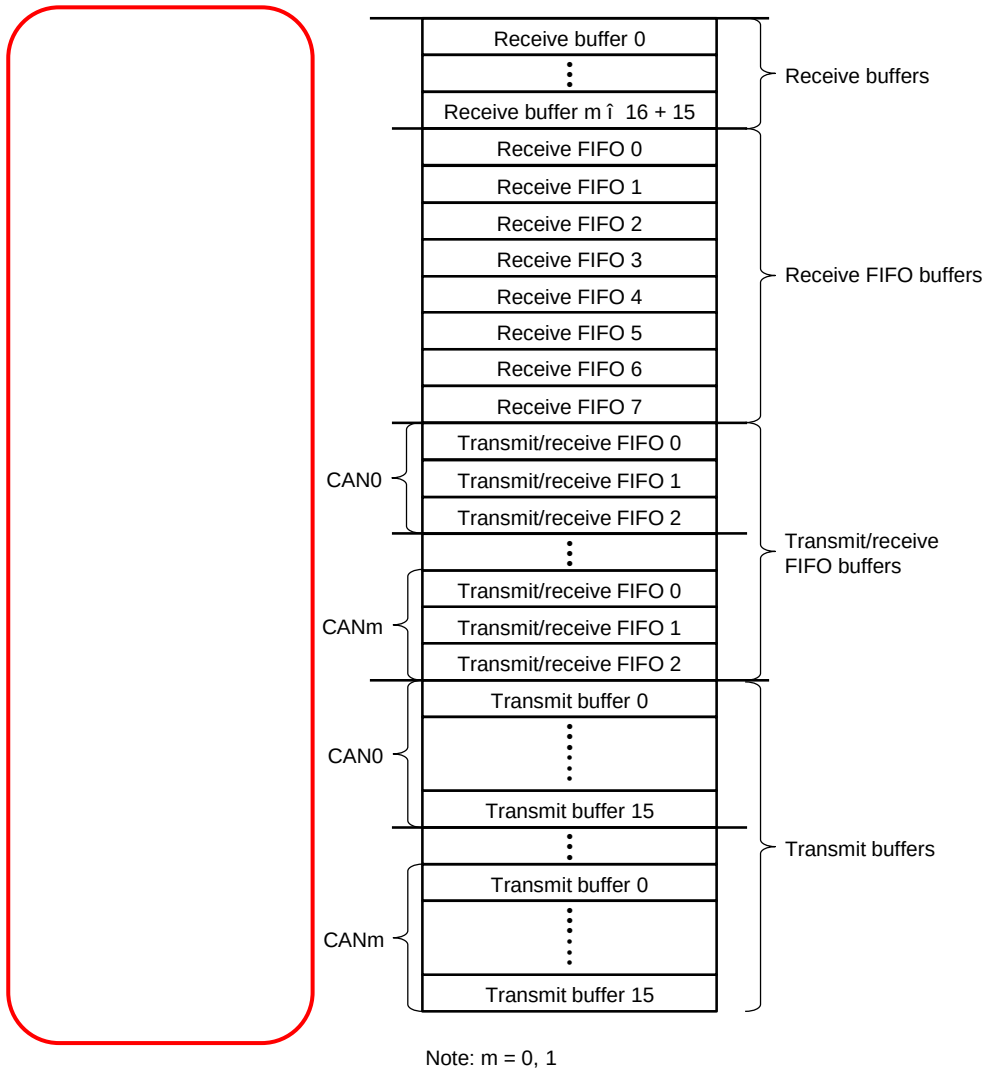

Figure 48.20 Buffer Configuration

Note: Receive buffers, receive FIFO buffers, transmit/receive FIFO buffers, and transmit buffers are located in succession.

[Description]

In Figure 48.20 Buffer Configuration, description concerning buffers are removed

[Reason for Correction]

Description concerning buffers are removed because its values depend on products.

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