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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0085A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Additional Descriptions and Document Corrections for IPMMU		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Additional Descriptions and Document Corrections for “Section 22. IPMMU”

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 22. IPMMU

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 22. IPMMU, Page 22-68, 22.5.3 Restrictions for IPMMU, Section of 22.5.3.5 to 22.5.3.12 restriction description are clarified by adding descriptions.

Current (from):

22.5.3 Restrictions for IPMMU

22.5.3.5 Virtual address space range

In case of using MMU, Virtual address space range cannot be configured less than or equal 128MB. In case of supporting this address range, set virtual address space range to 256MB by setting TSZ0/TSZ1 and unnecessary area is not mapped by MMU.

22.5.3.6 Treatments of ASID feature

In RZ/G2, IPMMU is not supported ASID feature. Software should not set the value except “0” in IMUASID register.

22.5.3.7 Disabling the address translation by IPMMU

Even if a master IP is disabling the address translation by IPMMU, IMUCTRn.TTSEL[2:0] needs to be set unused MMU context number. It means that only seven MMU context can be used for the address translation by IPMMU in this case.

22.5.3.8 Restriction for DMAC transfer [RZ/G2M V1.3 only]

SYS-DMAC/AUDIO-DMAC cannot support read interleaving feature. In order to avoid this occurrence, it is required to apply the following restriction in case that SYS-DMAC/AUDIO-DMAC need to access address space exceeding 32-bit.

1. Don’t set the transfer size exceeding 16 bytes in case of using IPMMU
2. Use 1GB page in order to avoid TLB miss.
3. Don’t use IPMMU. Use extended address function which is implemented in SYS-DMAC/AUDIO-DMAC.

22.5.3.9 Restriction for OS-ID support [RZ/G2M V1.3 only]

In order to perform address translation for 3DG Engine by IPMMU normally, context switching by OS-ID cannot be used. It is required to set the same MMU context number to each uTLB for 3DG Engine.

22.5.3.10 Restriction for TLB location [RZ/G2M V1.3 only]

TLB for address translation by IPMMU cannot be located at System-RAM. It is required to put TLB in the main memory.

22.5.3.11 Restriction for TLB flush operation [RZ/G2M V1.3 only]

In order to perform address translation by IPMMU normally, it is limited to replace the MMU context dynamically so as not to perform TLB flush operation. Use 1GB page to avoid this occurrence. Or Flush IPMMU cache or micro-TLB operation must only be performed while corresponding bus master is idle (no bus activity). Flush operations can be avoided by using statically defined Contexts.

22.5.3.12 Restriction for IPMMU cache [RZ/G2M V1.3, RZ/G2N, RZ/G2E]

In order to perform address translation by IPMMU normally, it is limited not to use IPMMU cache. In RZ/G2N and RZ/G2E, it is required to disable IPMMU cache by setting “IMSCTLR.dismmu” to 1. Address translation operation can be avoided by using statically defined Contexts. In RZ/G2M V1.3, IPMMU cache is always disabled by hardware. IPMMU cache cannot be used.

Correction (to):

22.5.3 Restrictions for IPMMU

22.5.3.5 Virtual address space range

In case of using MMU, Virtual address space range cannot be configured less than or equal 128MB. In case of supporting this address range, set virtual address space range to 256MB by setting TSZ0/TSZ1 and unnecessary area is not mapped by MMU. This restriction is notified as "Virtual address space setting to <=128MB".

22.5.3.6 Treatments of ASID feature

In RZ/G2, IPMMU is not supported ASID feature. Software should not set the value except “0” in IMUASID register.

22.5.3.7 Disabling the address translation by IPMMU

Even if a master IP is disabling the address translation by IPMMU, IMUCTRn.TTSEL[2:0] needs to be set unused MMU context number. It means that only seven MMU context can be used for the address translation by IPMMU in this case.

22.5.3.8 Restriction for DMAC transfer [RZ/G2M V1.3 only]

SYS-DMAC/AUDIO-DMAC cannot support read interleaving feature. To avoid this occurrence, it is required to apply the following restriction in case that SYS-DMAC/AUDIO-DMAC need to access address space exceeding 32-bit. This restriction is notified as "DMA operation".

1. Don’t set the transfer size exceeding 16 bytes in case of using IPMMU
2. Use 1GB page to avoid TLB miss.
3. Don’t use IPMMU. Use extended address function which is implemented in SYS-DMAC/AUDIO-DMAC.

22.5.3.9 Restriction for OS-ID support [RZ/G2M V1.3 only]

To perform address translation for 3DG Engine by IPMMU normally, context switching by OS-ID cannot be used. It is required to set the same MMU context number to each uTLB for 3DG Engine. This restriction is notified as "Automatic context selection by os_id".

22.5.3.10 Restriction for TLB location [RZ/G2M V1.3 only]

TLB for address translation by IPMMU cannot be located at System-RAM. It is required to put TLB in the main memory. This restriction is notified as "Page table in System RAM".

22.5.3.11 Restriction for TLB flush operation [RZ/G2M V1.3 only]

To perform address translation by IPMMU normally, it is limited to replace the MMU context dynamically so as not to perform TLB flush operation. Use 1GB page to avoid this occurrence. Or Flush IPMMU cache or micro-TLB operation must only be performed while corresponding bus master is idle (no bus activity). Flush operations can be avoided by using statically defined Contexts. This restriction is notified as "µTLB address translation".

22.5.3.12 Restriction for IPMMU cache [RZ/G2M V1.3, RZ/G2N, RZ/G2E]

To perform address translation by IPMMU normally, it is limited not to use IPMMU cache. In RZ/G2N and RZ/G2E, it is required to disable IPMMU cache by setting “IMSCTLR.dismmu” to 1. Address translation operation can be avoided by using statically defined Contexts. In RZ/G2M V1.3, IPMMU cache is always disabled by hardware. IPMMU cache cannot be used. This restriction is notified as "Address translation" and "Multiple translation requests handling".

[Description]

Restriction for all product, and restrictions for RZ/G2M V1.3 are corrected.

[Reason for Correction]

Additional explanation.

[Correction]

2. Section 22. IPMMU, Page 22-69, 22.5.3 Restrictions for IPMMU, Section of 22.5.3.14 to 22.5.3.16 restrictions are added for RZ/G2M V1.3.

Current (from):

22.5.3 Restrictions for IPMMU

22.5.3.13 Restriction for PMB

In order to perform address translation by IPMMU normally, it is limited not to use PMB mode in secure mode. Use PMB mode only in non-secure mode

Correction (to):

22.5.3 Restrictions for IPMMU

22.5.3.13 Restriction for PMB

To perform address translation by IPMMU normally, it is limited not to use PMB mode in secure mode. Use PMB mode only in non-secure mode.

22.5.3.14 Restriction for PMB with stage 2 Translation [RZ/G2M V1.3 only]

To perform address translation by IPMMU normally, it is limited not to use PMB mode with stage 2 Translation. Use MMU mode only in stage 2 Translation. This restriction is notified as "PMB address translation".

22.5.3.15 Restriction for 4K page TLB merge function [RZ/G2M V1.3 only]

4K page TLB merge functionality (default setting) in main IPMMU is not supported. Disable 4K page TLB merging functionality before enabling IPMMU functionality. For details, set value 1 nmerge40 bit and nmerge32 bit in MMU Auxiliary Control Register (IMSAUXCTLR). This restriction is notified as "4K page TLB merge function".

22.5.3.16 Restriction for pages size handling [RZ/G2M V1.3 only]

Two different behaviors in case of assigned page sizes:
1.When 512MB page size is used, which is supported by ARMv8 VMSAv8-64s, an incorrect address translation might occur.
2.When 64KB page size is set it will be treated as 4KB page size.
To prevent these restrictions, set page sizes to 4KB, 2MB, 1GB unit only. This restriction is notified as " Pages size handling".

[Description]

Restrictions for RZ/G2M V1.3 are added.

[Reason for Correction]

Additional explanation.

- End of Document -