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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0120A/E	Rev.	1.00
Title	RZ/G2H, G2M, G2N and G2E Correction of section 61. USB High-Speed Module (HS-USB)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E	Lot No.	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 (R01UH0808EJ0111)		
		All lots				

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Correction of section 61. High-Speed Module (HS-USB), correcting description for comments on figure for USB Data Bus

Regsiter Control, and Notes for Software reset when the USB disconnection is detected.

[Priority level]

Importance: "Normal"

Urgency: "Normal"

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 61. USB High-Speed Module (HS-USB)

"This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. "

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1.   Section 61.HS-USB, Page 61-80, Figure 61.1 "Connection to the USB Connector".
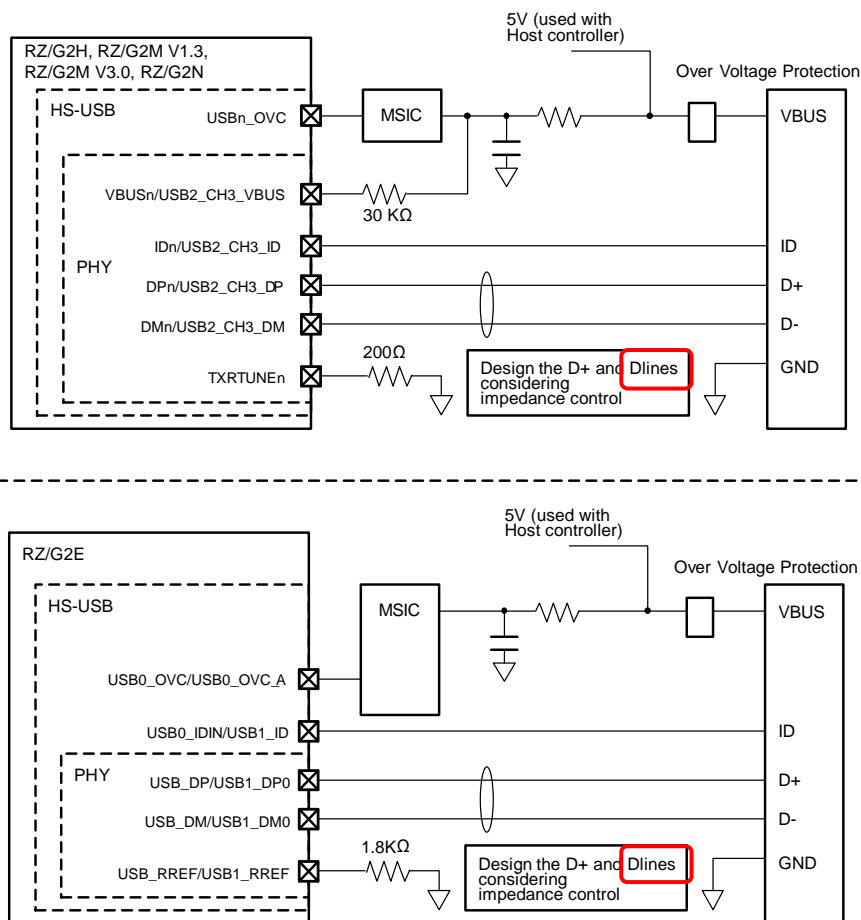
Current (from):

(3)   USB Data Bus Resistor Control

Figure 61.1 shows the connection between this module and the USB connector.

This module incorporates a pull-up resistor of the D+ signal. Specify pull-up using the DPRPU bits in SYSCFG.

Furthermore, this module controls the terminating resistors of the D+ and D- signals in high-speed operation, and the output resistors in full-speed operation. This module automatically switches the on-chip resistors after connection to the host controller detecting a reset handshake, suspended state, or resume.

When the DPRPU bit in SYSCFG is set to 0 during communication with the host controller, this module disables the pull-up resistors (or terminating resistors) of the USB data line. Therefore, the USB host can be notified of a disconnection from the device.

Figure 61.1   Connection to the USB Connector
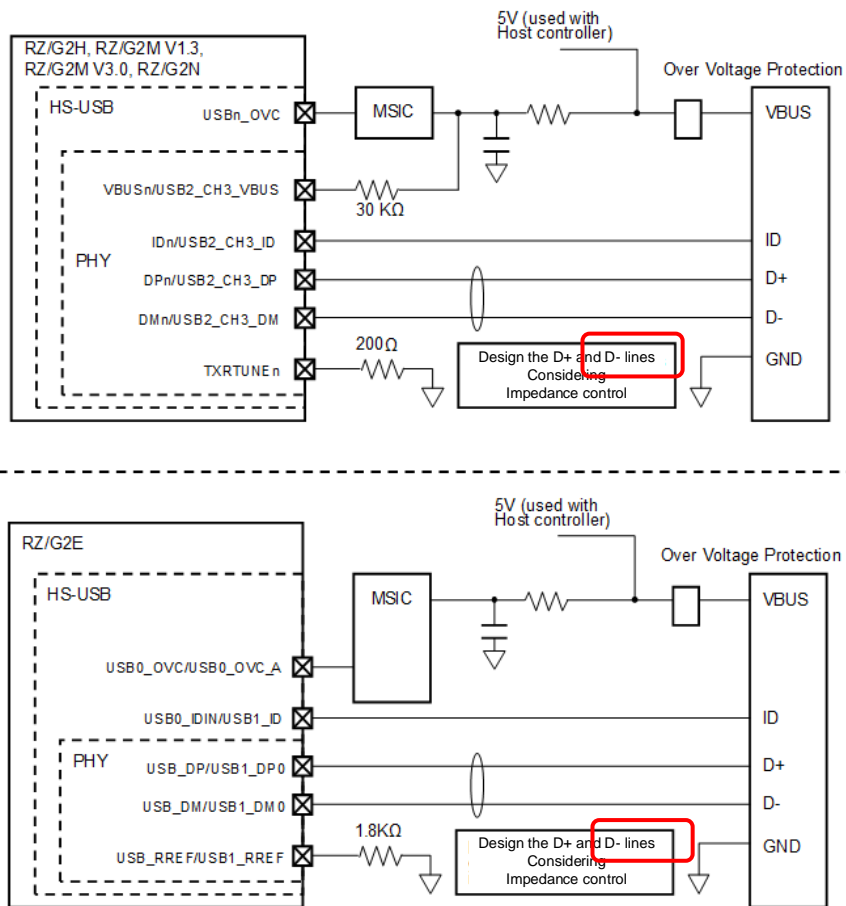
Correct (to):

(3)   USB Data Bus Resistor Control

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When the DPRPU bit in SYSCFG is set to 0 during communication with the host controller, this module disables the pull-up resistors (or terminating resistors) of the USB data line. Therefore, the USB host can be notified of a disconnection from the device.

Figure 61.2   Connection to the USB Connector

[Description]

Correction of the wrong expression.

[Reason for Correction]

General error correction

[Correction]

2.   Section 61. HS-USB, Page 61-81, 61.3.1 System Control and Oscillation Control, (4) Software reset when the USB

disconnection is detected

Current (from):

(4)   Software reset when the USB disconnection is detected

Issue a software reset of the USBHS module when the USB disconnection is detected. If the DMA interface is being used,

issue a software reset of the USB-DMAC module as well. A software reset can be issued via a register in the CPG

Whether or not the USB disconnection is detected can be determined by the VBSTS in the INTSTS0 register.

Note: USB-PHY might become inoperable to use by the instantaneous interruption of VBUS. As a result S/W on the LSI
side (driver) becomes a state of the connection, and USB-PHY becomes a state of power cutoff. It's possible to cancel
this state by putting the next way into effect by software.

1)   When detecting a bus reset or cutoff of VBUS, refer to the state bit of USB - PHY (USB_OFF bit of USBCR2
register in GPIO) and in case of USB_OFF = 1, set USB_START bit.

2)   When 1) is performed and USB - PHY is started, USB_PHY_ON interrupt occurs, so perform a soft reset to
USBHS,USB-DMAC and do the setting by which USBHS,USB-DMAC is initialization and DP pull up --, etc. by
this timing.

Correct (to):

(4)   Software reset when the USB disconnection is detected

Issue a software reset of the USBHS module when the USB disconnection is detected. If the DMA interface is being used,

issue a software reset of the USB-DMAC module as well. A software reset can be issued via a register in the CPG

Whether or not the USB disconnection is detected can be determined by the VBSTS in the INTSTS0 register.

Note: USB-PHY might become inoperable to use by the instantaneous interruption of VBUS. As a result S/W on the LSI
       side (driver) becomes a state of the connection, and USB-PHY becomes a state of power cutoff. It's possible to cancel
       this state by putting the next way into effect by software.
   1) When detecting cutoff of VBUS, refer to the VBINT and VBSTS in Interrupt Status Register 0 (INTSTS0).
   2) When 1) is detected, perform a soft reset to USBHS and USB-DMAC then initialize USBHS and USB-DMAC.

[Description]

Correction of the wrong expression.

[Reason for Correction]

General error correction

- End of Document -