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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0115A/E	Rev.	1.00
Title	RZ/G1H, G1M, G1N and G1E Additional Descriptions for AP-System Core		Information Category	Technical Notification		
Applicable Product	RZ/G Series RZ/G1H, RZ/G1M, RZ/G1N,RZ/G1E	Lot No. All lots	Reference Document	RZ/G Series, User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)		

This technical update describes document correction of RZ/G Series product.

[Summary]

Additional Descriptions for “Section 7B Advanced Power Management Unit for AP-System Core (APMU)”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G1H,

RZ/G1M,

RZ/G1N,

RZ/G1E

[Section number and title]

Section 7B. Advanced Power Management Unit for AP-System Core (APMU)

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“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 7B. APMU, Page 7B-9, 7B.3.5 Cortex-A7/Cortex-A15 Debug Resource Reset Control Register (CA7DBGRCR, CA15DBGRCR), explanation added.

Current (from):

7B.3.5 Cortex-A7/Cortex-A15 Debug Resource Reset Control Register (CA7DBGRCR, CA15DBGRCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Cortex-A7/Cortex-A15 debug resource reset control registers are 32-bit readable/writable registers of PCCU. These registers enable the reset requests derived from power-shutoff to the AP-system CPU cores in the debug mode. When you write to these registers, please modify only the target bits you want to change (read-modify-write). In the debug mode, bits 24 to 19 must be set to all 1 before the AP-system cores first resume from power-shutoff. In the normal mode (i.e. not debug mode), writing all 1 to bits 24 to 19 doesn't disturb normal operation. Therefore the same code to write these registers can be applied for both debug mode and normal mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DBGCPUREN	DBGCPU3REN	DBGCPU2REN	DBGCPU1REN	DBGCPU0REN	DBGCPUPREN	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	0	—	—	0	0	—	—	0	0	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	DBGCPUREN	0	R/W	Enable the reset request derived from power-shutoff to the circuits other than CPU cores in the debug mode. 0: Disables the reset request derived from power-shutoff to the circuits other than CPU cores in the debug mode. 1: Enables the reset request derived from power-shutoff to the circuits other than CPU cores in the debug mode.
23	DBGCPU3REN	0	R/W	[RZ/G1H]: Enable the reset request derived from power-shutoff to CPU3 in the debug mode. 0: Disables the reset request derived from power-shutoff to CPU3 in the debug mode. 1: Enables the reset request derived from power-shutoff to CPU3 in the debug mode. [RZ/G1M/N/E]: Reserved The initial value of this bit is 0. The value of this bit doesn't affect the operation of RZ/G1M/N. Therefore the write value can be either 0 or 1.

Correction (to):

7B.3.5 Cortex-A7/Cortex-A15 Debug Resource Reset Control Register (CA7DBGRCR, CA15DBGRCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Cortex-A7/Cortex-A15 debug resource reset control registers are 32-bit readable/writable registers of PCCU. These registers enable the reset requests derived from power-shutoff to the AP-system CPU cores in the debug mode. When you write to these registers, please modify only the target bits you want to change (read-modify-write). In the debug mode, bits 24 to 19 must be set to all 1 before the AP-system cores first resume from power-shutoff. In the normal mode (i.e. not debug mode), writing all 1 to bits 24 to 19 doesn't disturb normal operation. Therefore the same code to write these registers can be applied for both debug mode and normal mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DBGCPUREN	DBGCPU3REN	DBGCPU2REN	DBGCPU1REN	DBGCPU0REN	DBGCPUPREN	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	0	—	—	0	0	—	—	0	0	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	DBGCPUREN	0	R/W	Enable the reset request derived from power-shutoff to the circuits other than CPU cores. 0: Disables the reset request derived from power-shutoff to the circuits other than CPU cores. 1: Enables the reset request derived from power-shutoff to the circuits other than CPU cores. See also the explanation of these registers at the top of 7B.3.5 for note about bit 24 to 19.
23	DBGCPU3REN	0	R/W	[RZ/G1H]: Enable the reset request derived from power-shutoff to CPU3. 0: Disables the reset request derived from power-shutoff to CPU3. 1: Enables the reset request derived from power-shutoff to CPU3. See also the explanation of these registers at the top of 7B.3.5 for note about bit 24 to 19. [RZ/G1M/N/E]: Reserved The initial value of this bit is 0. The value of this bit doesn't affect the operation of RZ/G1M/N. Therefore the write value can be either 0 or 1.

22	DBGCPU2REN	0	R/W	[RZ/G1H]: Enable the reset request derived from power-shutoff to CPU2 in the debug mode. 0: Disables the reset request derived from power-shutoff to CPU2 in the debug mode. 1: Enables the reset request derived from power-shutoff to CPU2 in the debug mode. [RZ/G1M/N/E]: Reserved The initial value of this bit is 0. The value of this bit doesn't affect the operation of RZ/G1M/N. Therefore the write value can be either 0 or 1.
21	DBGCPU1REN	0	R/W	Enable the reset request derived from power-shutoff to CPU1 in the debug mode. 0: Disables the reset request derived from power-shutoff to CPU1 in the debug mode. 1: Enables the reset request derived from power-shutoff to CPU1 in the debug mode.
20	DBGCPU0REN	0	R/W	Enable the reset request derived from power-shutoff to CPU0 in the debug mode. 0: Disables the reset request derived from power-shutoff to CPU0 in the debug mode. 1: Enables the reset request derived from power-shutoff to CPU0 in the debug mode.
19	DBGCPUPREN	0	R/W	Enable the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller) in the debug mode. 0: Disables the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller) in the debug mode. 1: Enables the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller) in the debug mode.
18	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
17, 16	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

22	DBGCPU2REN	0	R/W	[RZ/G1H]: Enable the reset request derived from power-shutoff to CPU2. 0: Disables the reset request derived from power-shutoff to CPU2. 1: Enables the reset request derived from power-shutoff to CPU2. See also the explanation of these registers at the top of 7B.3.5 for note about bit 24 to 19. [RZ/G1M/N/E]: Reserved The initial value of this bit is 0. The value of this bit doesn't affect the operation of RZ/G1M/N. Therefore the write value can be either 0 or 1.
21	DBGCPU1REN	0	R/W	Enable the reset request derived from power-shutoff to CPU1. 0: Disables the reset request derived from power-shutoff to CPU1. 1: Enables the reset request derived from power-shutoff to CPU1 See also the explanation of these registers at the top of 7B.3.5 for note about bit 24 to 19.
20	DBGCPU0REN	0	R/W	Enable the reset request derived from power-shutoff to CPU0. 0: Disables the reset request derived from power-shutoff to CPU0. 1: Enables the reset request derived from power-shutoff to CPU0. See also the explanation of these registers at the top of 7B.3.5 for note about bit 24 to 19.
19	DBGCPUPREN	0	R/W	Enable the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller). 0: Disables the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller). 1: Enables the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller). See also the explanation of these registers at the top of 7B.3.5 for note about bit 24 to 19.
18	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
17, 16	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

[Description]

Descriptions that could be a cause of misunderstandings have been corrected.

[Reason for Correction]

Expression improvement

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