RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0114A/E	Rev.	1.00
Title	RZ/G1H, G1M, G1N and G1E Additional Des for AP-System Core	scriptions	Information Category	Technical Notification		
Applicable Product	RZ/G Series RZ/G1H, RZ/G1N, RZ/G1M, RZ/G1E	All lots	Reference Document	RZ/G Series, User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)		
This technica	al update describes document correction of RZ	/G Series pr	oduct.			
[Summary]						
Additional De	escriptions for "Section 09. AP-System Core"					
[Priority level	1					
Importance: '						
Urgency: "No						
[Products]						
RZ/G1H,						
RZ/G1N,						
RZ/G1M,						
RZ/G1E						
[Section num	ber and title]					
Section 09.	AP-System Core					



"This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. "

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)



[Correction]

1. Section 09. AP-System Core, Page 9-4, 9.3.1 Overview, explanation added.

Current (from):

9.3	Power-Down Mechanism	RZ/G1H	RZ/G1N
		RZ/G1M	RZ/G1E

9.3.1 Overview

The AP-System core supports the following three power-down modes.

- AP-System core power down mode (CPUs and L2 Cache shutdown: A3SM = OFF (Cortex-A15)/A2KL = OFF (Cortex-A7))
- Core standby mode (each CPU)*
- Sleep mode (clock stop, each CPU)
- L2 shutdown mode

In AP-System core power down mode, the power of the AP-System core area is shut down. This mode is intended to be used at long-time wait, and achieves the reduction of power consumption including leakage current cut-off. The system boots up from the reset vector at its return from AP-System core power down mode. For detail of the AP-system core power down control, see section 61, System Controller (SYSC).

In Core standby mode, all memories including L1 cache of the relevant CPU do not keep its contents, but the power of the SRAM of level 2 cache is supplied to keep its contents.

In L2 shutdown mode, all power of CPUs and L2 is shut down. So contents of both L1s and L2 are not to be retained.

For details of Core standby mode and L2 shutdown mode, see section 7B, Advanced Power Management Unit for AP-System Core (APMU).

Note: * In RZ/G1E case, if each CPU enter into the core standby mode, the clock supply for each CPU is stopped even if CPU core is always supplied power. After the power-on reset, the CPU other than the master CPU is in the core standby mode. When using the CPU in the core standby mode, follow the power-on sequence in order to start supply of the clock.



Correction (to):

9.3Power-Down MechanismRZ/G1HRZ/G1NRZ/G1MRZ/G1E
9.3.1 Overview
The AP-System core supports the following three power-down modes.
AP-System core power down mode
(CPUs and L2 Cache shutdown: A3SM = OFF (Cortex-A15)/A2KL = OFF (Cortex-A7))
 Core standby mode (each CPU)* Sleep mode (clock stop, each CPU)
 L2 shutdown mode
In AP-System core power down mode, the power of the AP-System core area is shut down. This mode is intended to be used
at long-time wait, and achieves the reduction of power consumption including leakage current cut-off. The system boots up
from the reset vector at its return from AP-System core power down mode. For detail of the AP-system core power down
control, see section 61, System Controller (SYSC).
In Core standby mode, all memories including L1 cache of the relevant CPU do not keep its contents, but the power of the
SRAM of level 2 cache is supplied to keep its contents.
In L2 shutdown mode, all power of CPUs and L2 is shut down. So contents of both L1s and L2 are not to be retained.
For details of Core standby mode and L2 shutdown mode, see section 7B, Advanced Power Management Unit for AP-System
Core (APMU).
For details of the power-on sequence (sequence of activation), see (10), Restoring the Power Supply to a CPU Other than the
Master Boot Device, in section Appendix B, Sequence of Activation for Second RZ/G Series Products.
Note: * In RZ/G1E case, if each CPU enter into the core standby mode, the clock supply for each CPU is stopped even if CPU core is always supplied power. After the power-on reset, the CPU other than the master CPU is in the core standby mode. When using the CPU in the core standby mode, follow the power-on sequence in order to start supply of the clock.
[Description]
Since there is an explanation for Power-up sequence in Appendix B, a reference to Appendix B has been added.
[Reason for Correction]

Lack of explanation

- End of Document -

