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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A027A/E	Rev.	1.00
Title	RZ/G Series User's Manual:Hardware Correction (EthernetAVB)		Information Category	Technical Notification		
Applicable Product	RZ/G Series RZ/G1H, M, N, and E	Lot No. All lots	Reference Document	RZ/G Series User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)		

This technical update describes document correction for RZ/G Series.

[Summary]

Correction of Register description about Bit2 and Bit3 in ECSIPR using EthernetAVB

[Products]

RZ/G1H, M, N, and E

[Note]

There is no specification change (Definition is cleared).

[Additional Explanation]

(Following gray highlighted parts (abcd) are corrected or newly added.)

Section 37A EthernetAVB

Description for updated registers

37A.2.51 E-MAC Interrupt Permission Register (ECSIPR)

Current (from):

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MPDIP	ICDIP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	MPDIP	0	R/W	Magic Packet™ Detect Interrupt Enable Setting this bit to 1 selects interrupt generation on setting of the Magic PacketTM detection bit (ECSR.MPD) in the E-MAC status register to 1. 0: Interrupts on setting of the MPD bit is disabled. 1: Interrupts on setting of the MPD bit is enabled.
0	ICDIP	0	R/W	Illegal Carrier Detect Interrupt Enable Setting this bit to 1 selects interrupt generation on setting of the illegal carrier detection bit (ECSR.ICD) in the E-MAC status register to 1. 0: Interrupts on setting of the ICD bit is disabled. 1: Interrupt on setting of the ICD bit is enabled.

Correction (to):

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PHYIM	LINKIM	MPDIP	ICDIP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
3	PHYIM	0	R/W	PHY Interrupt Mask Setting this bit to 1 selects interrupt generation on setting of the PHY interrupt terminal state bit (ECSR. PHYI) in the E-MAC status register to 1. 0: Interrupts on setting of the PHYI bit is disabled. 1: Interrupts on setting of the PHYI bit is enabled.
2	LINKIM	0	R/W	LINK Interrupt Mask Setting this bit to 1 selects interrupt generation on setting of the Link signal change bit (ECSR. LCHNG) in the E-MAC status register to 1. 0: Interrupts on setting of the LCHNG bit is disabled. 1: Interrupts on setting of the LCHNG bit is enabled.
1	MPDIP	0	R/W	Magic Packet™ Detect Interrupt Enable Setting this bit to 1 selects interrupt generation on setting of the Magic PacketTM detection bit (ECSR.MPD) in the E-MAC status register to 1. 0: Interrupts on setting of the MPD bit is disabled. 1: Interrupts on setting of the MPD bit is enabled.
0	ICDIP	0	R/W	Illegal Carrier Detect Interrupt Enable Setting this bit to 1 selects interrupt generation on setting of the illegal carrier detection bit (ECSR.ICD) in the E-MAC status register to 1. 0: Interrupts on setting of the ICD bit is disabled. 1: Interrupt on setting of the ICD bit is enabled.

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