Date: May 30, 2017

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A027A/E	Rev.	1.00		
Title	RZ/G Series User's Manual:Hardware Correct (EthernetAVB)	ction	Information Category	Technical Notification				
		Lot No.						
Applicable Product	RZ/G Series RZ/G1H, M, N, and E	All lots	Reference Document	RZ/G Series User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)				

This technical update describes document correction for RZ/G Series.

[Summary]

Correction of Register description about Bit2 and Bit3 in ECSIPR using EthernetAVB

[Products]

RZ/G1H, M, N, and E

[Note]

There is no specification change (Definition is cleared).

[Additional Explanation]

(Following gray highlighted parts (abcd) are corrected or newly added.)

Section 37A EthernetAVB

Description for updated registers

37A.2.51 E-MAC Interrupt Permission Register (ECSIPR)

Current (from):

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	_	_	_	_	_	_	_	ı	1	-	-	-	ı	_	_
Initial value: R/W:	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		_	_	_	_	_	_	_	_	_	_	_	_	_	MPDIP	ICDIP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	Dit I	Name	In	itial Va	duo	R/W	Dose	cription								
DIL	ו זום	vaine	III	iiliai Va	iiue	FK/ VV	Desc	hiptioi	1							

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	_	All 0	R/W	Reserved
				These bits are read as 0. The write value should be 0.

Bit	Bit I	Name	In	itial Va	alue	R/W	Desc	cription	1									
1	MP	DIP	0			R/W	Mag	ic Pack	et™ De	etect In	terrupt	Enable)					
							Magic Packet [™] Detect Interrupt Enable Setting this bit to 1 selects interrupt generation on setting of the Magic PacketTM detection bit (ECSR.MPD) in the E-MAC status register to 1.											
							0: In	terrupts	on set	ting of	the MP	D bit is	disable	ed.				
								-		_			enable					
)	ICDIP 0 R/W					Illega	al Carri	er Dete	ct Inter	rupt Er	nable							
			•										eration in the E					
							0: In	terrupts	on set	ting of	the ICE	bit is	disable	d.				
								-		_			nabled.					
Correction	(to):																	
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_		
nitial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	_	_	_	_	_	_	_	_	_	_	_	_	PHYIM	LINKIM	MPDIP	ICDIP		
nitial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Bit	Bit I	Name	In	itial Va	alue	R/W	Description											
31 to 4	_		Α	II 0		R/W	R/W Reserved											
					Thes	These bits are read as 0. The write value should be 0.												
3	PHYIM 0				R/W	PHY Interrupt Mask												
							Setting this bit to 1 selects interrupt generation on setting of the PHY interrupt terminal state bit (ECSR. PHYI) in the E-MAC status register to 1.											
							_			tina of	the PH	YI hit is	s disabl	ed				
							0: Interrupts on setting of the PHYI bit is disabled.1: Interrupts on setting of the PHYI bit is enabled.											
2	LINI	LINKIM 0 R/W				LINK Interrupt Mask												
-	LINKIN O IVV				Setting this bit to 1 selects interrupt generation on setting of the Link signal change bit (ECSR. LCHNG) in the E-MAC status register to 1.													
							0: In	terrupts	on set	ting of	the LC	HNG bi	it is disa	abled.				
							1: Interrupts on setting of the LCHNG bit is enabled.											
1	MPI)IP	0			R/W	Magic Packet [™] Detect Interrupt Enable											
							Setting this bit to 1 selects interrupt generation on setting of the Magic PacketTM detection bit (ECSR.MPD) in the E-MAC status register to 1.											
							0: Interrupts on setting of the MPD bit is disabled.											
								1: Interrupts on setting of the MPD bit is enabled.										
							1: In	torrapte			Illegal Carrier Detect Interrupt Enable							
0	ICD	IP	0			R/W					rupt Er	nable						
0	ICD	IP	0			R/W	Illega Setti	al Carri	er Dete	ct Inter	interru	ıpt gen	eration in the E	on sett				
0	ICD	IP	0			R/W	Illega Setti illega to 1.	al Carri ng this al carrie	er Dete bit to 1 er detec	ct Inter selects tion bit	interro (ECSF	upt gen R.ICD) i		on sett -MAC s				



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RENESAS TECHNICAL UPDATE	IN-RZ"-AUZ/A/E	Date: May 30, 2017
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