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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A010A/E	Rev.	1.00
Title	RZ/A1 Series: Notes about reset of debug interface		Information Category	Technical Notification		
Applicable Product	See following	Lot No. All	Reference Document	See following		

In RZ/A1H Group, RZ/A1M Group, and RZ/A1L Group, it is found that this LSI can not be released from reset state successfully if rise time of RES and TRST pin is very long.

Notes about rise time of RES and TRST pin are as follows.

According to this update, relevant manuals will be revised.

Applicable products and relevant documents

Applicable products		Relevant documents	Rev.	Document number
series	Group			
RZ/A	RZ/A1H, RZ/A1M	RZ/A1H Group, RZ/A1M Group User's Manual: Hardware	Rev 2.00	R01UH0403EJ0200
	RZ/A1L	RZ/A1L Group User's Manual: Hardware	Rev 2.00	R01UH0437EJ0200

[1] Condition

(1) In case that TRST pin and RES pin are controlled by same signal, if rise time of input signal of RES pin is very long.

(2) In case that TRST pin and RES pin are controlled by separate signal, if input signal of TRST pin rise after rise of input signal of RES pin.

[2] Phenomenon

Usually, transition from reset state to program execution state is done by rise of RES pin, but if RES and TRST pin condition is met above conditions, properly transition from reset state to program execution state is not done and might be dead-lock.

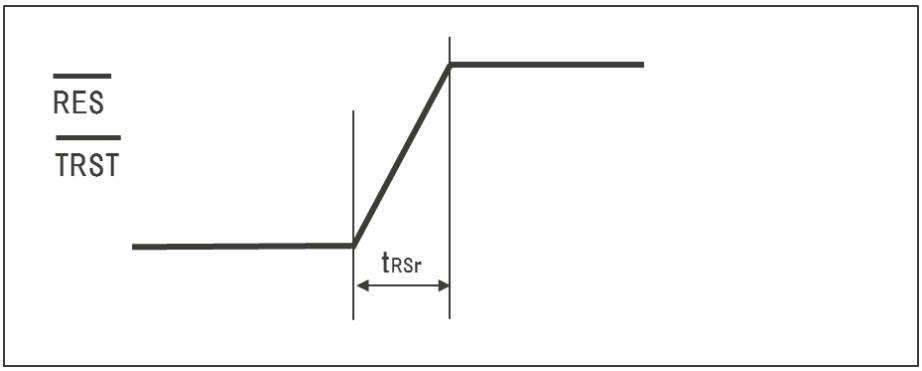
[3] Workaround

Please satisfy constraints of rise time of RES pin, or negate hold time of RES pin described in "[4] detail of constraints" in the next page.

[4] Detail of constraints

(1) When the same signal is controlling the TRST and RES pins.

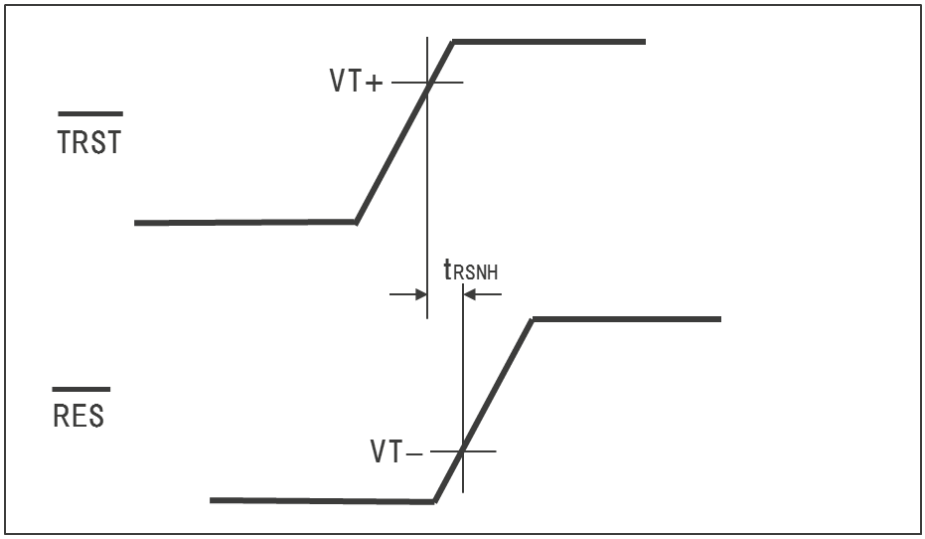
Please satisfy “RES input rise time (t_{RSr})”.



Item	Symbol	Min	Max	Unit
RES input rise time	t_{RSr}	—	500	μs

(2) When different signals are controlling the TRST and RES pins.

Please satisfy “RES negate hold time (t_{RSNH})”.



Item	Symbol	Min	Max	Unit
RES negate hold time	t_{RSNH}	0	—	ns

VT+ and VT- voltage, please refer to the User’s Manual Table 59.2 DC Characteristics (3).
(For RZ/A1L Group, please refer to Table 45.2 DC Characteristics (3).)

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