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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0103A/E	Rev.	1.00
Title	RZ/A Series: Notes about capture address and capture horizontal size of Capture Engine Unit		Information Category	Technical Notification		
Applicable Product	See following	Lot No. All	Reference Document	See following		

In the following applicable products, a bug about capture address and capture horizontal size of Capture Engine Unit (CEU) is found.

The detail of bug is shown in bellow. According to this update, relevant manuals will be revised.

Applicable products and relevant documents

Applicable products		Relevant documents	Rev.	Document number
series	Group			
RZ/A	RZ/A1H, RZ/A1M	RZ/A1H Group, RZ/A1M Group User's Manual: Hardware	Rev.6.00	R01UH0403EJ0600
	RZ/A1L, RZ/A1LU, RZ/A1LC	RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group User's Manual: Hardware	Rev.6.00	R01UH0437EJ0600
	RZ/A2M	RZ/A2M Group User's Manual: Hardware	Rev.4.00	R01UH0746JJ0600

1. Error occurrence condition

When CEU writes capture data to destinations other than On-chip RAM and sets the capture address or capture horizontal width to 4-byte units instead of 8-byte units.

2. Error phenomenon

4-byte writes to H'XXXX_XXX4 or H'XXXX_XXXC address are not performed properly.

3. Workarounds

When CEU writes capture data to destinations other than On-chip RAM, set the capture address and capture horizontal width to 8-byte units.

In this technical update, RZ/A1H Group and RZ/A1M Group is used as an example and note for set the capture address and capture horizontal width to 8-byte units is written.

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Table 46.1 Functional Overview of CEU Note of Connectable camera

Classification	Item	Function	Description	Note
Connectable camera	Size	・ ・ ・	・ ・ ・	Horizontal: 4-pixel units* Vertical: 4-line units Note *: When writing to other than On-chip RAM, 8-pixel units ・ ・ ・

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46.4.6 Capture Interface Width Register (CAPWR)

Description of HWDTH[12:0] bit

Bit	Bit Name	Initial Value	R/W	Description
12 to 10	HWDTH[12:1] HWDTH[0]	H'0000	R/W R	These bits specify the horizontal capture period. These bits specify the number of cycles to be captured from the location specified by the HOFST bits. Figure 46.22 shows the timing when the horizontal blanking period is 0. The CEU captures for only the number of cycles specified by these bits in the horizontal direction. Make a similar setting for data synchronous fetch. The maximum value to be set is as follows: ・ 8-bit interface Image capture (8-cycle units*1) : 5,120 cycles (2,560 pixels) Data synchronous fetch (4-cycle units*2) : 2,560 cycles (2,560 bytes) ・ 1 6-bit interface Image capture (4-cycle units*2) : 2,560 cycles (2,560 pixels) Data synchronous fetch (2-cycle units*3) : 1,280 cycles (2,560 bytes) Note: In data synchronous fetch mode, set CFSZR and CDWDR according to the values set in this register. For details, see the descriptions on CFSZR and CDWDR. Note *1: When writing to other than On-chip RAM, 16-cycle units Note *2: When writing to other than On-chip RAM, 8-cycle units Note *3: When writing to other than On-chip RAM, 4-cycle units

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Table 46.6 Unit for Setting Fetch (Capture) Cycle Width

Interface	Vertical Direction		Horizontal Direction	
	Image Capture	Data Synchronous Fetch	Image Capture	Data Synchronous Fetch
8-bit interface	4HD	4HD	8 cycles*1	4 cycles*2
16-bit interface	4HD	4HD	4 cycles*2	2 cycles*3

Note *1: When writing to other than On-chip RAM, 16 cycles

Note *2: When writing to other than On-chip RAM, 8 cycles

Note *3: When writing to other than On-chip RAM, 4 cycles

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46.4.11 Capture Filter Size Clip Register (CFSZR)

Description of HFCLP[11:0] bit

Bit	Bit Name	Initial Value	R/W	Description
11 to 10	HFCLP[12:1] HFCLP[0]	H'000	R/W R	These bits specify the horizontal clipping value of the filter output size (4-pixel units*). Note *: When writing to other than On-chip RAM, 8-pixel units

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46.4.12 Capture Destination Width Register (CDWDR)

Description of CHDW[12:0] bit

Bit	Bit Name	Initial Value	R/W	Description
12 to 2 1 to 0	CHDW[12:2] CHDW[1:0]	H'0000	R/W R	These bits specify the horizontal image size in the memory area where the captured image is to be stored (4-byte units*). The image data captured by the CEU is stored in the memory. If the right end of the captured image does not match the horizontal image size in the memory area as shown in Figure 46.34, some addresses must be skipped at the right end of the image when storing the captured image. Therefore, the horizontal image size in the memory area where the captured image is to be stored must be set in these bits. The maximum value to be set is 8188 bytes (8188 pixels). In data synchronous fetch mode, set as follows: 8-bit interface: CHDW = CAPWR.HWDTH 16-bit interface: CHDW = CAPWR.HWDTH × 2 Note *: When writing to other than On-chip RAM, 8-byte units

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46.4.13 Capture Data Address Y Register (CDAYR)

Description of CAYR[31:0] bit

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1 to 0	CAYR[12:2] CAYR[1:0]	H'0000	R/W R	· Frame image capture: These bits set the address for storing the Y (luminance) component data of the captured data (4-pixel units*1). · One-field image capture: These bits set the address for storing the Y (luminance) component data of the captured data (4-pixel units*1). · Both-field image capture: These bits set the address for storing the Y (luminance) component data of the captured top-field data (4-pixel units*1). · Data fetch: These bits set the address for storing data (4-byte units*2). · Data enable fetch bundle write: These bits set the address for storing data (32-byte units). Note *1: When writing to other than On-chip RAM, 8-pixel units Note *2: When writing to other than On-chip RAM, 8-byte units

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46.4.14 Capture Data Address C Register (CDACR)

Description of CACR[31:0] bit

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1 to 0	CACR[12:2] CACR[1:0]	H'0000	R/W R	· Frame image capture: These bits set the address for storing the C (chrominance) component data of the captured data (4-pixel units*). · One-field image capture: These bits set the address for storing the C (chrominance) component data of the captured data (4-pixel units*). · Both-field image capture: These bits set the address for storing the C (chrominance) component Note *: When writing to other than On-chip RAM, 8-pixel units

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46.4.15 Capture Data Bottom-Field Address Y Register (CDBYR)

Description of CBYR[31:0] bit

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1 to 0	CBYR[12:2] CBYR[1:0]	H'0000	R/W R	These bits set the address for storing the Y (luminance) component data of the captured bottom-field data (4-pixel units*). Note *: When writing to other than On-chip RAM, 8-pixel units

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46.4.16 Capture Data Bottom-Field Address C Register (CDBCR)

Description of CBCR[31:0] bit

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1 to 0	CBCR[12:2] CBCR[1:0]	H'0000	R/W R	These bits set the address for storing the C (chrominance) component data of the captured bottom-field data (4-pixel units*). Note *: When writing to other than On-chip RAM, 8-pixel units

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46.4.25 Capture Data Address Y Register 2 (CDAYR2)

Description of CAYR2[31:0] bit

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1 to 0	CAYR2[12:2] CAYR2[1:0]	H'0000	R/W R	· Frame image capture: These bits set the address for storing the Y component data of the captured data (4-pixel units*1). · One-field image capture: These bits set the address for storing the Y component data of the captured data (4-pixel units*1). · Both-field image capture: These bits set the address for storing the Y component data of the captured top-field data (4-pixel units*1). · Data synchronous fetch: These bits set the address for storing data (4-byte units*2). · Dana enable fetch: These bits set the address for storing data (32-byte units). Note *1: When writing to other than On-chip RAM, 8-pixel units Note *2: When writing to other than On-chip RAM, 8-byte units

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46.4.26 Capture Data Address C Register 2 (CDACR2)

Description of CACR2[31:0] bit

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1 to 0	CACR2[12:2] CACR2[1:0]	H'0000	R/W R	· Frame image capture: These bits set the address for storing the C component data of the captured data (4-pixel units*). · One-field image capture: These bits set the address for storing the C component data of the captured data (4-pixel units*). · Both-field image capture: These bits set the address for storing the C component data of the captured top-field data (4-pixel units*). Note *: When writing to other than On-chip RAM, 8-pixel units

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46.4.27 Capture Data Bottom-Field Address Y Register 2 (CDBYR2)

Description of CBYR2[31:0] bit

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1 to 0	CBYR2[12:2] CBYR2[1:0]	H'0000	R/W R	These bits set the address for storing the Y component data of the captured bottom-field data (4-pixel units*). Note *: When writing to other than On-chip RAM, 8-pixel units

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46.4.28 Capture Data Bottom-Field Address C Register 2 (CDBCR2)

Description of CBCR[31:0] bit

Bit	Bit Name	Initial Value	R/W	Description
31 to 2 1 to 0	CBCR[12:2] CBCR[1:0]	H'0000	R/W R	These bits set the address for storing the C component data of the captured bottom-field data (4-pixel units*). Note *: When writing to other than On-chip RAM, 8-pixel units

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Table 46.11 Restrictions on CEU Input/Output Functions

Item	Restriction
External module interface	The capture horizontal size in image capture must be specified as follows: 8-bit interface: 8-cycle units*1 16-bit interface: 4-cycle units*2 Note *1: When writing to other than On-chip RAM, 16-cycle units Note *2: When writing to other than On-chip RAM, 8-cycle units
	The capture horizontal size in data fetch must be specified as follows: 8-bit interface: 4-cycle units*1 16-bit interface: 2-cycle units*2 Note *1: When writing to other than On-chip RAM, 8-cycle units Note *2: When writing to other than On-chip RAM, 4-cycle units
Memory output	The output address must be specified in 32-bit units*. Note *: When writing to other than On-chip RAM, 64-bit units
	The horizontal size of the destination image (memory) must be specified in 4-pixel units*. Note *: When writing to other than On-chip RAM, 8-pixel units
	The number of horizontal output pixels (= horizontal clipping size) must be specified in 4-pixel units*. Note *: When writing to other than On-chip RAM, 8-pixel units

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