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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A039B/E	Rev.	1.00
Title	RL78/I1B Restriction		Information Category	Technical Notification		
Applicable Product	RL78/I1B Group ：R5F10Mxx	Lot No. All Lots	Reference Document	RL78/I1B User's Manual Hardware Rev.2.00 R01UH0407EJ0200 (Mar 19. 2014)		

The update below applies to the battery backup function in the above mentioned Applicable

List of Updates to be added in this notification

Item	Updates that are added in this notification.	Products.	Corresponding page
1.1	Update of the battery backup function	All	p.2-p.6

Revision History

Revision history of RL78/I1B updates

Document Number	Date issued	Description
TN-RL*-A039B/E	February 16, 2016	First edition issued List of usage update: No. 1.1 (this document)

1. Update that are added in this notification

1.1. Update of the battery backup function

1.1.1. On the occurrence condition

The update applies when all cases below 1) ~ 3) match

1) Battery backup function power switching operation enabled (VBATEN=1).
2) Internal VDD power switching is performed by hardware according to VDD pin voltage level (VBATSEL=0).
3) At VDD → VBAT power switching in the case of VDD pin voltage < power switching detection voltage ($V_{DETBAT1}$) or at VBAT → VDD power switching in the case of VDD pin voltage ≧ power switching detection voltage ($V_{DETBAT2}$).

1.1.2. Detail of the update

At internal VDD power switching, because of the sharp change of internal VDD, the frequency of high-speed on-chip oscillator clock (f_{IH}) varies or stops in certain period of time (approximately 10us) and Table 1 shows the influence of each peripheral operation.

Figure 1-1 Occurrence Condition (VBATEN = 1, VBATSEL = 0)

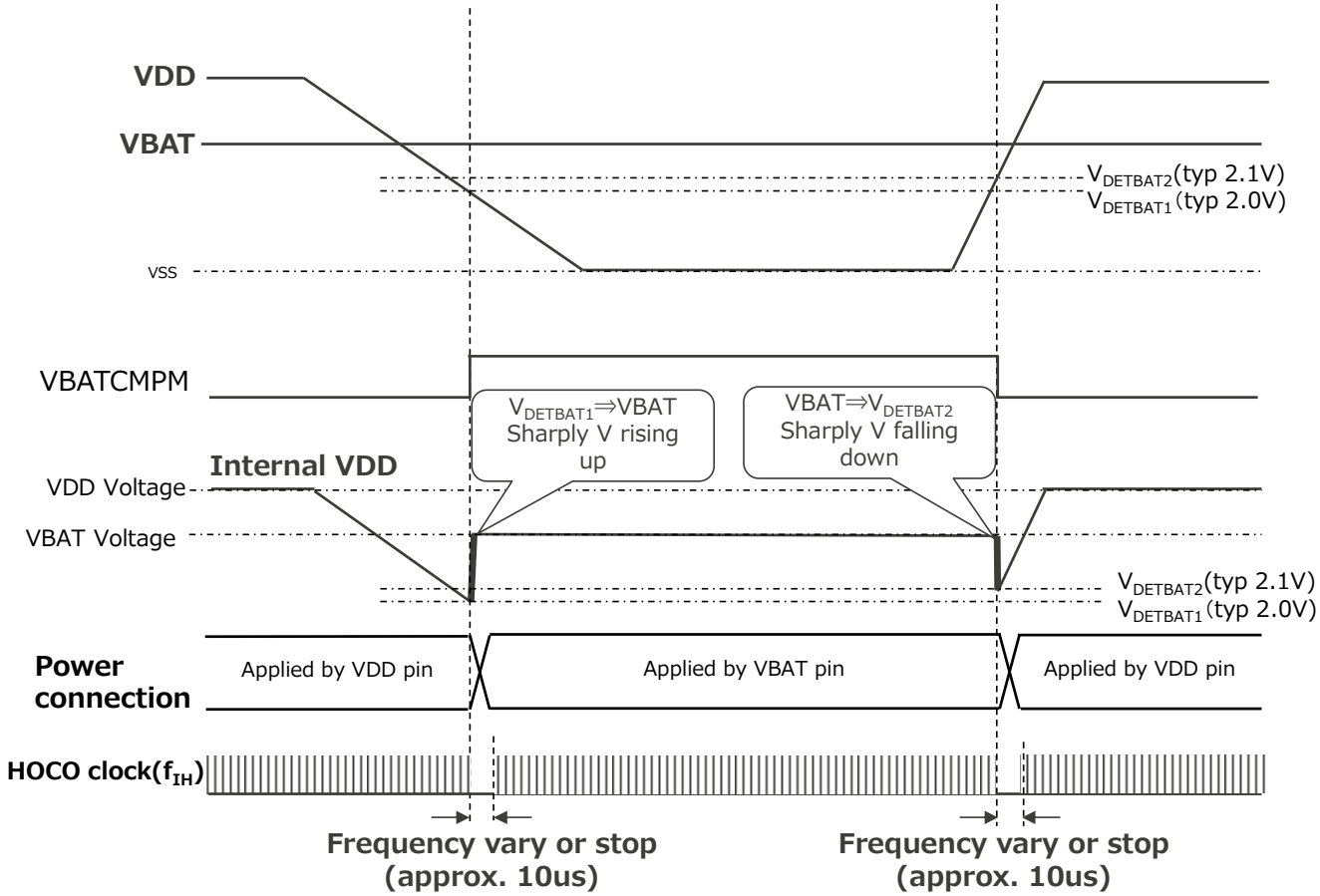


Table 1. Influence of each peripheral operation (1/2)

Item \ CPU operation clock	CPU operation on High-speed on-chip oscillator clock (f_{IH})			CPU operation on below clock ・X1 Clock（f_X） ・External Main SystemClock (f_{EX}) ・XT1 Clock（f_{XT}） ・Externa l Subsystem clock（f_{EXS}）
	CPU Operation	HALT Mode	STOP Mode	
System Clock				
Main system clock f_{IH}	Frequency vary or stop in certain period		No influence	Operation prohibited
Main system clock f_X, f_{EX}	Operation prohibited		No influence	
Subsystem Clock f_{XT}, f_{EXS}, f_{IL}	No influence			
CPU, Code Flash Memory, RAM	Instruction execution period varies or stops in certain period	No influence	No influence	
Port (latch)	No influence			
Timer Array Unit	In timer operation, as the frequency of timer operation clock varies or stops in certain period, timer count error occurs.		No influence	
Real Timer Clock 2	No influence			
Subsystem Frequency measurement circuit	Operation prohibited		No influence	
High-speed on-chip oscillator clock frequency correction function	High-speed on-chip oscillator clock frequency varies but there is no influence on correction result.		Operation prohibited	
Oscillation Stop Detection, Battery Backup Function, 12-bit Interval Timer, 8-bit Interval Timer, Watchdog timer	No influence			
Clock output/buzzer Output	There is no influence if subsystem clock is selected. Output frequency varies or stops in certain period if main system clock is selected.		No influence	
A/D Converter, ΔΣA/D converter	Because of the change of sampling frequency in certain period, there may be the error in analog conversion result.		No influence	
Temperature sensor2, Comparator	No influence			
Serial Array Unit (SAU)	Communication clock varies or stops. At UART communication and CSI master transmission/ Reception, because of communication clock frequency vary of stop, communication error may occur. At simple I^2C master communication and CSI slave transmission/ Reception, communication error do not occur.		No influence	
IrDA	Because of communication clock frequency vary of stop, communication error may occur.			
Serial Interface (IICA)	Because of communication clock frequency vary of stop, at slave communication, communication error may occur. At master communication, communication error does not occur.			

Table 1. Influence of each peripheral operation (2/2)

CPU operation clock / Item		CPU operation on High-speed on-chip oscillator clock (f_{IH})			CPU operation on below clock ・X1 Clock（f_X） ・External Main System Clock (f_{EX}) ・XT1 Clock（f_{XT}） ・External Subsystem clock（f_{EXS}）
		CPU Operation	HALT Mode	STOP Mode	
LCD Controller/ Driver		No influence			
Data Transfer Controller(DTC)		Transfer clock varies or stops in certain period.			No influence
Power-on-reset function		No influence			
Voltage Detection Function					
External Interrupt		Interrupt is acceptable but suspends in certain period			No influence
CRC operation function	High-speed CRC	No influence			
	General-purpose CRC				
RAM parity error detection function					
RAM guard function					
SFR guard function					
Illegal-memory access detection function					

1.1.3. Software Measure

・Detecting AC off by external circuit or by voltage detection function (LVD), stopping high-speed on-chip oscillator clock (f_{IH}) operation by executing STOP or transiting to subsystem clock operation before the internal VDD switching VDD→VBAT.

・At VBAT selection, please use STOP mode or subsystem clock operation or subsystem clock HALT mode. Note 1

Note 1. In the case of HS (high-speed main), using power switching detection interrupt (INTVBAT) to release STOP is prohibited as per recommendation from User Manual due to HS Mode Voltage requirements.

Figure 1-2 ~ Figure 1-5 show the software setting sequence by using Voltage detection interrupt (INTLVI) for AC off detection, power switching detection interrupt (INTVBAT) for AC on detection.

Figure 1-2 Power switching operation by using subsystem clock (HS, LS mode)

(VBATEN = 1, VBATSEL = 0)

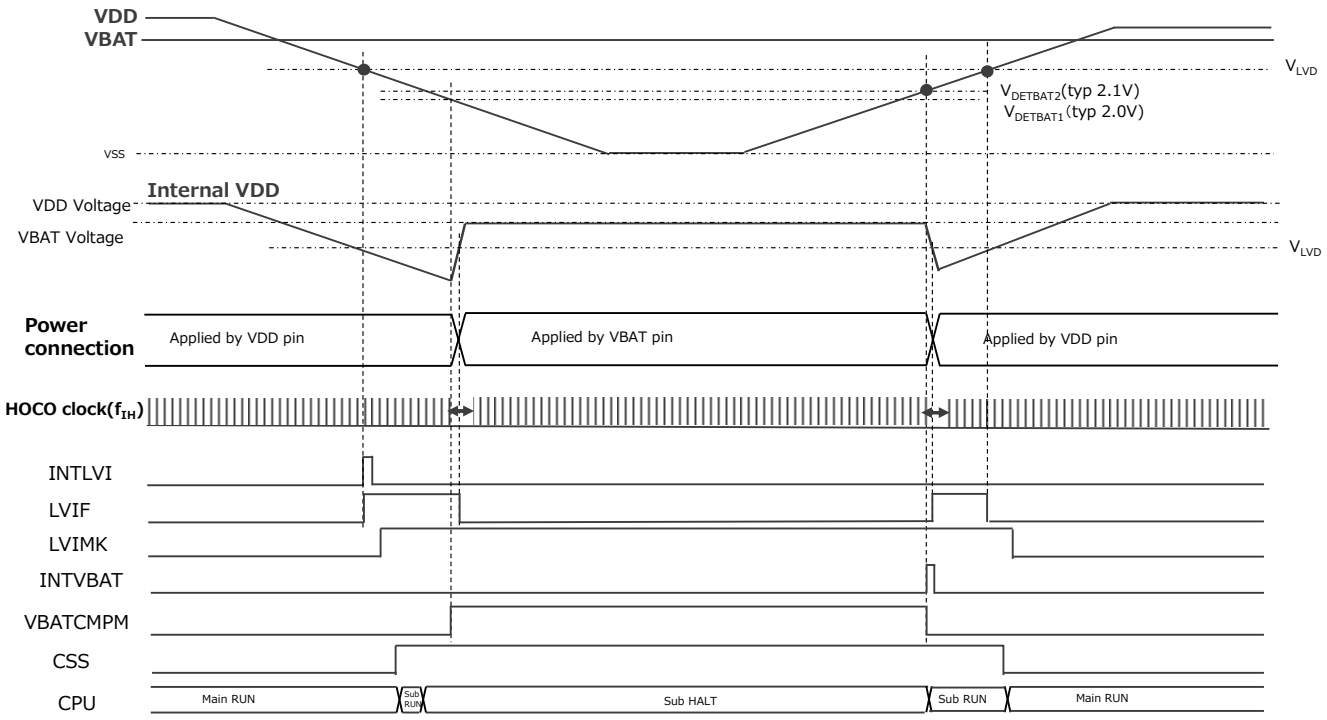


Figure 1-3 Software setting sequence (HS, LS mode)

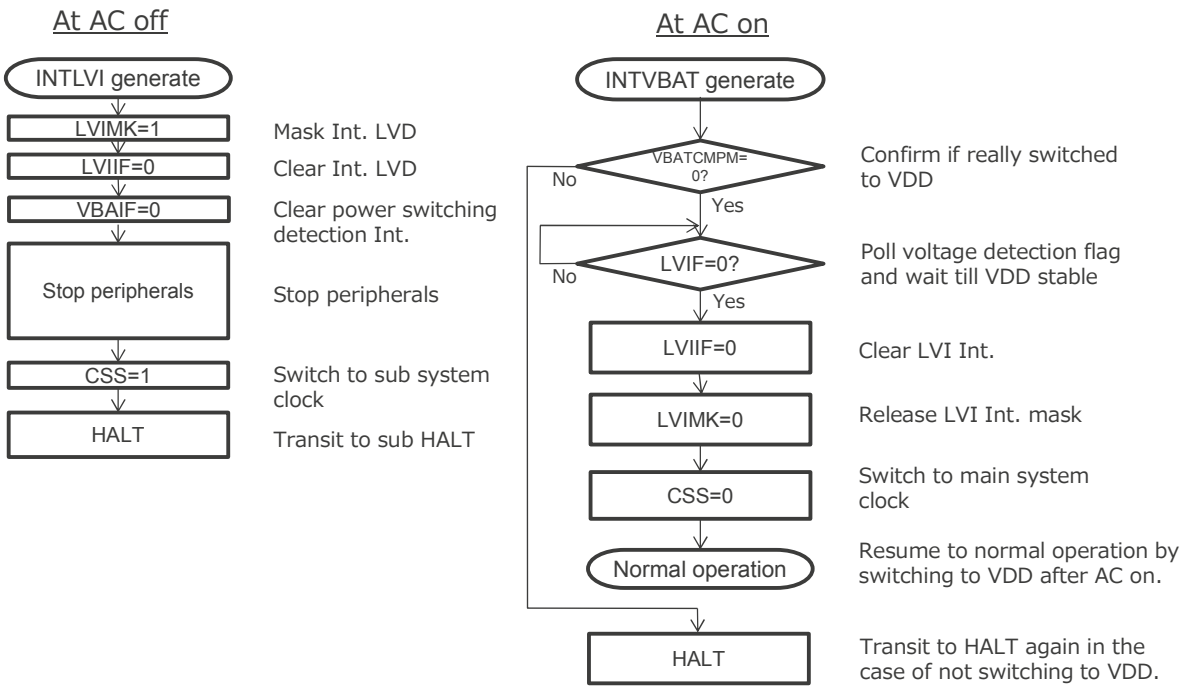


Figure 1-4 Power switching operation by using STOP (LS mode)

(VBATEN = 1, VBATSEL = 0)

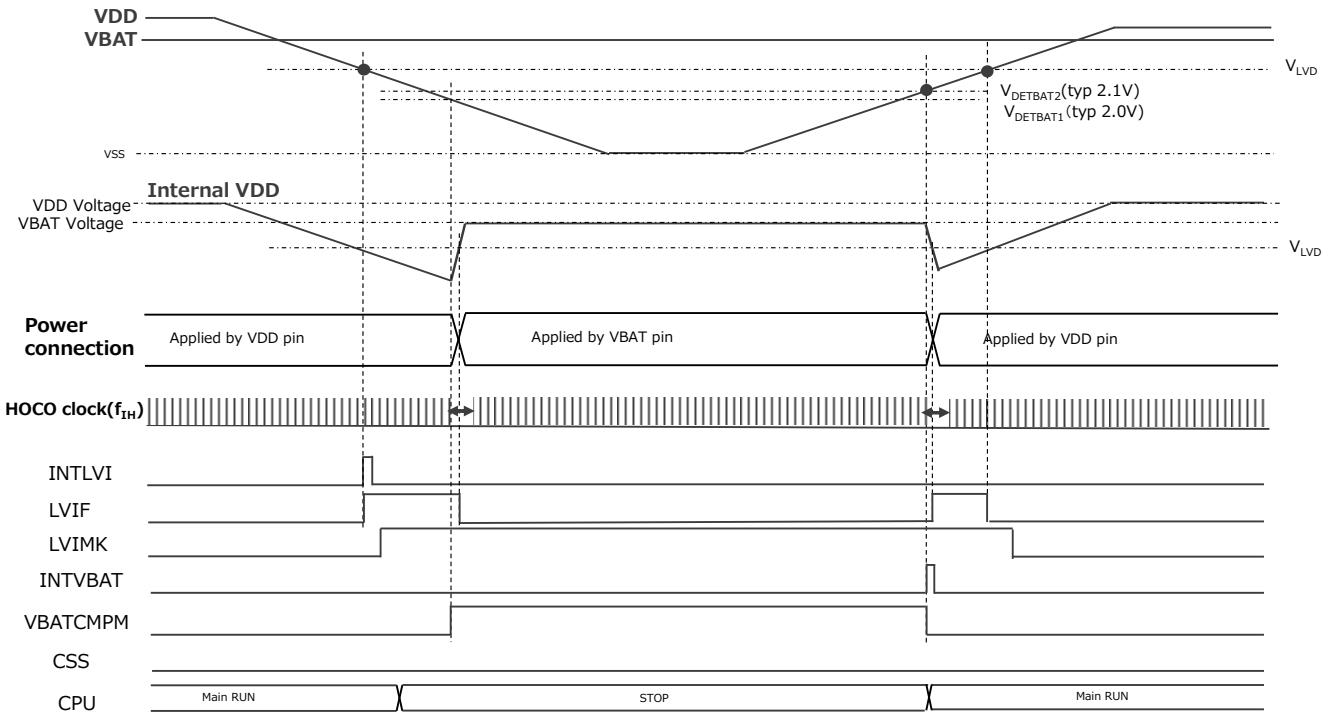
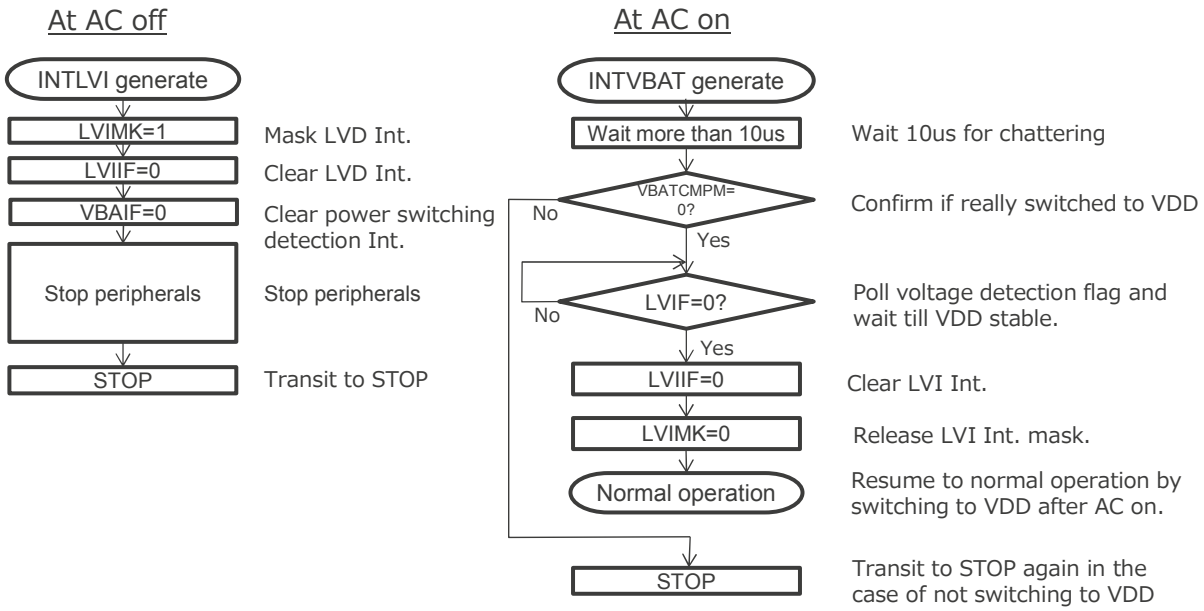


Figure 1.5 Software setting sequence (LS mode)



1.1.4 Improvement Plan

Please follow the battery backup function usage as mentioned in this update.

Renesas will add software measurement in user's manual in next edition.