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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A065A/E	Rev.	1.00
Title	RL78/G1H Direction of use		Information Category	Technical Notification		
Applicable Product	RL78/G1H R5F11Fxxx	Lot No. All lots	Reference Document	RL78/G1H User's Manual: Hardware Rev.1.10 R01UH0575EJ0110 (Jan 2016)		

This document describes correction of errors in the RL78/G1H User's Manual: Hardware Rev.1.10 (R01UH0575EJ0110).

Corrections

Applicable Item	Applicable Page	Contents
(4) GPIO0/CLKOUT, GPIO1/ANTSELOUT0, GPIO2/ANTSELOUT1, GPIO3, GPIO4/ANTSW	Page 546	Function restriction
(2) RF reference clock output	Page 551	Function restriction
Table 18 - 15 Function State in Each RF Mode	Page 663	Function restriction

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items		Pages in this document for corrections
	Item	R01UH0575JJ0110	
1	Function restrictions of clock output (CLKOUT) have been added.	Page 546	Page 3
2	Function restrictions concerning the divided clock of RF reference clock.	Page 551	Page 4
3	Function restrictions concerning CLKOUT of the function states in RF Transmission and RF Reception	Page 663	Page 5

Incorrect: ~~Strike-through~~, Correct: **Bold**

Revision History

RL78/G1H User's Manual: Hardware Rev.1.10 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A065A/E	Oct. 17, 2016	First edition issued No.1 to 3 in corrections (This notice)

1. (4) GPIO0/CLKOUT, GPIO1/ANTSELOUT0, GPIO2/ANTSELOUT1, GPIO3, GPIO4/ANTSW (Page 546)

Incorrect:

(4) GPIO0/CLKOUT, GPIO1/ANTSELOUT0, GPIO2/ANTSELOUT1, GPIO3, GPIO4/ANTSW

These are 5-bit I/O port pins.

GPIO0 pin also provides the clock output (CLKOUT) function, and the default is GPIO0 pin.

When using the clock output (CLKOUT) function, ~~connection of this clock output to EXCLK pin enables to use the pin also as the external main system clock of MCU. In this case, connect this pin to EXCLK pin on the user board~~.

GPIO1 and GPIO2 pins are alternative to switch control function for antenna diversity. The defaults are GPIO1 and GPIO2 pins.

GPIO4 pin is alternative to ANTSW signal function. The default is GPIO4.

Correct

(4) GPIO0/CLKOUT, GPIO1/ANTSELOUT0, GPIO2/ANTSELOUT1, GPIO3, GPIO4/ANTSW

These are 5-bit I/O port pins.

GPIO0 pin also provides the clock output (CLKOUT) function, and the default is GPIO0 pin.

When using the clock output (CLKOUT) function, **It cannot be used in RF transmission/reception mode.**

GPIO1 and GPIO2 pins are alternative to switch control function for antenna diversity. The defaults are GPIO1 and GPIO2 pins.

GPIO4 pin is alternative to ANTSW signal function. The default is GPIO4.

2. (2) RF reference clock output (Page 551)

Incorrect:

(2) RF reference clock output

The divided clock of RF reference clock can be output from CLKOUT pin. The frequencies 12 MHz, 8 MHz, and 4 MHz can be specified for outputting. ~~Connection of this clock output to EXCLK pin enables to use the pin also as the external main system clock of MCU. In this case, connect this pin to EXCLK pin on the user board.~~

correct:

(2) RF reference clock output

The divided clock of RF reference clock can be output from CLKOUT pin. The frequencies 12 MHz, 8 MHz, and 4 MHz can be specified for outputting.

3. 18.6.5 Pin state in each RF mode (Page 663)

Incorrect:

Table 18 - 15 Function State in Each RF Mode

Pin	SLEEP	IDLE	RF Transmission	RF Reception
STANDBY	Low input	High input	High input	High input
OSCDRVSE internal pin	Low input (During XTAL_RF oscillation) High input (During REFCLKIN_RF external clock)	High input	High input	High input
DON internal pin	Low input	High input	High input	High input
RFRESETB internal pin	Low input	High input	High input	High input
INTOUT	Hi-Z	Operable	Operable	Operable
CLKOUT	Hi-Z	Operable	~~Operable~~	~~Operable~~
GPIO0 GPIO1 GPIO2 GPIO3 GPIO4	Hi-Z	Operable	Operable	Operable

correct:

Table 18 - 15 Function State in Each RF Mode

Pin	SLEEP	IDLE	RF Transmission	RF Reception
STANDBY	Low input	High input	High input	High input
OSCDRVSE internal pin	Low input (During XTAL_RF oscillation) High input (During REFCLKIN_RF external clock)	High input	High input	High input
DON internal pin	Low input	High input	High input	High input
RFRESETB internal pin	Low input	High input	High input	High input
INTOUT	Hi-Z	Operable	Operable	Operable
CLKOUT	Hi-Z	Operable	**Prohibited**	**Prohibited**
GPIO0 GPIO1 GPIO2 GPIO3 GPIO4	Hi-Z	Operable	Operable	Operable