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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RH8-B0246B/E	Rev.	2.00
Title	RH850/C1M-A1, RH850/C1M-A2 User's Manual Hardware Rev.1.20 Errata		Information Category	Technical Notification		
Applicable Product	RH850/C1M-A1 RH850/C1M-A2	Lot No. -	Reference Document	Refer to the below		

1. Explanation

This document is errata of RH850/C1M-A1, RH850/C1M-A2 User's Manual Hardware Rev.1.20.

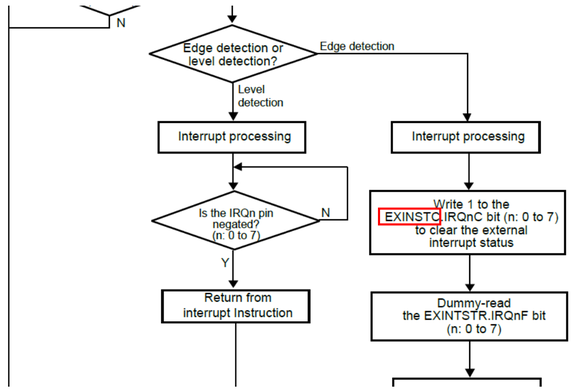
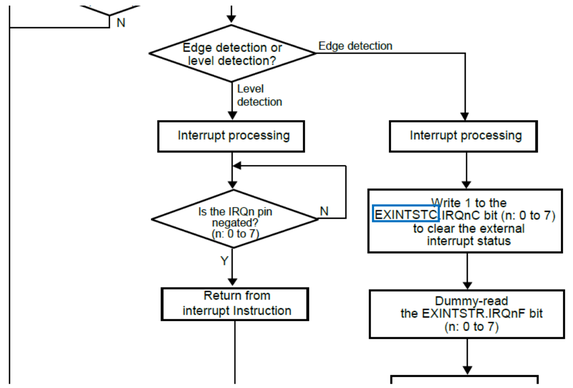
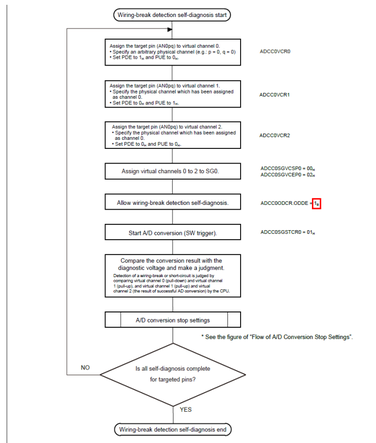
No.1 to No.15 have already been notified on the previous edition of TN-RH8-B0246A/E.

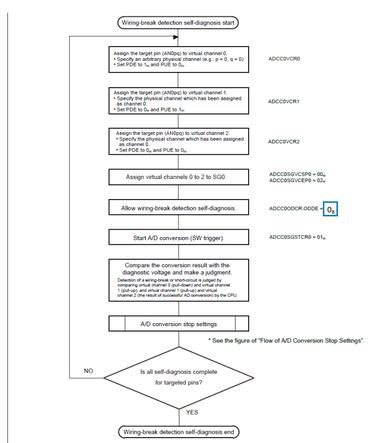
No.16 to No.53 are additional items.

【Reference Documents】

Series	Series	Series	Rev.	Document No
RH850	C1M-A1, C1M-A2	RH850/C1M-A1, RH850/C1M-A2 User's Manual: Hardware	1.20	R01UH0607EJ0120

The changes are shown below. (Error: red, Correct: blue)

<table>
<tr><th>No.</th><th>PDF page
(Rev.1.20)</th><th>Section</th><th>Chapter title
(Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>1</td><td>285</td><td>Interrupt</td><td>Figure 6.1 Example of External Interrupt Processing Flow</td><td> 
</td><td> 
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>2</td><td>2531</td><td>ADCC</td><td>27.4.7.3 Wiring-Break Detection Self-Diagnosis Circuit Function</td><td>27.4.7.3 Wiring-Break Detection Self-Diagnosis Circuit Function
This is a function to detect a wiring-break in a pin due to solder separation.
Discharge the target analog pin for the specified time in the wiring-break detection control register (ADCCnODCR register) and then perform A/D conversion. If the conversion result attenuates to approximately 0 V, you can determine that a wiring-break is present.</td><td>27.4.7.3 Wiring-Break Detection Self-Diagnosis Circuit Function
This is a function to detect a wiring-break in a pin due to solder separation.
If a wiring break exists the result of conversion converges approximately to AnVSS or AnVCC due to pull-down or pull-up method.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>3</td><td>2537</td><td>ADCC</td><td>27.5.5 Procedure for Setting Wiring-Break Detection Self-Diagnosis</td><td>27.5.5 Procedure for Setting Wiring-Break Detection Self-Diagnosis
Wiring-break detection is a facility for detecting wiring breaks in ANI. Both pull-down and pull-up methods are used for detection. In pull-down method, if a wiring-break occurs, the result of the AD conversion is attenuated to approximately 0V, which is detected as an abnormal value. Therefore, the user can judge that a wiring-break has been detected. In pull-up method, if a wiring-break occurs, the result of the AD conversion is booted to approximately 5V,which is detected as an abnormal value. Therefore, the user can judge that a wiring-break has been detected.</td><td>27.5.5 Procedure for Setting Wiring-Break Detection Self-Diagnosis
Wiring-break detection is a facility for detecting wiring breaks in ANI. In wiring-break detection mode, a pull-down or pull-up resistor is connected for sampling of the sample-and-hold circuits when the width of pulse is fixed (18 states).
In pull-down method, if a wiring-break occurs, the result of the AD conversion is attenuated to approximately AnVSS, which is detected as an abnormal value. Therefore, the user can judge that a wiring-break has been detected. In pull-up method, if a wiring-break occurs, the result of the AD conversion is booted to approximately AnVCC,which is detected as an abnormal value. Therefore, the user can judge that a wiring-break has been detected.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>4</td><td>2538</td><td>ADCC</td><td>Figure 27.28 Flow of Wiring-Break Detection Self-Diagnostic Settings</td><td> 

Note: Perform wiring-break detection self-diagnosis on each pin one by one.
Figure 27.28 Flow of Wiring-Break Detection Self-Diagnostic Settings</td><td> 

Note: Perform wiring-break detection self-diagnosis on each pin one by one.
Figure 27.28 Flow of Wiring-Break Detection Self-Diagnostic Settings</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>5</td><td>2649</td><td>Functional Safety</td><td>Table 29.66 List of ECC Modules</td><td>Table 29.66 List of ECC Modules
<table><tr><th colspan="2" rowspan="3">Supported Peripheral Function</th><th colspan="4">ECC Module Names and Register Base Addresses</th></tr><tr><th colspan="2">Master Side*1</th><th colspan="2">Checker Side*1</th></tr><tr><th>Module Name</th><th>Base Address <base_addr></th><th>Module Name</th><th>Base Address <base_addr></th></tr><tr><td>RS-CANFD</td><td>Message buffer RAM (MB RAM)</td><td>E7RC1M</td><td>FFC71000H</td><td>E7RC1C</td><td>FFC71200H</td></tr><tr><td></td><td>Acceptance filter list RAM (AFL RAM)</td><td>E7RC2M</td><td>FFC71400H</td><td>E7RC2C</td><td>FFC71600H</td></tr><tr><td>CSIH</td><td>CSIH0</td><td>E7CS0M</td><td>FFC70000H</td><td>E7CS0C</td><td>FFC70200H</td></tr><tr><td></td><td>CSIH1</td><td>E7CS1M</td><td>FFC70400H</td><td>E7CS1C</td><td>FFC70600H</td></tr><tr><td></td><td>CSIH2</td><td>E7CS2M</td><td>FFC70800H</td><td>E7CS1C</td><td>FFC70A00H</td></tr></table>Note 1. Two modules (one for master and the other for checker) are provided for duplex configuration.</td><td>Table 29.66 List of ECC Modules
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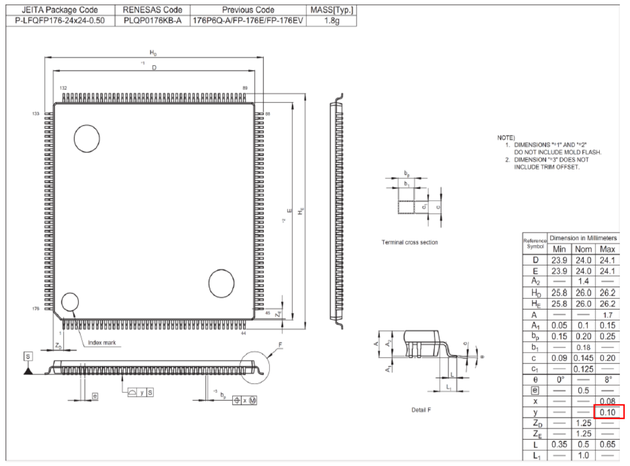
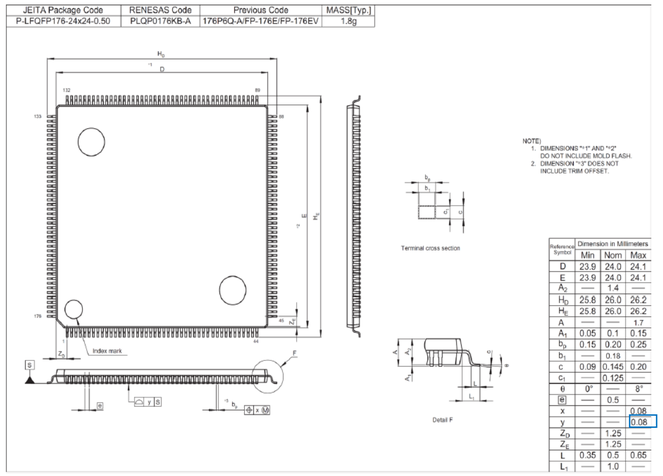
<tr><td>6</td><td>2895</td><td>Appendix A Package Dimensions</td><td>QFP176 (standard)</td><td>・QFP176 (standard)
 
</td><td>・QFP176 (standard)
 
</td><td>Description Change</td><td>TN-RH8-B163A/E</td><td>–</td></tr>
<tr><td>7</td><td>2710</td><td>Functional Safety</td><td>Table 29.103 ERRSLVxxADDR Register Contents</td><td>Table 29.103 ERRSLVxxADDR Register Contents
<table><tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr><tr><td>31 to 0</td><td>ADDR[31:0]</td><td>Address at which an error has occurred.
ADDR[1:0] are fixed to 0</td></tr></table></td><td>Table 29.103 ERRSLVxxADDR Register Contents
<table><tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr><tr><td>31 to 0</td><td>ADDR[31:0]</td><td>Address at which an error has occurred.
ADDR[1:0] are undefined.</td></tr></table></td><td>Description Change</td><td>TN-RH8-B0193A/E</td><td>–</td></tr>
<tr><td>8</td><td>2670</td><td>Functional Safety</td><td>29.3 Lockstep</td><td>none</td><td>29.3.3 Usage Notes
Reading a register with a value that is undefined after a reset without initializing the register may lead to a lock step compare error. Accordingly, such registers must be initialized with the desired settings.
Even if the branch instruction and the subsequent instruction is issued in parallel, the lock step compare error might be occurred by undefined register after the reset. It should be applied as specified below until the register which refer by subsequent instruction is initialized in case of branching in the preceding instruction.
● Insert the SYNCI instruction or the RIE instruction following the branch instruction.(It has to be added by assembler language. When C language is used, it could be optimized.)
Applicable branch instructions: Bcond except BR, JARL, JMP</td><td>Description Change</td><td>TN-RH8-B0183C/E</td><td>–</td></tr>
<tr><td>9</td><td>247</td><td>Operating Mode</td><td>Table 5.1 Selection of Operating Mode</td><td>Table 5.1 Selection of Operating Mode
<table><tr><th colspan="3">Value Set in the Pin</th><th colspan="2">Value Set in the Option Byte Register 0</th><th>Operating Mode</th><th>Startup Area</th><th>Type of IF*1</th><th>Remark</th></tr><tr><th>MD1</th><th>MD0</th><th>FLMODE</th><th>STMSEL1</th><th>STMSEL0</th><th></th><th></th><th></th><th></th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>User boot mode</td><td>User area</td><td>The interface can be selected by OPBT2 in the option byte area. For details, see Section 35.9.2 OPBT2 — Option Byte 2 Register.</td><td>On-chip debug is available.</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>User boot mode</td><td>User boot area</td><td></td><td></td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>X</td><td>Serial programming mode</td><td>Boot area</td><td>Writer I/F (2-line UART)</td><td>Serial programming is available.</td></tr><tr><td>0</td><td>0</td><td>1</td><td>X</td><td>X</td><td>Boundary scan mode</td><td>—</td><td>JTAG</td><td>Boundary scan is available.</td></tr><tr><td>0</td><td>1</td><td>0</td><td>X</td><td>X</td><td>Serial programming mode</td><td>Boot area</td><td>Writer I/F (2-line UART)</td><td>Serial programming is available.</td></tr><tr><td>0</td><td>1</td><td>1</td><td>X</td><td>X</td><td>Serial programming mode</td><td>Boot area</td><td>Writer I/F (3-line clock synchronous connection)</td><td>Serial programming is available.</td></tr></table>Note: X = Don't care
Note 1. See Section 2.4.3, Pin State for the functions and states of pins when each interface is selected.</td><td>Table 5.1 Selection of Operating Mode
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Note 1. See Section 2.4.3, Pin State for the functions and states of pins when each interface is selected.
Note 2. Always input low level to MD1.</td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>10</td><td>2795</td><td>On-Chip Debugging Unit (OCD)</td><td>Table 34.2 I/O Pins of AUDR</td><td>Table 34.2 I/O Pins of AUDR
<table><tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr><tr><td>$\overline{\text{AUDRST}}$</td><td>Input</td><td>AUDR reset input pin
Inputting L to this pin resets the AUDR, ~~but it does not initialize the AUDISR, AUDMBR and AUDMBRC (described below).~~
When this pin is not connected, it is internally pulled-down.</td></tr></table></td><td>Table 34.2 I/O Pins of AUDR
<table><tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr><tr><td>$\overline{\text{AUDRST}}$</td><td>Input</td><td>AUDR reset input pin
Inputting L to this pin resets the AUDR.
When turning on the power, set this pin to Low regardless of the use of AUDR.
When this pin is not connected, it is internally pulled-down.
Make sure to initialize AUDR before inputting High to this pin.
CAUTION: AUDR is initialized when this pin is Low and AUDCK is input for a fixed number of cycles, but it does not initialize the AUDISR, AUDMBR and AUDMBRC (described below).
Refer to Section 34.4.4.3, Usage Notes on the AUDR Function and Section 39, Electrical Characteristics for the number of cycles required for initialization.</td></tr></table></td><td>Description Change</td><td>TN-RH8-B0228A/E</td><td>–</td></tr>
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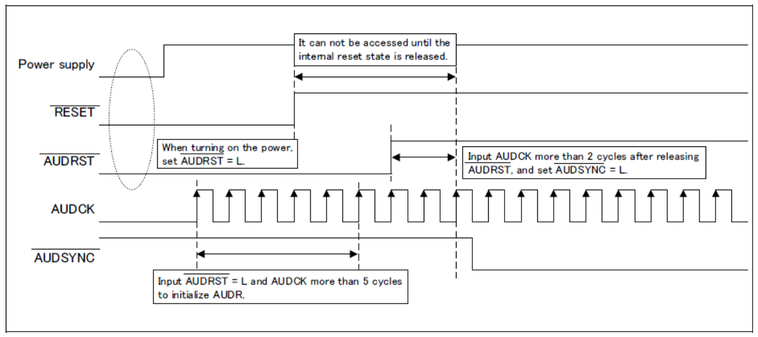
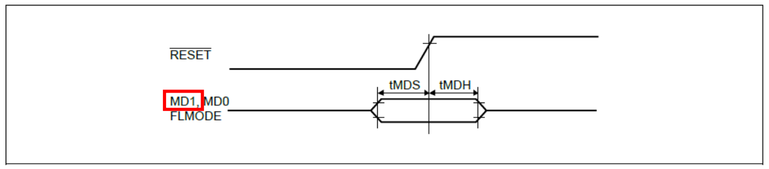
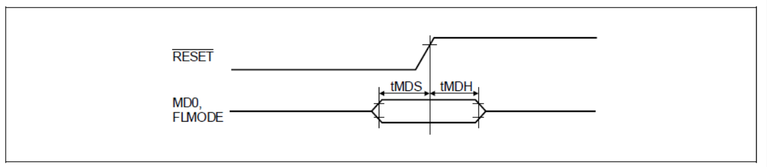
<tr><td>11</td><td>2807</td><td>On-Chip Debugging Unit (OCD)</td><td>34.4.4.3 Usage Notes on the AUDR Function</td><td>34.4.4.3 Usage Notes on the AUDR Function
• Do not negate the $\overline{\text{AUDSYNC}}$ pin until one cycle of AUDCK has elapsed after a command is input to the AUDATA pin and the Ready flag has been returned.
• When uninitialized memory is accessed through the AUDR, a bus error may occur due to ECC error detection.</td><td>34.4.4.3 Usage Notes on the AUDR Function
• Do not negate the $\overline{\text{AUDSYNC}}$ pin until one cycle of AUDCK has elapsed after a command is input to the AUDATA pin and the Ready flag has been returned.
• When uninitialized memory is accessed through the AUDR, a bus error may occur due to ECC error detection.
• Do not reset AUDR with $\overline{\text{AUDRST}}$ = L, while transferring data with AUDR ($\overline{\text{AUDSYNC}}$ = L). The data transfer of AUDR is not completed in the System Interconnect, and it may interfere with the data transfer of other bus masters.
• AUDR can not transfer data when being in external or internal reset state.
• Do not assert $\overline{\text{AUDSYNC}}$ pin for a minimum of 2 AUDCK cycles after AUDR reset release with $\overline{\text{AUDRST}}$ = H.
• The timing from power on to data transfer is shown in Figure 34.xx.
 
Figure 34.xx Timings from power on to data transfer</td><td>Description Change</td><td>TN-RH8-B0228A/E</td><td>–</td></tr>
<tr><td>12</td><td>2808</td><td>On-Chip Debugging Unit (OCD)</td><td>34.5 Cautions on Using On-Chip Debugger</td><td>none</td><td>(5) Handling of /DCUTRSTpin at power on
Set the /DCUTRSTpin to the low level at power on, regardless of whether on-chip debugging is used.</td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>13</td><td>2867</td><td>Electrical Characteristics</td><td>Figure 39.5 Control Signal Timing</td><td> 
Figure 39.5 Control Signal Timing</td><td> 
Figure 39.5 Control Signal Timing</td><td>Writing Error</td><td>–</td><td>–</td></tr>
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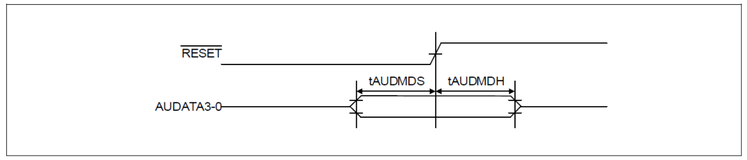
<tr><td>14</td><td>2884</td><td>Electrical Characteristics</td><td>Table 39.30 AUD RAM Monitor Timing</td><td>Table 39.30 AUD RAM Monitor Timing
Conditions: Tj = – 40°C to 150°C, CL = 30 pF
<table><tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th></tr><tr><td>AUDCK cycle time (monitor mode)</td><td>tAUCKMcyc</td><td>50</td><td>—</td><td>ns</td></tr><tr><td>AUDCK high-level width (monitor mode)</td><td>tAUCKMH</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>AUDCK low-level width (monitor mode)</td><td>tAUCKML</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>$\overline{\text{AUDRST}}$ setup time (monitor mode, vs. AUDCK↑)</td><td>tAURSTMS</td><td>30</td><td>—</td><td>ns</td></tr><tr><td>$\overline{\text{AUDRST}}$ input pulse width (monitor mode)</td><td>tAURSTMW</td><td>5 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>Monitor data output delay time (to AUDCK ↑)</td><td>tAUDTMD</td><td>—</td><td>35</td><td>ns</td></tr><tr><td>Monitor data input setup time (to AUDCK ↑)</td><td>tAUDTMS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>Monitor data input hold time (from AUDCK ↑)</td><td>tAUDTMH</td><td>5</td><td>—</td><td>ns</td></tr><tr><td>$\overline{\text{AUDSYNC}}$ input setup time (vs. AUDCK ↑)</td><td>tAUDSYS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>$\overline{\text{AUDSYNC}}$ input hold time (vs. AUDCK ↑)</td><td>tAUDSYH</td><td>5</td><td>—</td><td>ns</td></tr></table></td><td>Table 39.30 AUD RAM Monitor Timing
Conditions: Tj = – 40°C to 150°C, CL = 30 pF
<table><tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th></tr><tr><td>AUDCK cycle time (monitor mode)</td><td>tAUCKMcyc</td><td>50</td><td>—</td><td>ns</td></tr><tr><td>AUDCK high-level width (monitor mode)</td><td>tAUCKMH</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>AUDCK low-level width (monitor mode)</td><td>tAUCKML</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>$\overline{\text{AUDRST}}$ setup time (monitor mode, vs. AUDCK↑)</td><td>tAURSTMS</td><td>30</td><td>—</td><td>ns</td></tr><tr><td>$\overline{\text{AUDRST}}$ input pulse width (monitor mode)</td><td>tAURSTMW</td><td>5 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>Monitor data output delay time (to AUDCK ↑)</td><td>tAUDTMD</td><td>—</td><td>35</td><td>ns</td></tr><tr><td>Monitor data input setup time (to AUDCK ↑)</td><td>tAUDTMS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>Monitor data input hold time (from AUDCK ↑)</td><td>tAUDTMH</td><td>5</td><td>—</td><td>ns</td></tr><tr><td>$\overline{\text{AUDSYNC}}$ input setup time (vs. AUDCK ↑)</td><td>tAUDSYS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>$\overline{\text{AUDSYNC}}$ input hold time (vs. AUDCK ↑)</td><td>tAUDSYH</td><td>5</td><td>—</td><td>ns</td></tr><tr><td>AUDISR setup time</td><td>tAUDMDS</td><td>1</td><td>—</td><td>ms</td></tr><tr><td>AUDISR hold time</td><td>tAUDMDH</td><td>1</td><td>—</td><td>ms</td></tr></table></td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>15</td><td>2884</td><td>Electrical Characteristics</td><td>39.3.12 AUD RAM Monitor</td><td>none</td><td> 
Figure 39.xx Timing to reflect settings on AUDISR</td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>16</td><td>63</td><td>Overview</td><td>Table 1.1 Overview of Products (2/2)</td><td><table><tr><td>Motor control</td><td>R/D converter (RDC3A)</td><td>2 units</td><td>1 unit</td></tr><tr><td></td><td>Enhanced motor control unit (EMU3): Number of units</td><td>1 unit (2 channels)</td><td>1 unit (2 channels)</td></tr><tr><td></td><td>Enhanced motor control unit (EMU3): SubCPU frequency</td><td>320 MHz</td><td>240 MHz</td></tr></table></td><td><table><tr><td>Motor control</td><td>R/D converter (RDC3A)</td><td>2 units</td><td>1 unit</td></tr><tr><td></td><td>Enhanced motor control unit (EMU3): Number of units</td><td>1 unit (2 channels)</td><td>1 unit (1 channel)</td></tr><tr><td></td><td>Enhanced motor control unit (EMU3): SubCPU frequency</td><td>320 MHz</td><td>240 MHz</td></tr></table></td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>17</td><td>157</td><td>Pins</td><td>Table 2.64 Example Handling of Unused Pins (2/2)</td><td><table><tr><th>Category</th><th>Pins</th><th>IO</th><th>Example handling of unused pins</th><th>Internal pull-up/pull-down resistor</th></tr><tr><td>Debug system (NEXUS/LPD)</td><td>DCUTDI</td><td>I</td><td>• Leave the pin open.
• Separately connect the pin with VCC via a resistor.
(Serial programming mode is disabled.)</td><td>An internal pull-up resistor is included.</td></tr><tr><td></td><td>DCUTDO</td><td>O</td><td>• Leave the pin open.
(Serial programming mode is disabled.)</td><td>None</td></tr><tr><td></td><td>DCUTCK</td><td>I</td><td>• Leave the pin open.
• Separately connect the pin with VCC via a resistor.
(Serial programming mode is disabled.)</td><td>An internal pull-up resistor is included.</td></tr><tr><td></td><td>$\overline{\text{DCUTMS}}$</td><td>I</td><td>• Leave the pin open.
• Separately connect the pin with VCC via a resistor.</td><td>An internal pull-up resistor is included.</td></tr><tr><td></td><td>$\overline{\text{DCUTRST}}$</td><td>I</td><td>Separately connect the pin with VSS via a resistor.</td><td>An internal pull-down resistor is included.</td></tr><tr><td></td><td>$\overline{\text{DCURDY}}$</td><td>O</td><td>Leave the pin open.</td><td>None</td></tr></table></td><td><table><tr><th>Category</th><th>Pins</th><th>IO</th><th>Example handling of unused pins</th><th>Internal pull-up/pull-down resistor</th></tr><tr><td>Debug system (NEXUS/LPD)</td><td>DCUTDI</td><td>I</td><td>• Leave the pin open.
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</table>

<table>
<tr><th>No.</th><th>PDF page
(Rev.1.20)</th><th>Section</th><th>Chapter title
(Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>18</td><td>160</td><td>CPU System</td><td>Table 3.1 Peripheral Group Configuration (1/4)</td><td>
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<table>
<tr><th>Peripheral Group</th><th>Module Name*1</th></tr>
<tr><td>CPU</td><td>INTC1</td></tr>
<tr><td></td><td>IPIRSS</td></tr>
<tr><td></td><td>IPG</td></tr>
<tr><td></td><td>MEV</td></tr>
<tr><td></td><td>PEG</td></tr>
<tr><td></td><td>SEG</td></tr>
<tr><td></td><td>TESTCOMP</td></tr>
<tr><td>CPU (DEBUG)</td><td>AUDR</td></tr>
<tr><td>0</td><td>APDP[INTC2]</td></tr>
<tr><td></td><td>APDP[PDMA]</td></tr>
<tr><td></td><td>DMASS</td></tr>
<tr><td></td><td>ECCCPU1</td></tr>
<tr><td></td><td>ECCCPU2</td></tr>
<tr><td></td><td>ECCEEP</td></tr>
<tr><td></td><td>ECCEEPC</td></tr>
<tr><td></td><td>ECCFLI</td></tr>
<tr><td></td><td>ECCGRAM</td></tr>
<tr><td></td><td>ECCIC1</td></tr>
<tr><td></td><td>ECCIC2</td></tr>
<tr><td></td><td>FACI[FCUFAREA*2]</td></tr>
<tr><td></td><td>FLASH[FRDCYCLD]</td></tr>
<tr><td></td><td>INTC2</td></tr>
<tr><td></td><td>MGDGR</td></tr>
<tr><td></td><td>MISG (CPU1, CPU2)</td></tr>
<tr><td></td><td>PBG[PBG0, PBG1]</td></tr>
<tr><td></td><td>ICUSE</td></tr>
<tr><td></td><td>DataFlash</td></tr>
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<tr><td></td><td>DataFlash</td></tr>
<tr><td></td><td>CPU(BOOTCTRL)</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>19</td><td>213</td><td>CPU</td><td>Table 3.63 PEG Register Base Address: FFFE E600H</td><td>
<table>
<tr><th>Address Offset</th><th>Size (byte)</th><th>Register Name</th><th>Symbol</th><th>Permission</th><th>R/W</th><th colspan="4">Operable Bit</th><th>Value after Reset</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td>8</td><td>16</td><td>32</td><td></td></tr>
<tr><td>+00C$_H$</td><td>2</td><td>PE guard PEID&SPID master decision control register</td><td>PEGSP</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>—</td><td>0000$_H$</td></tr>
<tr><td>+080$_H$</td><td>4</td><td>PE guard area mask setting register 0</td><td>PEGG0MK</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>FFE0 0000$_H$</td></tr>
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<tr><td>+088$_H$</td><td>4</td><td>PE guard area SPID setting register 0</td><td>PEGG0SP</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+08C$_H$</td><td>4</td><td>PE guard area PEID setting register 0</td><td>PEGG0PE</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+090$_H$</td><td>4</td><td>PE guard area mask setting register 1</td><td>PEGG1MK</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>FFE0 0000$_H$</td></tr>
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<tr><td>+0A8$_H$</td><td>4</td><td>PE guard area SPID setting register 2</td><td>PEGG2SP</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+0AC$_H$</td><td>4</td><td>PE guard area PEID setting register 2</td><td>PEGG2PE</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+0B0$_H$</td><td>4</td><td>PE guard area mask setting register 3</td><td>PEGG3MK</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>FFE0 0000$_H$</td></tr>
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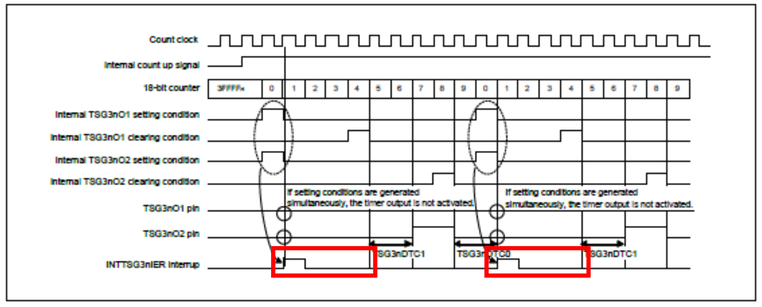
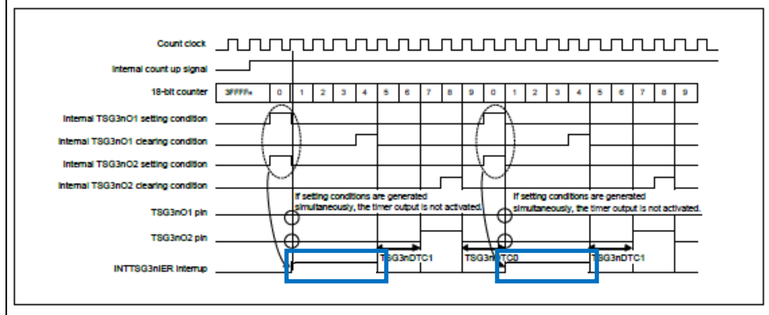
Note 2. The registers with "SV" are only accessible in SV mode (UM = 0).
</td><td>Description Change</td><td>TN-RH8-B0281A/E</td><td>–</td></tr>
<tr><td>20</td><td>707</td><td>RLIN3</td><td>13.9 LIN Self-Test Mode</td><td>Regardless of the setting of the baud rate related registers, the baud rate operates at the LIN communication clock source/16 [bps].
(The NSPB bits in the RLN3nLWBR register should be set to 0000$_B$ or 1111$_B$.)</td><td>Regardless of the setting of the baud rate related registers, the baud rate operates at the LIN communication clock source/16 [bps].
(The NSPB bits in the RLN3nLWBR register should be set to 0000$_B$ or 1111$_B$.)
(The LPRS bits in the RLN3nLWBR register should be set to 000$_B$.)</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>21</td><td>709</td><td>RLIN3</td><td>13.9.2 Transmission in LIN Master Self-Test Mode</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 xxxx_B*1</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 000x_B</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>22</td><td>710</td><td>RLIN3</td><td>13.9.3 Reception in LIN Master Self-Test Mode</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 xxxx_B*1</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 000x_B</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>23</td><td>711</td><td>RLIN3</td><td>13.9.4 Transmission in LIN Slave Self-Test Mode</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 xxx0_B*1</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 0000$_B$</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>24</td><td>712</td><td>RLIN3</td><td>13.9.5 Reception in LIN Slave Self-Test Mode</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 xxx0_B*1</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 0000$_B$</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>25</td><td>712</td><td>RLIN3</td><td>13.9.5 Reception in LIN Slave Self-Test Mode</td><td>To execute a self-test on LIN slave reception, perform the procedure below:。</td><td>To execute a self-test on LIN slave reception, perform the procedure below:</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>26</td><td>849</td><td>RS-CANFD</td><td>14.3.13.3 RSCANnTHLPCTRm</td><td>At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCANnTHLSTSm register is decremented.</td><td>At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCANnTHLSTSm register is decremented by 1.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>27</td><td>1005</td><td>RS-CANFD</td><td>14.4.14.3 RSCFDnCFDTHLPCTRm</td><td>At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCFDnCFDTHLSTSm register is decremented.</td><td>At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCFDnCFDTHLSTSm register is decremented by 1.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

No.	PDF page (Rev.1.20)	Section	Chapter title (Chart title)	Error	Correct	Change reason	Notice situation	Note
28	1032	RS-CANFD	14.8.1 Transmit Priority Determination	When messages are retransmitted due to an arbitration-lost or an error, transmit priority determination is made again regardless of the TPRI bit.	When messages are retransmitted due to an arbitration-lost or an error, transmit priority determination is made again according to the TPRI bit.	Writing Error	-	-
29	1051	RS-CANFD	14.11.1.4 Receive Rule Setting	Up to 16 receive rules can be registered per page. Specify pages 0 to 23 (for 6-channel unit) by the AFLPN[4:0] bits in the RSCFDn(CFD)GAFLECTR register.	Up to 16 receive rules can be registered per page. Specify pages 0 to 15 (for 4-channel unit) by the AFLPN[4:0] bits in the RSCFDn(CFD)GAFLECTR register.	Writing Error	-	-
30	1059	RS-CANFD	14.11.2.2 FIFO Buffer Reading Procedure	When received messages have been stored in one or more receive FIFO buffers or a transmit/receive FIFO buffer that is set to receive mode or gateway mode, the corresponding message count display counter (RFMC[7:0] bits in the RSCFDn(CFD)RFSTSx register (x = 0 to 7) or CFMC[7:0] bits in the RSCFDn(CFD)CFSTSk register (k = 0 to 11)) is incremented.	When received messages have been stored in one or more receive FIFO buffers or a transmit/receive FIFO buffer that is set to receive mode or gateway mode, the corresponding message count display counter (RFMC[7:0] bits in the RSCFDn(CFD)RFSTSx register (x = 0 to 7) or CFMC[7:0] bits in the RSCFDn(CFD)CFSTSk register (k = 0 to 11)) is incremented by 1.	Writing Error	-	-
31	1063	RS-CANFD	14.11.2.3 FIFO Buffer Reading Procedure by DMA Transfer	Note 1. ・For receive FIFO buffers RCFDCnCFDRFIDx, RCFDCnCFDRFPTRx, RCFDCnCFDRFFDSTSx, RCFDCnCFDRFDFd_x ・For transmit/receive FIFO buffers RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk, RCFDCnCFDCFDFd_k	Note 1. ・For receive FIFO buffers RSCFDnCFDRFIDx、RSCFDnCFDRFPTRx、RSCFDnCFDRFFDSTSx、RSCFDnCFDRFDFd_x ・For transmit/receive FIFO buffers RSCFDnCFDCFIDk、RSCFDnCFDCFPTRk、RSCFDnCFDCFFDCSTSk、RSCFDnCFDCFDFd_k	Writing Error	-	-
32	1160	OS Timer	17.2.2 Block Diagram	The following block diagram shows the main components of the OSTM.	The following block diagram shows the main components of the OSTM. This product does not implement OSTMnTTOUT output.	Writing Error	-	-
33	1576	TSG3	20.2.1 Functional Overview	● Reload mode – Writing to TSG3nCMP1E enables reload (the reload request flag (TSG3nRSF) is set), and allows simultaneous transfer of the values of multiple registers. – Data can be transferred at peak/trough/peak or trough reload timing – Reload request flag (TSG3nRSF) – Register address assignment allowing DMA transfer	● Reload mode – Writing to TSG3nCMP1E enables reload (the reload request flag (TSG3nRSF) is set), and allows simultaneous transfer of the values of multiple registers. – Data can be transferred at peak/trough/peak or trough reload timing – Reload request flag (TSG3nRSF) – Register address assignment allowing DMA transfer – Reload skipping	Writing Error	-	-
34	1577	TSG3	20.2.1 Functional Overview	Reload skipping ● HT-PWM mode – 0 to 100% PWM duty cycle output is possible (with possible dead time reduction). – The LSB in the compare register can be used to append an additional pulse to the PWM output during count up, thus improving the output resolution without extra load on software.	● HT-PWM mode – 0 to 100% PWM duty cycle output is possible (with possible dead time reduction). – The LSB in the compare register can be used to append an additional pulse to the PWM output during count up, thus improving the output resolution without extra load on software.	Writing Error	-	-
35	1688	TSG3	Figure 20.48 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode)	 Figure 20.48 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode)	 Figure 20.48 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode)	Writing Error	-	-
36	1700	TSG3	Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)	● TSG3nCMP1E + TSG3nDTC1 ≥ TSG3nCMP0E + TSG3nCMP2E (TSG3nO2 stays inactive) ● TSG3nCMP2E + TSG3nDTC0 ≥ TSG3nCMP0E + TSG3nCMP1E (TSG3nO1 stays inactive)	● TSG3nCMP1E + TSG3nDTC1 ≥ TSG3nCMP0E + TSG3nCMP3E (TSG3nO2 stays inactive) ● TSG3nCMP3E + TSG3nDTC0 ≥ TSG3nCMP0E + TSG3nCMP1E (TSG3nO1 stays inactive)	Writing Error	-	-
37	1700	TSG3	Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)	At (4), the falling edge (inactive) of the TSG3nO1 output is caused by the simultaneous active state detected and the dead time counter starts counting. After the end of the dead time counter operation, the TSG3nO2 output becomes active.	At (4), the falling edge (inactive) of the TSG3nO1 output is caused by the simultaneous active state detected. The dead time counter starts counting after compare match with the TSG3nCMP1 register. After the end of the dead time counter operation, the TSG3nO2 output becomes active.	Writing Error	-	-

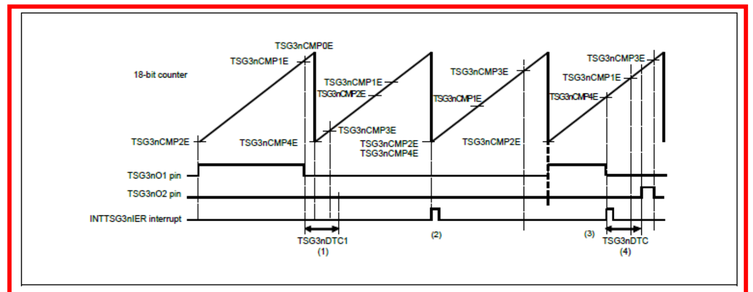
<table>
<tr><th>No.</th><th>PDF page
(Rev.1.20)</th><th>Section</th><th>Chapter title
(Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>38</td><td>1700</td><td>TSG3</td><td>Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)</td><td> 

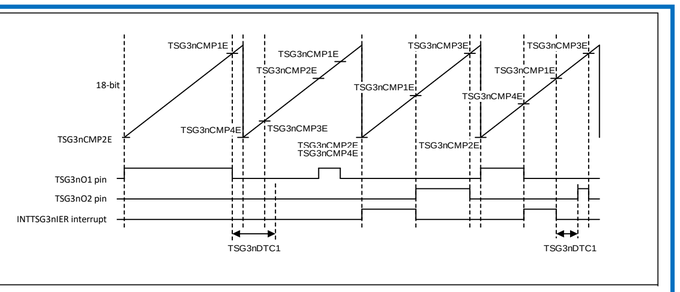
Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)</td><td> 

Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>39</td><td>1812</td><td>TAPA</td><td>Table 21.17 Operation of the Hi-Z Start Trigger (TAPAnOPHS)</td><td>

TAPAnOPHS	Operation
0/1	Writing 1 to the TAPAnOPHS0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the low level.

</td><td>

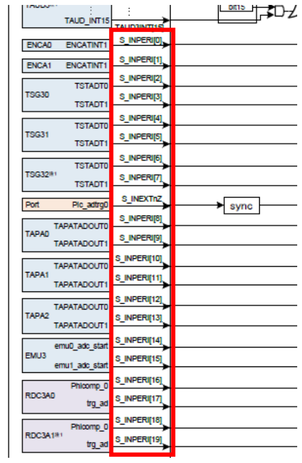
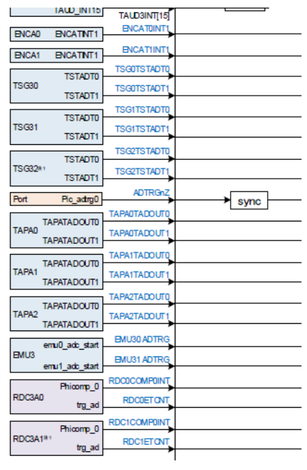
TAPAnDCM	Operation
0/1	Writing 1 to the TAPAnOPHS0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the low level.

</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>40</td><td>1812</td><td>TAPA</td><td>Table 21.18 Operation of the Hi-Z Stop Trigger (TAPAnOPHT) during Hi-Z Control in Response to Asynchronous Input</td><td>

TAPAnOPHT	Operation
0	Writing 1 to the TAPAnOPHT0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the high level.
1	If TAPAnTHASIN is at the inactive level, writing 1 to the TAPAnOPHT0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the high level. If TAPAnTHASIN is at the active level, writing of 1 to the TAPAnOPHT0 bit is ignored.

</td><td>

TAPAnDCM	Operation
0	Writing 1 to the TAPAnOPHT0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the high level.
1	If TAPAnTHASIN is at the inactive level, writing 1 to the TAPAnOPHT0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the high level. If TAPAnTHASIN is at the active level, writing of 1 to the TAPAnOPHT0 bit is ignored.

</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>41</td><td>2079</td><td>PIC</td><td>Figure 24.79 Block Diagram of PIC2D</td><td> 
</td><td> 
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>42</td><td>2379</td><td>RDC3A</td><td>Table 26.31 RDC3AnDIAG1 Register Contents (2/2)</td><td>

8	ERRST	Error Signal Reset Bit Writing 1 to this bit resets the register bits listed below to 0. Note that each of these bits remains at 1 if an error is continuous. This bit becomes 0 after two clock cycles have elapsed following it being set to 1. Register bits: ERHD, ERDEXC, ERDSBC, ERDSBS, ERDP2, ERDCNV, ERDR1 to 4V

</td><td>

8	ERRST	Error Signal Reset Bit Writing 1 to this bit resets the register bits listed below to 0. Note that each of these bits remains at 1 if an error is continuous. This bit becomes 0 after two clock cycles have elapsed following it being set to 1. Register bits: ERHD, ERDEXC, ERDSBC, ERDSBS, ERDP2, ERDCNV, ERDR1 to 2V,ERDS1 to 4V,ERDR1 to 2G,ERDS1 to 4G

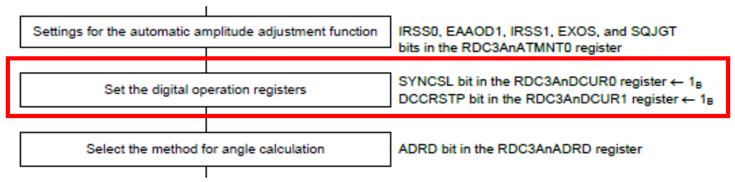
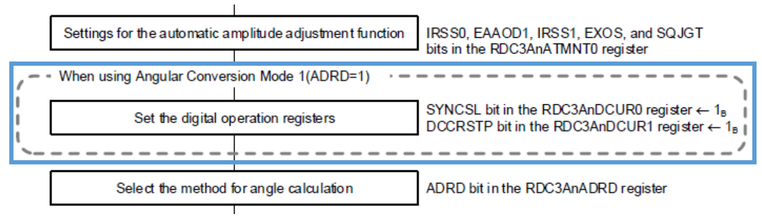
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>43</td><td>2399</td><td>RDC3A</td><td>Table 26.46 Data Selection</td><td>

DATASEL[5:0]	Output Signal	Output Destination DATA[X:X]
11.1011	12-bit AD output code [11:0]	[11:0]
10.1111	Control variation value [7:0] in angular conversion mode 1	[7:0]
00.0101	Control variation value [7:0] in angular conversion mode 0	[7:0]

</td><td>

DATSEL[5:0]	Output Signal	Output Destination DATA[X:X]
11.1011	12-bit AD output code [11:0]	[11:0]
10.1111	Control variation value [7:0] in angular conversion mode 1	[7:0]
00.0101	Control variation value [7:0] in angular conversion mode 0	[7:0]

</td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

No.	PDF page (Rev.1.20)	Section	Chapter title (Chart title)	Error	Correct	Change reason	Notice situation	Note
44	2405	RDC3A	Table 26.51 RDC3AnDCUR0 Register Contents	5 SYNCSL Synchronous Detection Setting in Angular Conversion Mode 1 (ADRD = 1) b5 0: Synchronous detection setting 0 1: Synchronous detection setting 1	5 SYNCSL Synchronous Detection Setting in Angular Conversion Mode 1 (ADRD = 1) b5 0: Synchronous detection setting 0 1: Synchronous detection setting 1 In Angular Conversion Mode 0 (ADRD = 0), set this bit to 0.	Description Change	TN-RH8-B0314A/E	–
45	2406	RDC3A	Table 26.52 RDC3AnDCUR1 Register Contents	13 DCCRSTP DC Error Correction Setting in Angular Conversion Mode 1 (ADRD = 1) b13 0: DC correction enabled 1: DC correction disabled Be sure to set this bit to 1 when the DC resolver is used.	13 DCCRSTP DC Error Correction Setting in Angular Conversion Mode 1 (ADRD = 1) b13 0: DC correction enabled 1: DC correction disabled Be sure to set this bit to 1 when the DC resolver is used. This setting has no effect when Angular Conversion Mode 0 (ADRD = 0).	Description Change	TN-RH8-B0314A/E	–
46	2439	RDC3A	26.4.5.1 Built-in Self-Test Function	The BISTs are categorized into two groups depending on their execution timing as follows; ● Execution is possible during angle conversion and when starting up the power (short-period BIST): ADBIST, resolver signal error detection BIST, resolver signal disconnect detection BIST, power short error BIST, ground short error BIST, sum-of-squares amplitude error detection BIST (high side), sum-of-squares amplitude error detection BIST (low side) ● Execution is possible when starting up the power: angle conversion BIST, conversion error BIST	The BISTs are categorized into two groups depending on their execution timing as follows; ● Execution is possible during angle conversion and when starting up the power (short-period BIST): ADBIST, resolver signal error detection BIST, resolver signal disconnect detection BIST, power short error BIST, ground short error BIST, sum-of-squares amplitude error detection BIST (high side), sum-of-squares amplitude error detection BIST (low side) ● Execution is possible when starting up the power: angle conversion BIST, conversion error BIST Short-period BIST can also be executed at starting up the power. However, if angle conversion BIST or conversion error BIST or both are executed at power-on, they must be executed before short-period BIST.	Description Change	TN-RH8-B0314A/E	–
47	2447	RDC3A	26.4.6.1 Period Measurement Timer	The period measurement timer measures the cycle of excitation signal (zero-crossing signal). When an edge (selectable from rise edge and fall edge) of the zero-crossing signal is detected, the value of the period measurement counter is captured and stored in the RDC3AnETCAP register. By reading the RDC3AnETCAP register, the cycle of excitation signal can be obtained. The cycle of excitation signal can be calculated from the following formula: (RDC3AnETCAP register value + 1) × CCLK cycle (25 ns). When the IREN bit in the RDC3AnETEN register is set to 1 (enables the interrupt), an excitation timer interrupt request is generated if the value set in the RDC3AnETCAP register matches the period measurement counter value. The excitation signal cycle error can be detected by setting a value of longer duration than the excitation signal cycle to the RDC3AnETCAP register.	The period measurement timer measures the cycle of excitation signal (zero-crossing signal). When an edge (selectable from rise edge and fall edge) of the zero-crossing signal is detected, the value of the period measurement counter is captured and stored in ET Capture bits of the RDC3AnETCAP register. By reading the RDC3AnETCAP register, the cycle of excitation signal can be obtained. The cycle of excitation signal can be calculated from the following formula: (RDC3AnETCAP register value + 1) × CCLK cycle (25 ns). When the IREN bit in the RDC3AnETEN register is set to 1 (enables the interrupt), an excitation timer interrupt request is generated if the value set in ET Compare bits of the RDC3AnETCAP register matches the period measurement counter value. The excitation signal cycle error can be detected by setting a value of longer duration than the excitation signal cycle to the RDC3AnETCAP register.	Writing Error	–	–
48	2454	RDC3A	Figure 26.29 Flow of Initial Settings of the Registers			Description Change	TN-RH8-B0314A/E	–
49	2455	RDC3A	26.6 Resolver Interface Circuit	1. RH ≈ {(RVCC − VCOM) / (22.0 × 10^{-6})} − RIN, where VCOM = RVCC/2[V]	1. RH ≈ {(+VEXT − VCOM) / (22.0 × 10^{-6})} − RIN, where VCOM = RVCC/2[V]	Writing Error	–	–
50	2541	ADCC	Table 27.52 Notes on Setting Registers	ADCCnTHCR, ADCCnTHACR, ADCCnTHBCR, ADCCnTHER, ADCCnTHGSR, ADCCnSGCRx, ADCCnSGVCSPx, ADCCnSGVCEPx: When setting the registers listed at left, write to the registers after they have been read. If this procedure is not followed, the written register value may not be correctly reflected in operations.	ADCCnTHCR, ADCCnTHACR, ADCCnTHBCR, ADCCnTHER, ADCCnTHGSR, ADCCnSGCRx, ADCCnSGVCSPx, ADCCnSGVCEPx: When setting the registers listed at left, write to the registers after they have been read. If writing to the register shown at the left occurs continuously without following this procedure, the written register value may not be correctly reflected in operations.	Additional Description	–	–

<table>
<tr><th>No.</th><th>PDF page
(Rev.1.20)</th><th>Section</th><th>Chapter title
(Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>51</td><td>2743</td><td>ECM</td><td>Table 30.8 List of Error Sources and Safety Processing (1/2)</td><td>
<table>
<tr><td>6</td><td>RAM</td><td>Local RAM (CPU1, CPU2) 2-bit ECC error and local RAM (CPU1) address parity error*3</td></tr>
<tr><td>7</td><td></td><td>Local RAM (CPU1, CPU2) 1-bit ECC error and local RAM (CPU1) parity bit error*3</td></tr>
</table>
</td><td>
<table>
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<tr><td>7</td><td></td><td>Local RAM (CPU1, CPU2) 1-bit ECC error and local RAM (CPU1, CPU2) parity bit error*3</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>52</td><td>2835</td><td>Flash Memory</td><td>35.10 Notes</td><td>(7) Items prohibited during programming and erasure
Do not perform the following operations during programming and erasure of the flash memory.</td><td>(7) Items prohibited during programming, erasure and blank checking
Do not perform the following operations during programming, erasure and blank checking of the flash memory.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>53</td><td>2888</td><td>Electrical Characteristics</td><td>Table 39.33 RDC Conversion Performance (2/2)</td><td>
<table>
<tr><th>Item</th><th colspan="2">Condition</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>Response delay*4</td><td rowspan="2">Electrical angle output response delay in fixed angular velocity</td><td>Angle conversion mode 0</td><td>–0.2</td><td>—</td><td>0.20</td><td rowspan="2">°/10000 min-1</td></tr>
<tr><td>Angle conversion mode 1</td><td>–0.2</td><td>—</td><td>0.20</td></tr>
<tr><td>BIST determination time*5</td><td colspan="2">Obtaining the sum of squares in amplitude abnormality detection BIST (L side)</td><td>—</td><td>—</td><td>1</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Obtaining the sum of squares in amplitude abnormality detection BIST (H side)</td><td>—</td><td>—</td><td>1</td><td>ms</td></tr>
<tr><td></td><td colspan="2">ADBIST</td><td>—</td><td>—</td><td>32</td><td>µs</td></tr>
<tr><td></td><td colspan="2">Angle conversion BIST (angle determination threshold is within ±8 LSB)</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Resolver signal error detection BIST</td><td>—</td><td>—</td><td>0.5</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Resolver signal cut off detection BIST</td><td>—</td><td>—</td><td>1</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Conversion error BIST</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Power short error BIST</td><td>—</td><td>—</td><td>80</td><td>µs</td></tr>
<tr><td></td><td colspan="2">Ground short error BIST</td><td>—</td><td>—</td><td>80</td><td>µs</td></tr>
<tr><td>BIST recovery time*5</td><td colspan="2">All kinds of BIST</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
</table>
</td><td>
<table>
<tr><th>Item</th><th colspan="2">Condition</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>Response delay*4</td><td rowspan="2">Electrical angle output response delay in fixed angular velocity</td><td>Angle conversion mode 0</td><td>–0.2</td><td>—</td><td>0.20</td><td rowspan="2">°/10000 min-1</td></tr>
<tr><td>Angle conversion mode 1</td><td>–0.2</td><td>—</td><td>0.20</td></tr>
<tr><td>BIST determination time*5</td><td colspan="2">Obtaining the sum of squares in amplitude abnormality detection BIST (L side)</td><td>—</td><td>—</td><td>1</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Obtaining the sum of squares in amplitude abnormality detection BIST (H side)</td><td>—</td><td>—</td><td>1</td><td>ms</td></tr>
<tr><td></td><td colspan="2">ADBIST</td><td>—</td><td>—</td><td>32</td><td>µs</td></tr>
<tr><td></td><td colspan="2">Angle conversion BIST (angle determination threshold is within ±16 LSB)</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Resolver signal error detection BIST</td><td>—</td><td>—</td><td>0.5</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Resolver signal cut off detection BIST</td><td>—</td><td>—</td><td>1</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Conversion error BIST</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
<tr><td></td><td colspan="2">Power short error BIST</td><td>—</td><td>—</td><td>80</td><td>µs</td></tr>
<tr><td></td><td colspan="2">Ground short error BIST</td><td>—</td><td>—</td><td>80</td><td>µs</td></tr>
<tr><td>BIST recovery time*6</td><td colspan="2">All kinds of BIST</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

End of the list