Date: Mar. 24, 2023

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RH8-B0468A/E	Rev.	1.00
Title	RH850 TSG3 issue		Information Category	Technical Notification		
Applicable Product	RH850 series	Lot No. All lot	Reference Document	See related documents below.		

The limitations of TSG3 are added as follows:

Red character: Added

1. Modified Description

(1) C1H/C1M

The following description is added under Table 19.13 TSG3nCTL5 Register Contents (3/3) and Table 19.14 TSG3nCTL6 Register Contents (3/3).

CAUTION

TSG3nATxx register bits should be set when the timer is stopped (TSG3nSTR0.TSG3nTE = 0).
Only the same value with current setting can be written during timer operation (TSG3nSTR0.TSG3nTE = 1).
If the different value is written to this register when TSG3nSTR0.TSG3nTE = 1,
timer operation cannot be guaranteed.

(2) C1M-A1/C1M-A2

The following description is added under Table 20.13 TSG3nCTL5 Register Contents (2/2) and Table 20.14 TSG3nCTL6 Register Contents (2/2).

CAUTION

TSG3nATxx register bits should be set when the timer is stopped (TSG3nSTR0.TSG3nTE = 0).
Only the same value with current setting can be written during timer operation (TSG3nSTR0.TSG3nTE = 1).
If the different value is written to this register when TSG3nSTR0.TSG3nTE = 1,
timer operation cannot be guaranteed.

(3) P1M

The following description is added under Table 25.14 TSG3nCTL5 Register Contents (3/3) and Table 25.15 TSG3nCTL6 Register Contents (3/3).

CAUTION

TSG3nATxx register bits should be set when the timer is stopped (TSG3nSTR0.TSG3nTE = 0).
Only the same value with current setting can be written during timer operation (TSG3nSTR0.TSG3nTE = 1).
If the different value is written to this register when TSG3nSTR0.TSG3nTE = 1,
timer operation cannot be guaranteed.

(4) P1M-E

The following description is added under Table 25.13 TSG3nCTL5 Register Contents (3/3) and Table 25.14 TSG3nCTL6 Register Contents (3/3).

CAUTION

TSG3nATxx register bits should be set when the timer is stopped (TSG3nSTR0.TSG3nTE = 0).
Only the same value with current setting can be written during timer operation (TSG3nSTR0.TSG3nTE = 1).
If the different value is written to this register when TSG3nSTR0.TSG3nTE = 1,
timer operation cannot be guaranteed.

(5) U2Ax

The following description is added under Table 35.14 TSG3nCTL5 Register Contents (3/3) and Table 35.15 TSG3nCTL6 Register Contents (3/3).

CAUTION

TSG3nATxx register bits should be set when the timer is stopped (TSG3nSTR0.TSG3nTE = 0).
Only the same value with current setting can be written during timer operation (TSG3nSTR0.TSG3nTE = 1).
If the different value is written to this register when TSG3nSTR0.TSG3nTE = 1,
timer operation cannot be guaranteed.

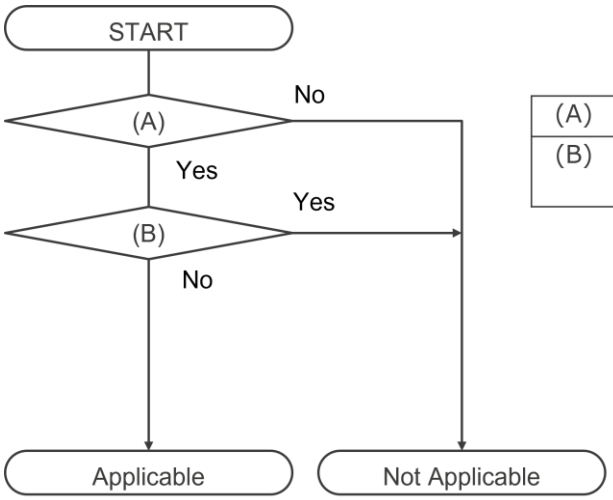
(6) U2Bx

The following description is added under Table 38.16 TSG3nCTL5 Register Contents (3/3) and Table 38.17 TSG3nCTL6 Register Contents (3/3).

CAUTION

TSG3nATxx register bits should be set when the timer is stopped (TSG3nSTR0.TSG3nTE = 0).
Only the same value with current setting can be written during timer operation (TSG3nSTR0.TSG3nTE = 1).
If the different value is written to this register when TSG3nSTR0.TSG3nTE = 1,
timer operation cannot be guaranteed.

2. Judgement flow



(A)	Using TSG3 ?
(B)	TSG3nATxx register bits should be set when the timer is stopped (TSG3nSTR0.TSG3nTE = 0) ?

3. Reference Documents

Group	Document Title	Rev.	Document Number
C1H/C1M	RH850/C1x User's Manual: Hardware	1.60	R01UH0414EJ0160
C1M-A1/C1M-A2	RH850/C1M-A1, RH850/C1M-A2User's Manual: Hardware	1.20	R01UH0607EJ0120
P1M	RH850/P1x Group User's Manual: Hardware	1.40	R01UH0436EJ0140
P1M-E	RH850/P1M-E Group User's Manual: Hardware	1.20	R01UH0585EJ0120
U2Ax	RH850/U2A-EVA Group User's Manual: Hardware	1.30	R01UH0864EJ0130
U2Bx	RH850/U2B Group User's Manual: Hardware	0.60	R01UH0923EJ0060