Date: Jan. 16, 2019

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	System LSI		Document No.	TN-RIN-A027A/E	Rev.	1.00
Title	Revisions of Documents Associated with R-IN32M3 Series User's Manual		Information Category	Technical Notification		
Applicable Product	R-IN32M3 Series (See below for details)	Lot No. All lots	Reference Document	R-IN32M3 Series Documents (See below for details)		

This is to report revisions of the R-IN32M3 Series documents listed in the "Reference Documents" below.

Please use the products covered in this report in consideration with the revised contents.

The item marked with "♦" is strongly related to device specifications and constraints.

1. Applicable Products

Product Type		Model Marking	Product Code
R-IN32M3-EC	Previous product	MC-10287F1	MC-10287F1-HN4-A
			MC-10287F1-HN4-M1-A
	Current product	MC-10287BF1	MC-10287BF1-HN4-A
			MC-10287BF1-HN4-M1-A
R-IN32M3-CL	Previous product	D60510F1	UPD60510F1-HN4-A
			UPD60510F1-HN4-M1-A
	Current product	D60510BF1	UPD60510BF1-HN4-A
			UPD60510BF1-HN4-M1-A

2. Reference Documents

Doc. No. in this TU	Document Title	Renesas Document Number	Previous Edition	Revised Edition
1	R-IN32M3 Series Data Sheet	R18DS0008EJ****	V4.01	V5.00
2	R-IN32M3-CL User's Manual	R18UZ0005EJ****	V3.01	V4.00
3	R-IN32M3-EC User's Manual	R18UZ0003EJ****	V4.01	V5.00
4	R-IN32M3 Series User's Manual: Peripheral Modules	R18UZ0007EJ****	V10.00	V11.00
5	R-IN32M3 Series User's Manual: Board design edition	R18UZ0021EJ****	V3.00	V4.00
6	R-IN32M3 Series Programming Manual: Driver	R18UZ0009EJ****	V5.00	V6.00
7	R-IN32 Series User's Manual (CC-Link Remote device station)	R18UZ0056EJ****	V1.01	V1.02

3. Revision Contents

Doc. No. in this TU	Item No.	Revisions (Section Number)	Previous Edition's Page Number	Revision Type
1	1-1	1.3 Overview	3	Complement
1	1-2	1.5 Memory Maps	6, 7, 10, 11	Note addition
1	1-3	1.5 Memory Maps	6, 7	Error correction
1	1-4	1.5 Memory Maps	10, 11	Error correction
1	1-5	2.3.5 Port Pins and Real-time Port Pins	22	Error correction
1	1-6	2.3.15 CC-Link Pins (Intelligent Device Station)	30	Error correction
1	1-7	4.2 Absolute Maximum Ratings	69	Complement
1	1-8	4.3 Recommended Operating Conditions	70	Complement
1	1-9	4.8.4 External MCU Interface Pins ♦ (3) Asynchronous Mode	92 94	Complement
1	1-10	4.8.5 Serial Flash ROM Interface ♦	99	Error correction
2	2-1	1.5 Base Addresses of the System Registers Area	-	Complement
2	2-2	2.1.4 Port Pins and Real-Time Port Pins	12	Error correction
2	2-3	2.1.14 CC-Link Pins (Intelligent Device Station)	19	Error correction
2	2-4	3. Memory Maps	40, 43	Note addition
2	2-5	7.2 Port Configuration	57	Expression alignment
2	2-6	7.2 Port Configuration	57	Note alignment
2	2-7	7.4 List of Selectable Multiplexed Functions	84	Error correction
3	3-1	1.5 Base Addresses of the System Registers Area	-	Complement
3	3-2	2.1.14 CC-Link Pins (Intelligent Device Station)	20	Error correction
3	3-3	3. Memory Maps	40, 43	Note addition
3	3-4	8.2 Port Configuration	182	Expression alignment
3	3-5	8.2 Port Configuration	182	Note alignment
4	4-1	2.4 Operations for Reset	2-9	Complement
4	4-2	5.1 Selecting the Boot Mode (1) External Memory Boot Mode	5-1	Expression alignment
4	4-3	7.3.4.1 MIIM Register (GMAC_MIIM)	7-9	Expression alignment
4	4-4	7.3.4.5 RX MODE Register (GMAC_RXMODE)	7-12	Error correction
4	4-5	7.3.4.6 TX MODE Register (GMAC_TXMODE)	7-14	Error correction
4	4-6	7.3.4.6 TX MODE Register (GMAC_TXMODE)	7-14	Error correction
4	4-7	7.4.1.2 Flow of Processing for Issuing the Hardware Function Call ♦	7-32	Complement
4	4-8	7.4.1.3 Buffer Allocator	7-33	Error correction
4	4-9	7.4.1.3 Buffer Allocator	7-36	Error correction
4	4-10	7.4.1.3 Buffer Allocator	7-37	Error correction
4	4-11	7.4.1.4 MAC DMA Controller, (2) DMA for the Reception MAC	7-44	Error correction
4	4-12	7.4.1.4 MAC DMA Controller, (2) DMA for the Reception MAC	7-45	Error correction
4	4-13	7.4.1.4 MAC DMA Controller, (3) DMA for the Transmission MAC	7-50	Error correction

Doc. No. in this TU	Item No.	Revisions (Section Number)	Previous Edition's Page Number	Revision Type
4	4-14	7.4.1.4 MAC DMA Controller, (3) DMA for the Transmission MAC	7-50	Complement
4	4-15	7.4.1.5 Buffer RAM DMA Controller, (2) DMA Transfer	7-52	Error correction
4	4-16	7.4.1.5 Buffer RAM DMA Controller, (2) DMA Transfer	7-52	Error correction
4	4-17	7.4.2 Interrupts	7-56	Complement
4	4-18	7.4.2 Interrupts	7-58	Complement
4	4-19	7.5 Notes	-	Note addition
4	4-20	9.7 Memory Access Timing Examples	9-17 to 9-24	Expression alignment
4	4-21	9.7 Memory Access Timing Examples	9-20	Error correction
4	4-22	11.1 Memory Map	11-3	Note addition
4	4-23	11.1 Memory Map	11-3	Error correction
4	4-24	11.2.5 Control Registers (2) HOSTIF bus control register (HIFBCC)	11-17 11-18	Error correction
4	4-25	11.2.5 Control Registers (2) HOSTIF bus control register (HIFBCC)	11-18	Note addition
4	4-26	11.2.5 Control Registers (4) HOSTIF page ROM control register (HIFPRC)	11-20	Error correction
4	4-27	12.3 Connection with Serial Flash ROM	12-12	Expression alignment
4	4-28	13.1.1 Overview	13-2	Expression alignment
4	4-29	13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)	13-85	Note addition
4	4-30	13.6 Interrupt Output	13-89	Expression alignment
4	4-31	17.4.2 Master/Slave Connections	17-38, 17-39	Expression alignment
4	4-32	18.3 Registers (6) IICBn high-level width setting register	18-13	Error correction
4	4-33	18.6.1 Single Transfer Mode (3) Example of communications in single transfer mode (slave reception)	18-41	Error correction
4	4-34	21.7 System Protect Command Register (SYSPCMD)	21-7	Complement
4	4-35	22. Debugging	22-1	Expression alignment
5	5-1	12. Serial Flash ROM Connection Pins ♦	37	Error correction
5	5-2	17. CSIH Pins	-	Newly added
5	5-3	22.4 BSCAN Non-Supported Pins	49	Complement
5	5-4	22.6 Notes on Using BSDL	—	Newly added
5	5-5	25. Thermal Design	53	Expression alignment
5	5-6	26. Countermeasure for Noise	-	Newly added
6	6-1	1.2 Development Environment	2	Expression alignment
6	6-2	3.2.1 Memory Map	11, 12, 15, 16	Note addition
6	6-3	3.2.1 Memory Map	11, 12	Error correction
6	6-4	3.2.1 Memory Map	15, 16	Error correction
6	6-5	6.4.1 Initialization of IIC Controller ♦	35	Error correction
6	6-6	6.5.5 Confirmation of Received Data (for Slave)	46	Error correction
6	6-7	6.9 CAN Control	-	Newly added
7	7-1	3. Specified Parts and Recommended Parts	4	Complement
7	7-2	5. CC-Link Remote Device Station Pins	6, 8	Complement
7	7-3	6.1 Setting the Number of Occupied Stations	9	Complement
7	7-4	14.1 Circuit Design in General, (3) Questions and Answers Related to Switches, Connectors, and Terminal Blocks	72	Complement

No.1-1 1.3 Overview

Description of 1.5 V power supply for internal PHY was added.

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>3</td><td>[Table 1.2 Overview of R-IN32M3 (2/2)]
<table><tr><td>Power supply voltage</td><td>I/O: VDD33 = 3.3±0.3 V
Internal circuit :VDD10 = 1.0±0.1 V</td></tr></table></td><td>3</td><td>[Table 1.2 Overview of R-IN32M3 (2/2)]
<table><tr><td>Power supply voltage</td><td>I/O: VDD33 = 3.3±0.3 V
Internal circuit: VDD10 = 1.0±0.1 V
Power supply for internal PHY Note 2: VDD15 = 1.5±0.15V (internal regulator available)</td></tr></table></td></tr>
</table>

No.1-2 1.5 Memory Maps

Note regarding the instruction RAM mirror area was added.

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>6</td><td>[Figure 1.1 Memory Map (All) (R-IN32M3-EC)]

N/A</td><td>6</td><td>[Figure 1.1 Memory Map (All) (R-IN32M3-EC)]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.</td></tr>
<tr><td>7</td><td>[Figure 1.2 Memory Map (All) (R-IN32M3-CL)]

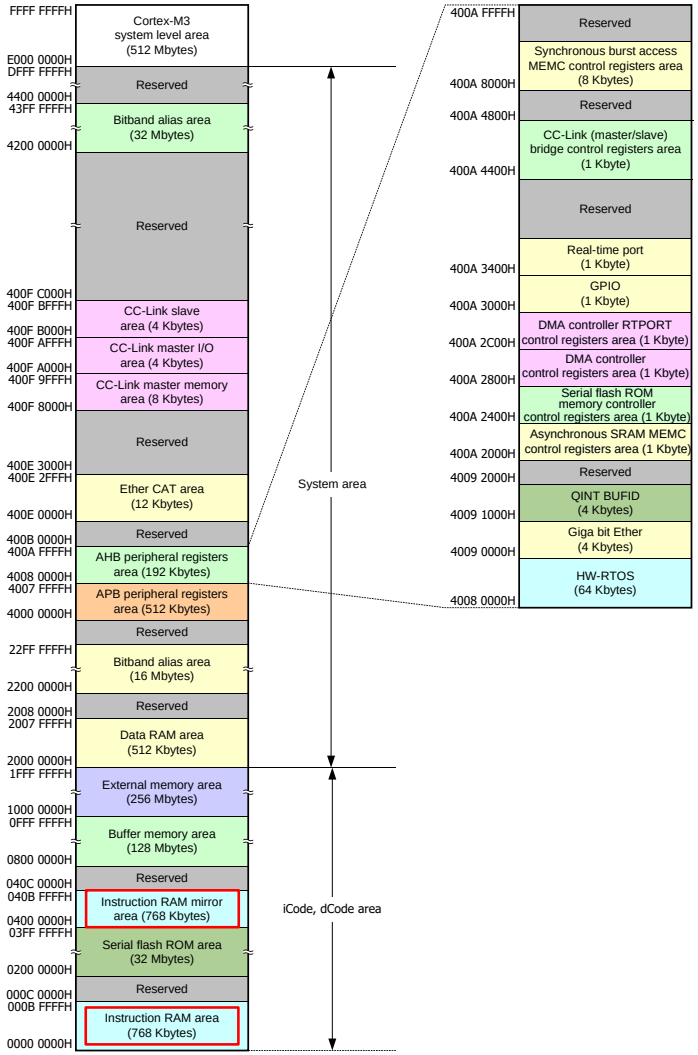
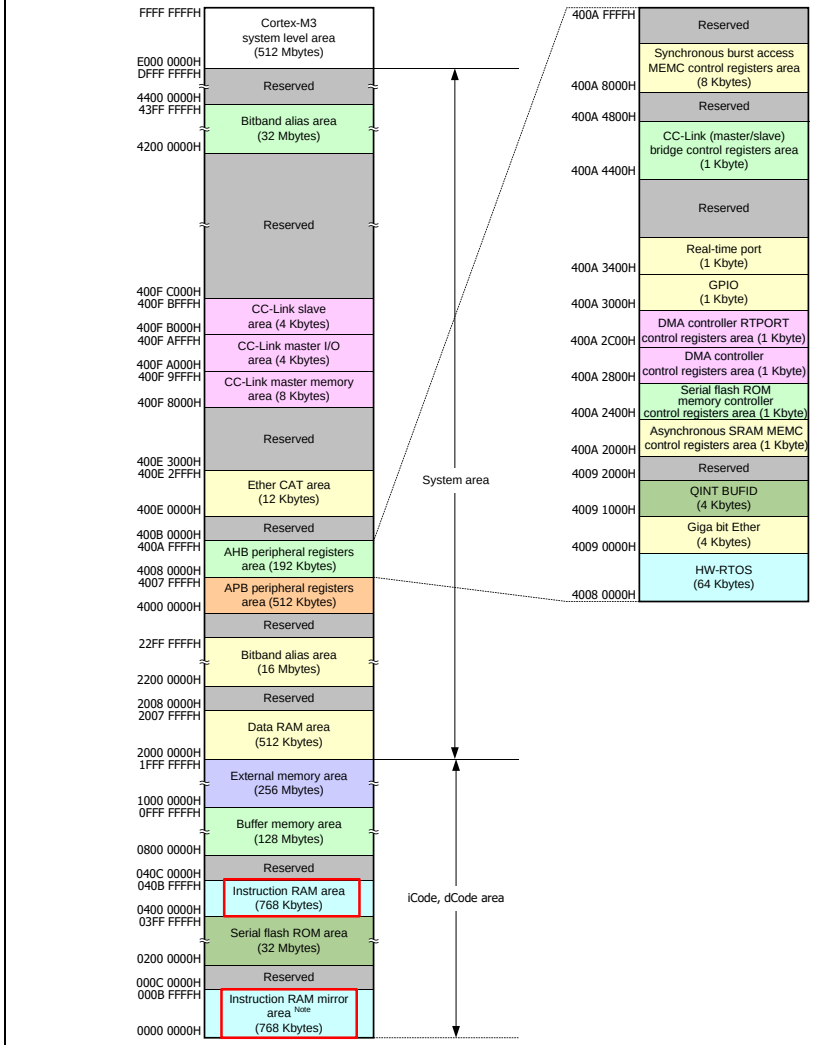
N/A</td><td>7</td><td>[Figure 1.2 Memory Map (All) (R-IN32M3-CL)]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.</td></tr>
<tr><td>10</td><td>[Figure 1.6 External MCU Interface Area (R-IN32M3-EC)]

N/A</td><td>10</td><td>[Figure 1.6 External MCU Interface Area (R-IN32M3-EC)]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr>
</table></td></tr>
<tr><td>11</td><td>[Figure 1.7 External MCU Interface Area (R-IN32M3-CL)]

N/A</td><td>11, 12</td><td>[Figure 1.7 External MCU Interface Area (R-IN32M3-CL)]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr>
</table></td></tr>
</table>

No.1-3 1.5 Memory Maps [1/2]

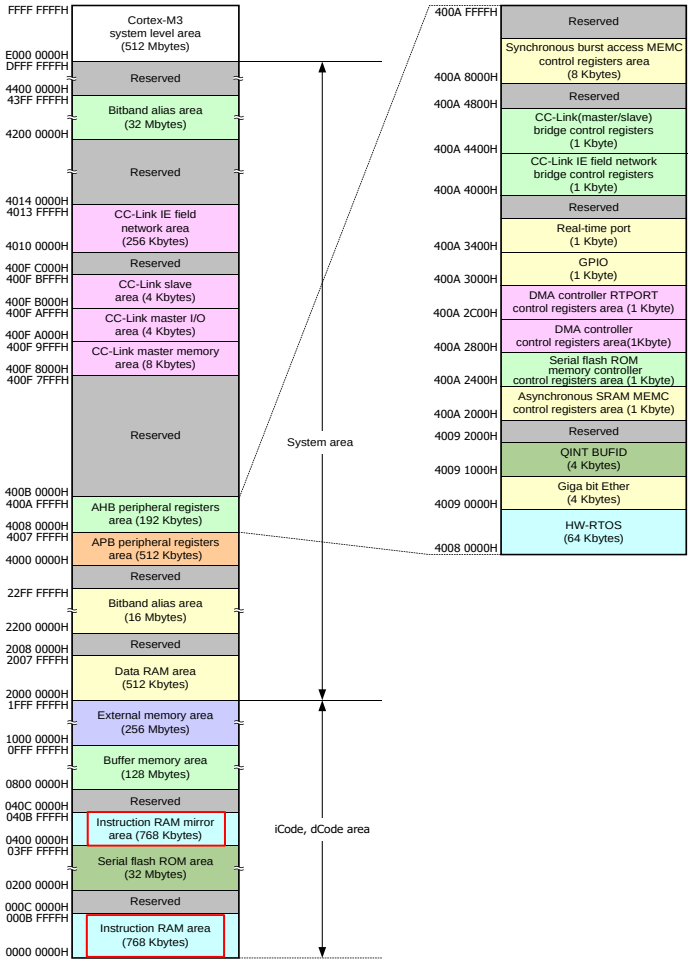
Locations of "Instruction RAM area" and "Instruction RAM mirror area" were corrected.

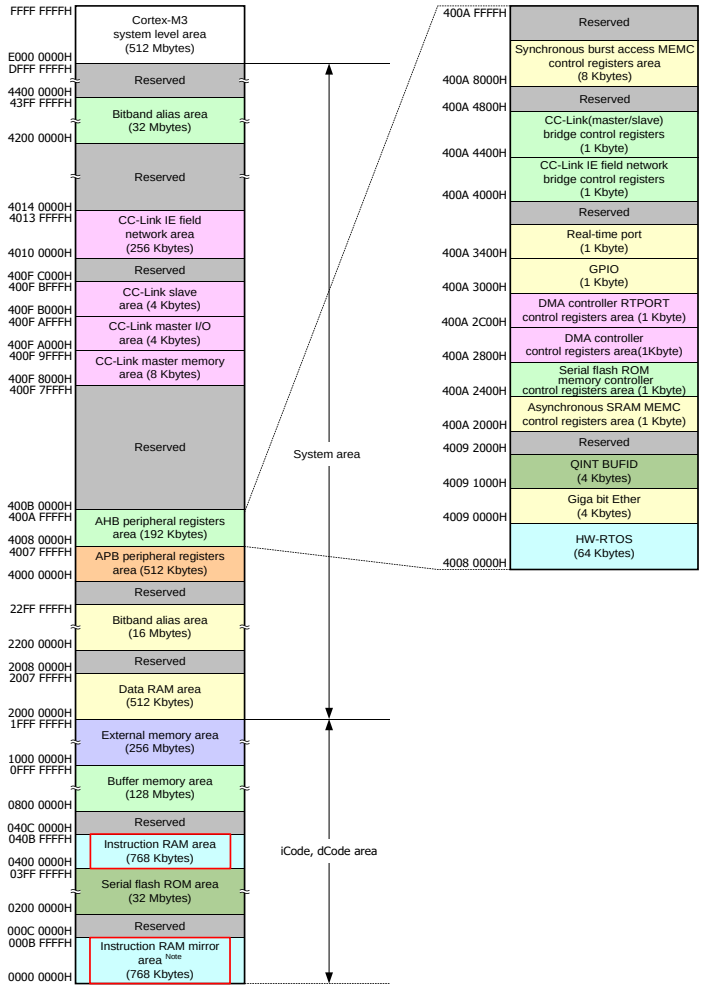
V4.01		V5.00	
Page	Description	Page	Revised Description
6	**[Figure 1.1 Memory Map (All) (R-IN32M3-EC)]** 	6	**[Figure 1.1 Memory Map (All) (R-IN32M3-EC)]** 

No.1-3 1.5 Memory Maps [2/2]

Locations of "Instruction RAM area" and "Instruction RAM mirror area" were corrected.

V4.01		V5.00	
Page	Description	Page	Revised Description
7	**[Figure 1.2 Memory Map (All) (R-IN32M3-CL)]**	7	**[Figure 1.2 Memory Map (All) (R-IN32M3-CL)]**

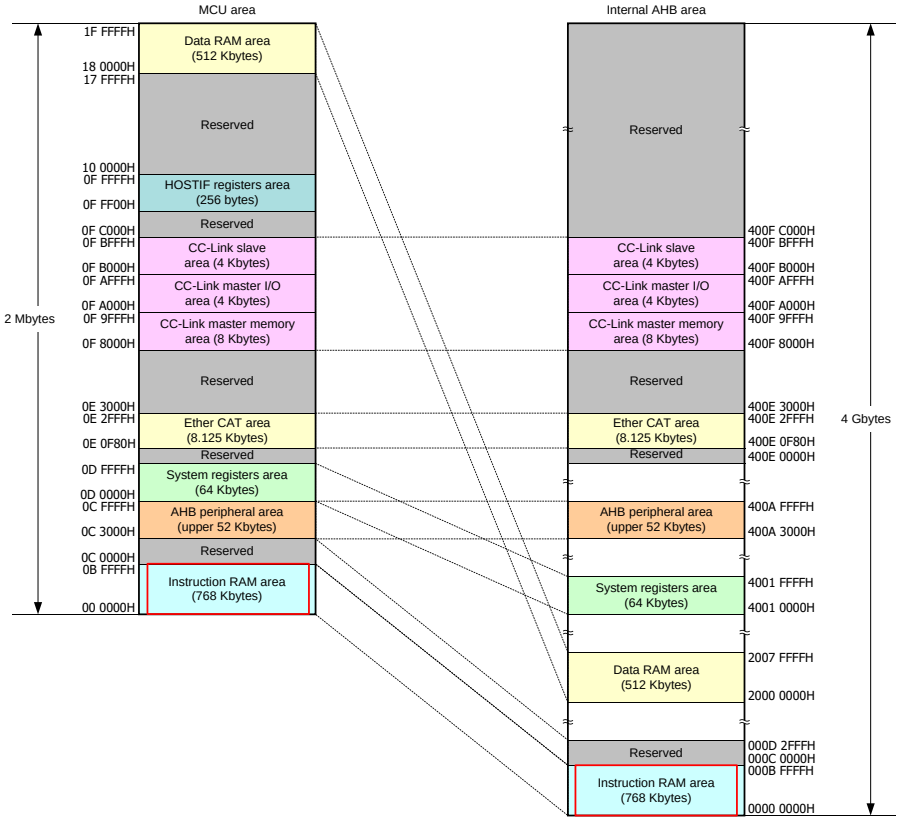


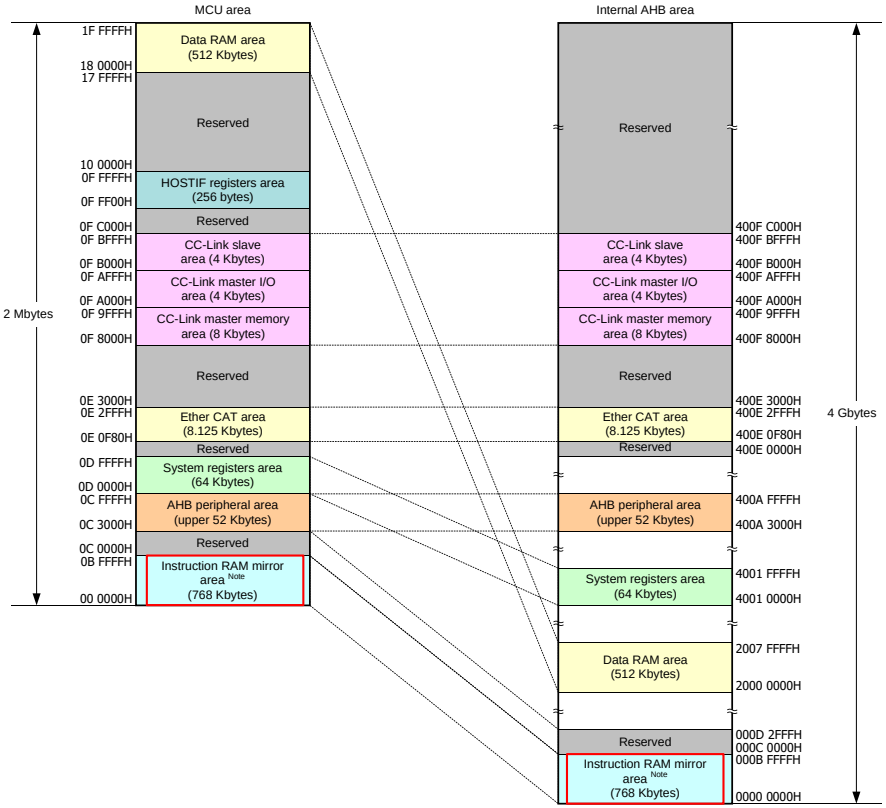


No.1-4 1.5 Memory Maps [1/2]

"Instruction RAM area" was corrected to "Instruction RAM mirror area".

V4.01		V5.00	
Page	Description	Page	Revised Description
10	**[Figure 1.6 External MCU Interface Area (R-IN32M3-EC)]**	10	**[Figure 1.6 External MCU Interface Area (R-IN32M3-EC)]**

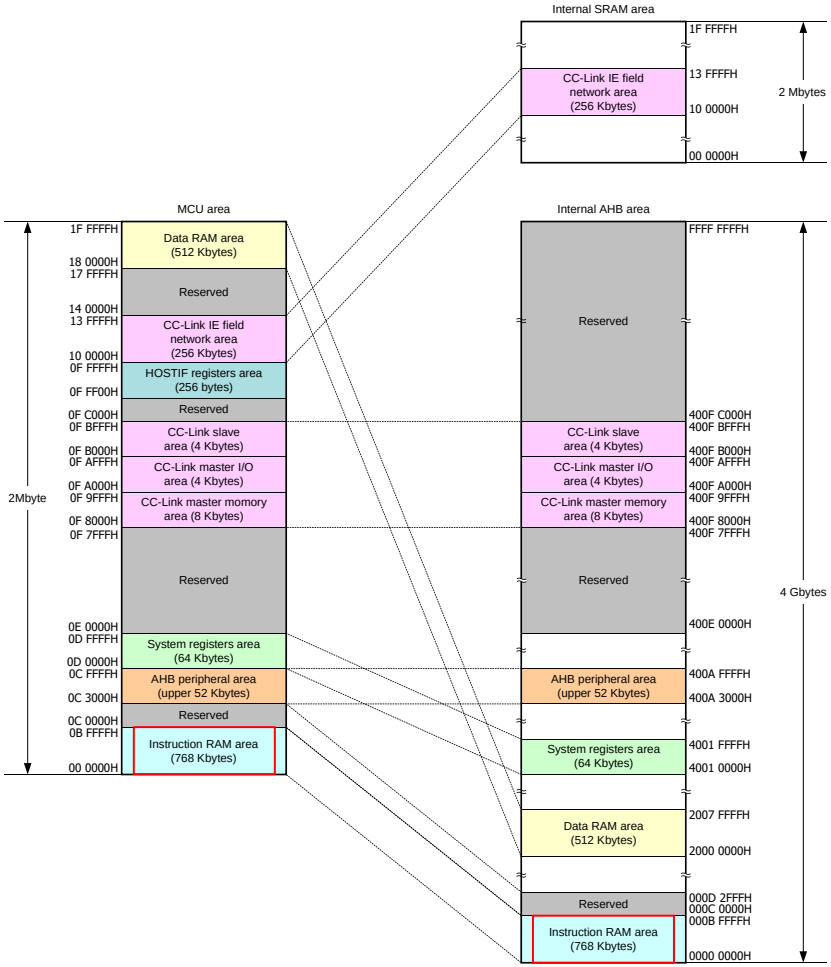


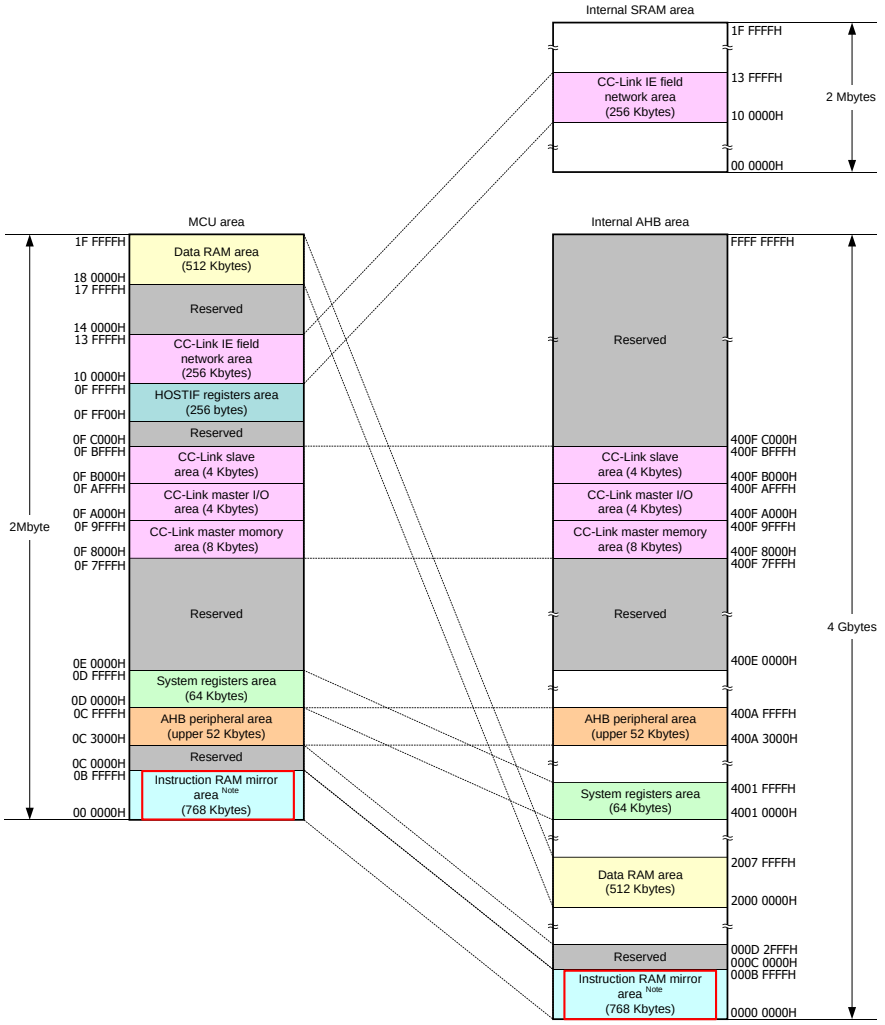


No.1-4 1.5 Memory Maps [2/2]

"Instruction RAM area" was corrected to "Instruction RAM mirror area".

V4.01		V5.00	
Page	Description	Page	Revised Description
11	**[Figure 1.7 External MCU Interface Area (R-IN32M3-CL)]**	11	**[Figure 1.7 External MCU Interface Area (R-IN32M3-CL)]**





No.1-5 2.3.5 Port Pins and Real-time Port Pins

The pin name indicated as "CCM_IRZ" was modified to "CCM_IRLZ".

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>22</td><td>[2.3.5 Port Pins and Real-time Port Pins]
<table>
<tr><th></th><th>Port Name</th><th>Mode 1</th><th>Mode 2</th><th>Mode 3</th><th>Mode 4</th><th>Level during Reset</th></tr>
<tr><td rowspan="8">P3</td><td>P30</td><td>RXD1</td><td>-</td><td>-</td><td>-</td><td rowspan="8">Hi-Z (High)</td></tr>
<tr><td>P31</td><td>TXD1</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>P32</td><td>DMAREQZ1</td><td>-</td><td>-</td><td>CCS_MON1</td></tr>
<tr><td>P33</td><td>DMAACKZ1</td><td>CCI_WAITEDGEH Note2</td><td>-</td><td>CCS_MON2</td></tr>
<tr><td>P34</td><td>DMATCZ1</td><td>CCI_WRLENH Note2</td><td>-</td><td>CCS_MON3</td></tr>
<tr><td>P35</td><td>CSISCK1</td><td>INTPZ22</td><td>CCM_IRZ</td><td>-</td></tr>
<tr><td>P36</td><td>CSISI1</td><td>INTPZ23</td><td>CCS_FUSEZ</td><td>-</td></tr>
<tr><td>P37</td><td>CSISO1</td><td>INTPZ24</td><td>CCM_MSTZ</td><td>-</td></tr>
</table></td><td>23</td><td>[2.3.5 Port Pins and Real-time Port Pins]
<table>
<tr><th></th><th>Port Name</th><th>Mode 1</th><th>Mode 2</th><th>Mode 3</th><th>Mode 4</th><th>Level during Reset</th></tr>
<tr><td rowspan="8">P3</td><td>P30</td><td>RXD1</td><td>-</td><td>-</td><td>-</td><td rowspan="8">Hi-Z (High)</td></tr>
<tr><td>P31</td><td>TXD1</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>P32</td><td>DMAREQZ1</td><td>-</td><td>-</td><td>CCS_MON1</td></tr>
<tr><td>P33</td><td>DMAACKZ1</td><td>CCI_WAITEDGEH Note2</td><td>-</td><td>CCS_MON2</td></tr>
<tr><td>P34</td><td>DMATCZ1</td><td>CCI_WRLENH Note2</td><td>-</td><td>CCS_MON3</td></tr>
<tr><td>P35</td><td>CSISCK1</td><td>INTPZ22</td><td>CCM_IRLZ</td><td>-</td></tr>
<tr><td>P36</td><td>CSISI1</td><td>INTPZ23</td><td>CCS_FUSEZ</td><td>-</td></tr>
<tr><td>P37</td><td>CSISO1</td><td>INTPZ24</td><td>CCM_MSTZ</td><td>-</td></tr>
</table></td></tr>
</table>

No.1-6 2.3.15 CC-Link Pins (Intelligent Device Station)

Functional descriptions of the CC-Link (intelligent device station) pins were modified.

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>30</td><td>[2.3.15 CC-Link Pins (Intelligent Device Station)]
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th><th>Level during Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>O</td><td>Link error LED control output</td><td>P20</td><td>Low</td><td rowspan="5">Note</td></tr>
<tr><td>CCM_ERRZ</td><td>O</td><td>Error LED control output</td><td>P21</td><td>Low</td></tr>
<tr><td>CCM_RUNZ</td><td>O</td><td>Run LED control output</td><td>P26</td><td>Low</td></tr>
<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>I</td><td>Transfer rate and mode setting switch input</td><td>P62-P65</td><td>-</td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>I</td><td>Station no. setting switch input</td><td>P70-P77</td><td>-</td></tr>
<tr><td>CCM_LNKRUNZ</td><td>O</td><td>Link run LED control output</td><td>P50</td><td>Low</td><td rowspan="12">Hi-Z
(High)</td></tr>
<tr><td>CCM_RDLEDZ</td><td>O</td><td>Receive data LED control output</td><td>P51</td><td>Low</td></tr>
<tr><td>CCM_SDLEDZ</td><td>O</td><td>Transfer data LED control output</td><td>RP00</td><td>Low</td></tr>
<tr><td>CCM_IRZ</td><td>O</td><td>Interrupt output</td><td>P35</td><td>Low</td></tr>
<tr><td>CCM_WDTENZ</td><td>I</td><td>Watchdog timer error input</td><td>P13</td><td>Low</td></tr>
<tr><td>CCM_MSTZ</td><td>O</td><td>Operation check LED</td><td>P37</td><td>Low</td></tr>
<tr><td>CCM_SMSTZ</td><td>O</td><td>Standby master LED control output</td><td>RP01</td><td>Low</td></tr>
<tr><td>CCM_RD</td><td>I</td><td>Communications circuit data reception</td><td>P53</td><td>-</td></tr>
<tr><td>CCM_SD</td><td>O</td><td>Communications circuit data transmission pin</td><td>P54</td><td>-</td></tr>
<tr><td>CCM_SDGCZ</td><td>O</td><td>Communications circuit transmit data & gate control pin</td><td>P42</td><td>Low</td></tr>
<tr><td>CCM_CLK80M</td><td>I</td><td>CC-Link clock input (80 MHz)</td><td>-</td><td>-</td><td>-</td></tr>
</table></td><td>31</td><td>[2.3.15 CC-Link Pins (Intelligent Device Station)]
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th><th>Level during Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>O</td><td>Link error LED control output</td><td>P20</td><td>Low</td><td rowspan="5">Note</td></tr>
<tr><td>CCM_ERRZ</td><td>O</td><td>Not used</td><td>P21</td><td>Low</td></tr>
<tr><td>CCM_RUNZ</td><td>O</td><td>Run LED control output</td><td>P26</td><td>Low</td></tr>
<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>I</td><td>Transfer rate setting input</td><td>P62-P65</td><td>-</td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>I</td><td>Station no. setting switch input</td><td>P70-P77</td><td>-</td></tr>
<tr><td>CCM_LNKRUNZ</td><td>O</td><td>Link run LED control output</td><td>P50</td><td>Low</td><td rowspan="12">Hi-Z
(High)</td></tr>
<tr><td>CCM_RDLEDZ</td><td>O</td><td>Receive data LED control output</td><td>P51</td><td>Low</td></tr>
<tr><td>CCM_SDLEDZ</td><td>O</td><td>Transfer data LED control output</td><td>RP00</td><td>Low</td></tr>
<tr><td>CCM_IRLZ</td><td>O</td><td>Interrupt signal output from communications circuit</td><td>P35</td><td>Low</td></tr>
<tr><td>CCM_WDTENZ</td><td>I</td><td>Watchdog timer error input</td><td>P13</td><td>Low</td></tr>
<tr><td>CCM_MSTZ</td><td>O</td><td>Not used</td><td>P37</td><td>Low</td></tr>
<tr><td>CCM_SMSTZ</td><td>O</td><td>Not used</td><td>RP01</td><td>Low</td></tr>
<tr><td>CCM_RD</td><td>I</td><td>Communications circuit data reception</td><td>P53</td><td>-</td></tr>
<tr><td>CCM_SD</td><td>O</td><td>Communications circuit data transmission pin</td><td>P54</td><td>-</td></tr>
<tr><td>CCM_SDGCZ</td><td>O</td><td>Communications circuit transmit data & gate control pin</td><td>P42</td><td>Low</td></tr>
<tr><td>CCM_CLK80M</td><td>I</td><td>CC-Link clock input (80 MHz)</td><td>-</td><td>-</td><td>-</td></tr>
</table></td></tr>
</table>

No.1-7 4.2 Absolute Maximum Ratings

1.5 V type was added as the condition for power supply

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>69</td><td>[Table 4.4 Absolute Maximum Ratings]
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>Ratings</th><th>Unit</th></tr>
<tr><td rowspan="2">Power supply voltage</td><td rowspan="2">V_{DD}</td><td>1.0 V type</td><td>−0.5 to +1.4</td><td>V</td></tr>
<tr><td>3.3 V type</td><td>−0.5 to +4.6</td><td>V</td></tr>
</table></td><td>70</td><td>[Table 4.4 Absolute Maximum Ratings]
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>Ratings</th><th>Unit</th></tr>
<tr><td rowspan="3">Power supply voltage</td><td rowspan="3">V_{DD}</td><td>1.0 V type</td><td>−0.5 to +1.4</td><td>V</td></tr>
<tr><td>1.5 V type</td><td>−0.5 to +2.0</td><td>V</td></tr>
<tr><td>3.3 V type</td><td>−0.5 to +4.6</td><td>V</td></tr>
</table></td></tr>
</table>

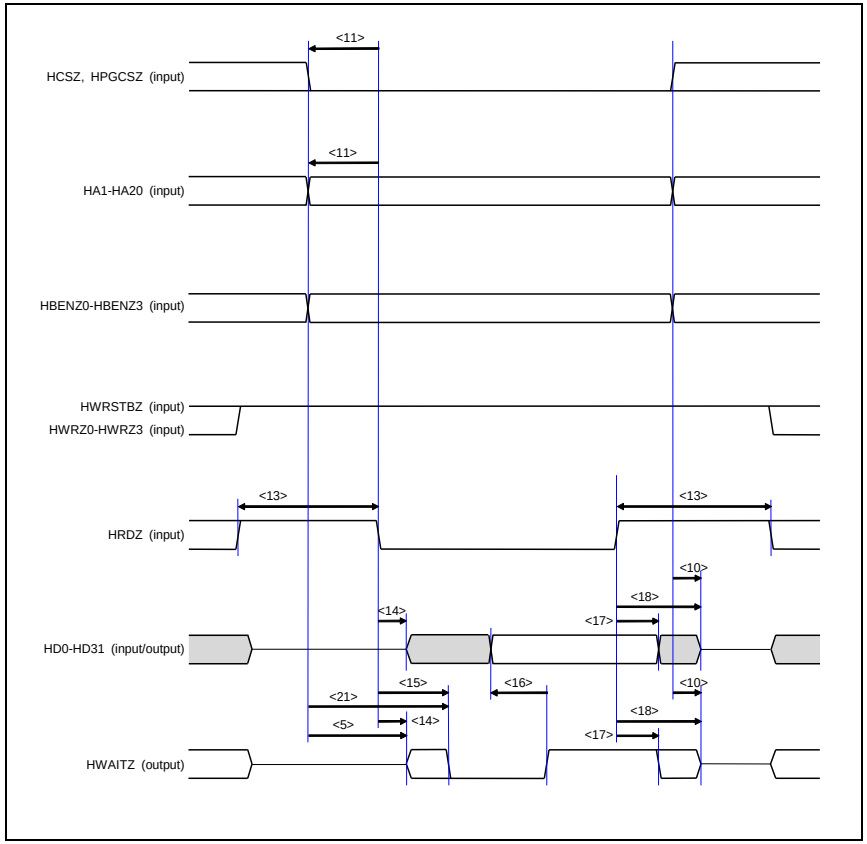
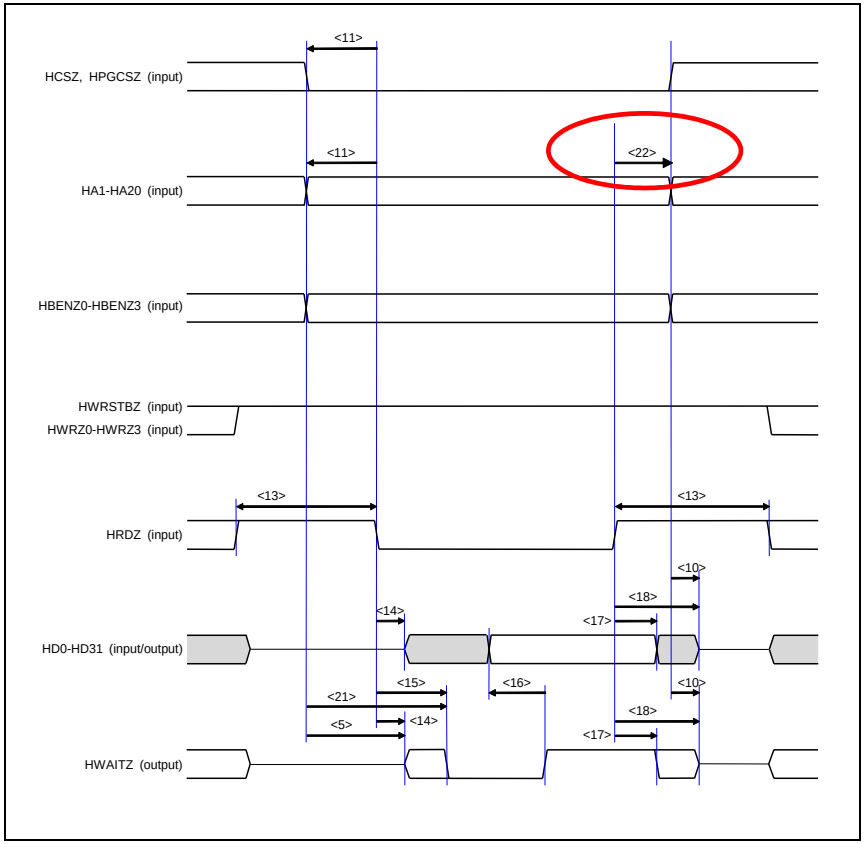
No.1-8 4.3 Recommended Operating Conditions

1.5 V power supply was added as the condition for power supply voltage.

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>70</td><td>[Table 4.5 Recommended Operating Conditions]
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>MIN.</th><th>TYP.</th><th>MAX.</th><th>Unit</th></tr>
<tr><td rowspan="2">Power supply voltage</td><td rowspan="2">V_{DD}</td><td>1.0 V power supply</td><td>0.9</td><td>1.0</td><td>1.1</td><td>V</td></tr>
<tr><td>3.3 V power supply</td><td>3.0</td><td>3.3</td><td>3.6</td><td>V</td></tr>
</table></td><td>71</td><td>[Table 4.5 Recommended Operating Conditions]
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>MIN.</th><th>TYP.</th><th>MAX.</th><th>Unit</th></tr>
<tr><td rowspan="3">Power supply voltage</td><td rowspan="3">V_{DD}</td><td>1.0 V power supply</td><td>0.9</td><td>1.0</td><td>1.1</td><td>V</td></tr>
<tr><td>1.5 V power supply</td><td>1.35</td><td>1.5</td><td>1.65</td><td>V</td></tr>
<tr><td>3.3 V power supply</td><td>3.0</td><td>3.3</td><td>3.6</td><td>V</td></tr>
</table></td></tr>
</table>

No.1-9 4.8.4 External MCU Interface Pins (3) Asynchronous Mode

Specification of "Address input hold time when advance reading" was added.

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>92</td><td>[4.8.4 External MCU Interface Pins (3) Asynchronous Mode]
<table>
<tr><th>No.</th><th>Parameter</th><th>Symbol</th><th>MIN</th><th>MAX</th><th>Unit</th></tr>
<tr><td colspan="6">N/A</td></tr>
</table></td><td>93</td><td>[4.8.4 External MCU Interface Pins (3) Asynchronous Mode]
<table>
<tr><th>No.</th><th>Parameter</th><th>Symbol</th><th>MIN</th><th>MAX</th><th>Unit</th></tr>
<tr><td>22</td><td>Address input hold time when advance reading is enabled (from HRDZ↑)</td><td>$t_{ADDRDHP}$</td><td>4.3</td><td>–</td><td>ns</td></tr>
</table></td></tr>
<tr><td>94</td><td>[Figure 4.14 External MCU Read Timing (MEMCSEL = L, HIFSYNC = L)]
 
</td><td>95</td><td>[Figure 4.14 External MCU Read Timing (MEMCSEL = L, HIFSYNC = L)]
 
</td></tr>
</table>

No.1-10 4.8.5 Serial Flash ROM Interface

Specifications of $t_{DSMCSCK}$ and $t_{DSMCKCS}$ were

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>99</td><td>[4.8.5 Serial Flash ROM Interface]
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>MIN</th><th>MAX</th><th>Unit</th></tr>
<tr><td>Delay time from a falling of SMCSZ to a rising of SMSCK</td><td>$t_{DSMCSCK}$</td><td>C_L = 15 pF
Freq = 50 MHz</td><td>7.5 Note</td><td>–</td><td>ns</td></tr>
<tr><td>Hold time until a rising of SMCSZ from a rising of SMSCK</td><td>$t_{DSMCKCS}$</td><td>C_L = 15 pF
Freq = 50 MHz</td><td>11.5 Note</td><td>–</td><td>ns</td></tr>
</table></td><td>100</td><td>[4.8.5 Serial Flash ROM Interface]
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Conditions</th><th>MIN</th><th>MAX</th><th>Unit</th></tr>
<tr><td>Delay time from a falling of SMCSZ to a rising of SMSCK</td><td>$t_{DSMCSCK}$</td><td>C_L = 15 pF
Freq = 50 MHz</td><td>6.0 Note</td><td>–</td><td>ns</td></tr>
<tr><td>Hold time until a rising of SMCSZ from a rising of SMSCK</td><td>$t_{DSMCKCS}$</td><td>C_L = 15 pF
Freq = 50 MHz</td><td>9.0 Note</td><td>–</td><td>ns</td></tr>
</table></td></tr>
</table>

No.2-1 1.5 Base Addresses of the System Registers Area

The description on the base addresses of the system registers area was added.

<table>
<tr><th colspan="2">V3.01</th><th colspan="2">V4.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>-</td><td>[1.5 Base Addresses of the System Registers Area]

N/A</td><td>6</td><td>[1.5 Base Addresses of the System Registers Area]
1.5 Base Addresses of the System Registers Area
The addresses of registers given in the subsequent sections are relative to the base addresses. In access to the registers via the external MCU interface, the base address is D_0000H. In access by the internal CPU or DMA controller, the base address is 4001_0000H.
• In access by the CPU or DMA controller
BASE = 4001_0000H
• In access via the external microcontroller interface
BASE = D_0000H</td></tr>
</table>

No.2-2 2.1.4 Port Pins and Real-Time Port Pins

The pin name indicated as "CCM_IRZ" was modified to "CCM_IRLZ".

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>12</td><td>[2.1.4 Port Pins and Real-Time Port Pins]
<table>
<tr><th></th><th>Pin Name</th><th>Mode 1</th><th>Mode 2</th><th>Mode 3</th><th>Mode 4</th><th>Level during & after Reset</th></tr>
<tr><td rowspan="8">P3</td><td>P30</td><td>RXD1</td><td>-</td><td>-</td><td>-</td><td rowspan="8">Hi-Z (High)</td></tr>
<tr><td>P31</td><td>TXD1</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>P32</td><td>DMAREQZ1</td><td>-</td><td>-</td><td>CCS_MON1</td></tr>
<tr><td>P33</td><td>DMAACKZ1</td><td>CCI_ WAITEDGEH</td><td>-</td><td>CCS_MON2</td></tr>
<tr><td>P34</td><td>DMATCZ1</td><td>CCI_WRLENH</td><td>-</td><td>CCS_MON3</td></tr>
<tr><td>P35</td><td>CSISCK1</td><td>INTPZ22</td><td>CCM_IRZ</td><td>-</td></tr>
<tr><td>P36</td><td>CSISI1</td><td>INTPZ23</td><td>CCS_FUSEZ</td><td>-</td></tr>
<tr><td>P37</td><td>CSISO1</td><td>INTPZ24</td><td>CCM_MSTZ</td><td>-</td></tr>
</table></td><td>13</td><td>[2.1.4 Port Pins and Real-Time Port Pins]
<table>
<tr><th></th><th>Pin Name</th><th>Mode 1</th><th>Mode 2</th><th>Mode 3</th><th>Mode 4</th><th>Level during & after Reset</th></tr>
<tr><td rowspan="8">P3</td><td>P30</td><td>RXD1</td><td>-</td><td>-</td><td>-</td><td rowspan="8">Hi-Z (High)</td></tr>
<tr><td>P31</td><td>TXD1</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>P32</td><td>DMAREQZ1</td><td>-</td><td>-</td><td>CCS_MON1</td></tr>
<tr><td>P33</td><td>DMAACKZ1</td><td>CCI_ WAITEDGEH</td><td>-</td><td>CCS_MON2</td></tr>
<tr><td>P34</td><td>DMATCZ1</td><td>CCI_WRLENH</td><td>-</td><td>CCS_MON3</td></tr>
<tr><td>P35</td><td>CSISCK1</td><td>INTPZ22</td><td>CCM_IRLZ</td><td>-</td></tr>
<tr><td>P36</td><td>CSISI1</td><td>INTPZ23</td><td>CCS_FUSEZ</td><td>-</td></tr>
<tr><td>P37</td><td>CSISO1</td><td>INTPZ24</td><td>CCM_MSTZ</td><td>-</td></tr>
</table></td></tr>
</table>

No.2-3 2.1.14 CC-Link Pins (Intelligent Device Station)

The name and functional descriptions of the CC-Link (intelligent device station) pins were modified.

<table>
<tr><th colspan="2">V3.01</th><th colspan="2">V4.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>19</td><td>[2.1.14 CC-Link Pins (Intelligent Device Station)]
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th><th>Level during & after Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>O</td><td>Link error LED control output</td><td>P20</td><td>Low</td><td>Hi-Z (High)</td></tr>
<tr><td>CCM_ERRZ</td><td>O</td><td>Error LED control output</td><td>P21</td><td>Low</td><td></td></tr>
<tr><td>CCM_RUNZ</td><td>O</td><td>Run LED control output</td><td>P26</td><td>Low</td><td></td></tr>
<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>I</td><td>Transfer rate and mode setting switch input</td><td>P62-P65</td><td>-</td><td></td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>I</td><td>Station no. setting switch input</td><td>P70-P77</td><td>-</td><td></td></tr>
<tr><td>CCM_LNKRUNZ</td><td>O</td><td>Link run LED control output</td><td>P50</td><td>Low</td><td></td></tr>
<tr><td>CCM_RDLEDZ</td><td>O</td><td>Receive data LED control output</td><td>P51</td><td>Low</td><td></td></tr>
<tr><td>CCM_SDLEDZ</td><td>O</td><td>Transmit data LED control output</td><td>RP00</td><td>Low</td><td></td></tr>
<tr><td>CCM_IRZ</td><td>O</td><td>Interrupt output</td><td>P35</td><td>Low</td><td></td></tr>
<tr><td>CCM_WDTENZ</td><td>I</td><td>Watchdog timer error input</td><td>P13</td><td>Low</td><td></td></tr>
<tr><td>CCM_MSTZ</td><td>O</td><td>Operation check LED</td><td>P37</td><td>Low</td><td></td></tr>
<tr><td>CCM_SMSTZ</td><td>O</td><td>Standby master LED control output</td><td>RP01</td><td>Low</td><td></td></tr>
<tr><td>CCM_RD</td><td>I</td><td>Communications circuit data reception pin</td><td>P53</td><td>-</td><td></td></tr>
<tr><td>CCM_SD</td><td>O</td><td>Communications circuit data transmission pin</td><td>P54</td><td>-</td><td></td></tr>
<tr><td>CCM_SDGCZ</td><td>O</td><td>Communications circuit transmit data & gate control pin</td><td>P42</td><td>Low</td><td></td></tr>
<tr><td>CCM_CLK80M</td><td>I</td><td>CC-Link clock (80 MHz)</td><td>-</td><td>-</td><td>-</td></tr>
</table></td><td>20</td><td>[2.1.14 CC-Link Pins (Intelligent Device Station)]
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th><th>Level during & after Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>O</td><td>Link error LED control output</td><td>P20</td><td>Low</td><td>Hi-Z (High)</td></tr>
<tr><td>CCM_ERRZ</td><td>O</td><td>Not used</td><td>P21</td><td>Low</td><td></td></tr>
<tr><td>CCM_RUNZ</td><td>O</td><td>Run LED control output</td><td>P26</td><td>Low</td><td></td></tr>
<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>I</td><td>Transfer rate setting input</td><td>P62-P65</td><td>-</td><td></td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>I</td><td>Station no. setting switch input</td><td>P70-P77</td><td>-</td><td></td></tr>
<tr><td>CCM_LNKRUNZ</td><td>O</td><td>Link run LED control output</td><td>P50</td><td>Low</td><td></td></tr>
<tr><td>CCM_RDLEDZ</td><td>O</td><td>Receive data LED control output</td><td>P51</td><td>Low</td><td></td></tr>
<tr><td>CCM_SDLEDZ</td><td>O</td><td>Transmit data LED control output</td><td>RP00</td><td>Low</td><td></td></tr>
<tr><td>CCM_IRLZ</td><td>O</td><td>Interrupt signal output from communications circuit</td><td>P35</td><td>Low</td><td></td></tr>
<tr><td>CCM_WDTENZ</td><td>I</td><td>Watchdog timer error input</td><td>P13</td><td>Low</td><td></td></tr>
<tr><td>CCM_MSTZ</td><td>O</td><td>Note used</td><td>P37</td><td>Low</td><td></td></tr>
<tr><td>CCM_SMSTZ</td><td>O</td><td>Note used</td><td>RP01</td><td>Low</td><td></td></tr>
<tr><td>CCM_RD</td><td>I</td><td>Communications circuit data reception pin</td><td>P53</td><td>-</td><td></td></tr>
<tr><td>CCM_SD</td><td>O</td><td>Communications circuit data transmission pin</td><td>P54</td><td>-</td><td></td></tr>
<tr><td>CCM_SDGCZ</td><td>O</td><td>Communications circuit transmit data & gate control pin</td><td>P42</td><td>Low</td><td></td></tr>
<tr><td>CCM_CLK80M</td><td>I</td><td>CC-Link clock (80 MHz)</td><td>-</td><td>-</td><td>-</td></tr>
</table></td></tr>
</table>

No.2-4 3 Memory Maps

Note regarding the instruction RAM mirror area was

<table>
<tr><th colspan="2">V3.01</th><th colspan="2">V4.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>40</td><td>[Figure 3.1 Memory Map (All)]

N/A</td><td>41</td><td>[Figure 3.1 Memory Map (All)]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.</td></tr>
<tr><td>43</td><td>[Figure 3.5 External MCU Interface Area]

N/A</td><td>44</td><td>[Figure 3.5 External MCU Interface Area]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr>
</table></td></tr>
</table>

No.2-5 7.2 Port Configuration

"Application and Operation" for the port function control registers and the port function control expansion registers was modified.

<table>
<tr><th colspan="2">V3.01</th><th colspan="2">V4.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>57</td><td>[7.2 Port Configuration]
<table><tr><th rowspan="2">Register Name</th><th colspan="2">Application and Operation</th></tr><tr><th>Read</th><th>Write</th></tr><tr><td>Port function control registers (PFCn, RPFCm)</td><td>If more than two pin functions are multiplexed on port pins, the corresponding register is used to read which functions are selected.</td><td>If more than two pin functions are multiplexed on port pins, the corresponding register is used to select which functions are to be used.</td></tr><tr><td>Port function control expansion registers (PFCEn, RPFCEm)</td><td>If more than three pin functions are multiplexed on port pins, the corresponding register is used to read which functions are selected.</td><td>If more than three pin functions are multiplexed on port pins, the corresponding register is used to select which functions are to be used in combination with the PFCn register.</td></tr></table></td><td>58</td><td>[7.2 Port Configuration]
<table><tr><th rowspan="2">Register Name</th><th colspan="2">Application and Operation</th></tr><tr><th>Read</th><th>Write</th></tr><tr><td>Port function control registers (PFCn, RPFCm)</td><td rowspan="2">Used to read which function is selected for the multiplexed pin.</td><td rowspan="2">Used to select the function of the multiplexed pin.</td></tr><tr><td>Port function control expansion registers (PFCEn, RPFCEm)</td></tr></table></td></tr>
</table>

No.2-6 7.2 Port Configuration

Caution on the port configuration was modified.

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>57</td><td>[7.2 Port Configuration]
Caution: If a port pin having multiple multiplexed functions which include an external interrupt input is set to control mode by using the PMCn and RPMCm registers, and the multiplexed function is an input, the external interrupt input is also multiplexed.</td><td>58</td><td>[7.2 Port Configuration]
Caution: Operation is not guaranteed if an unsupported function is allocated to the multiplexed pin. For example, if multiplexed function 4 is allocated to the P00 pin, which does not support multiplexed function 4, operation does not proceed correctly. For the allocation of multiplexed pins, see section 7.4, List of Selectable Multiplexed Functions.</td></tr>
</table>

No.2-7 7.4 List of Selectable Multiplexed Functions

Pins name indicated as "CCM_IRZ" was modified to "CCM_IRLZ".

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>84</td><td>[(1) Ports (P00 to P77) (2/3)]
<table>
<tr><th rowspan="3">Pin Name</th><th colspan="2" rowspan="2">PMCmn = 0 (Port Mode)</th><th colspan="4">PMCmn = 1 (Control Mode)</th></tr>
<tr><th colspan="2">PFCEmn = 0</th><th colspan="2">PFCEmn = 1</th></tr>
<tr><th>PMmn = 0 (Output Port)</th><th>PMmn = 1 (Input Port)</th><th>PFCmn = 0 (Multiplexed Function 1)</th><th>PFCmn = 1 (Multiplexed Function 2)</th><th>PFCmn = 0 (Multiplexed Function 3)</th><th>PFCmn = 1 (Multiplexed Function 4)</th></tr>
<tr><td>P35</td><td>P35 (output mode)</td><td>P35 (input mode)</td><td>CSISCK1</td><td>INTPZ22</td><td>CCM_IRZ</td><td>-</td></tr>
</table></td><td>86</td><td>[(1) Ports (P00 to P77) (2/3)]
<table>
<tr><th rowspan="3">Pin Name</th><th colspan="2" rowspan="2">PMCmn = 0 (Port Mode)</th><th colspan="4">PMCmn = 1 (Control Mode)</th></tr>
<tr><th colspan="2">PFCEmn = 0</th><th colspan="2">PFCEmn = 1</th></tr>
<tr><th>PMmn = 0 (Output Port)</th><th>PMmn = 1 (Input Port)</th><th>PFCmn = 0 (Multiplexed Function 1)</th><th>PFCmn = 1 (Multiplexed Function 2)</th><th>PFCmn = 0 (Multiplexed Function 3)</th><th>PFCmn = 1 (Multiplexed Function 4)</th></tr>
<tr><td>P35</td><td>P35 (output mode)</td><td>P35 (input mode)</td><td>CSISCK1</td><td>INTPZ22</td><td>CCM_IRLZ</td><td>-</td></tr>
</table></td></tr>
</table>

No.3-1 1.5 Base Addresses of the System Registers Area

The description on the base addresses of the system registers area was added.

V4.01		V5.00	
Page	Description	Page	Revised Description
-	**[1.5 Base Addresses of the System Registers Area]** N/A	6	**[1.5 Base Addresses of the System Registers Area]** 1.5 Base Addresses of the System Registers Area The addresses of registers given in the subsequent sections are relative to the base addresses. In access to the registers via the external MCU interface, the base address is D_0000H. In access by the internal CPU or DMA controller, the base address is 4001_0000H. • In access by the CPU or DMA controller BASE = 4001_0000H • In access via the external microcontroller interface BASE = D_0000H

No.3-2 2.1.14 CC-Link Pins (Intelligent Device Station)

Functional descriptions of the CC-Link (intelligent device station) pins were modified.

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>20</td><td>[2.1.14 CC-Link Pins (Intelligent Device Station)]
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th><th>Level during & after Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>O</td><td>Link error LED control output</td><td>P20</td><td>Low</td><td>Hi-Z</td></tr>
<tr><td>CCM_ERRZ</td><td>O</td><td>Error LED control output</td><td>P21</td><td>Low</td><td></td></tr>
<tr><td>CCM_RUNZ</td><td>O</td><td>Run LED control output</td><td>P26</td><td>Low</td><td></td></tr>
<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>I</td><td>Transfer rate and mode setting switch input</td><td>P62-P65</td><td>-</td><td></td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>I</td><td>Station no. setting switch input</td><td>P70-P77</td><td>-</td><td></td></tr>
<tr><td>CCM_LNKRUNZ</td><td>O</td><td>Link run LED control output</td><td>P50</td><td>Low</td><td>Hi-Z (High)</td></tr>
<tr><td>CCM_RDLEDZ</td><td>O</td><td>Receive data LED control output</td><td>P51</td><td>Low</td><td></td></tr>
<tr><td>CCM_SDLEDZ</td><td>O</td><td>Transmit data LED control output</td><td>RP00</td><td>Low</td><td></td></tr>
<tr><td>CCM_IRZ</td><td>O</td><td>Interrupt output</td><td>P35</td><td>Low</td><td></td></tr>
<tr><td>CCM_WDTENZ</td><td>I</td><td>Watchdog timer error input</td><td>P13</td><td>Low</td><td></td></tr>
<tr><td>CCM_MSTZ</td><td>O</td><td>Operation check LED</td><td>P37</td><td>Low</td><td></td></tr>
<tr><td>CCM_SMSTZ</td><td>O</td><td>Standby master LED control output</td><td>RP01</td><td>Low</td><td></td></tr>
<tr><td>CCM_RD</td><td>I</td><td>Communications circuit data reception pin</td><td>P53</td><td>-</td><td></td></tr>
<tr><td>CCM_SD</td><td>O</td><td>Communications circuit data transmission pin</td><td>P54</td><td>-</td><td></td></tr>
<tr><td>CCM_SDGCZ</td><td>O</td><td>Communications circuit transmit data & gate control pin</td><td>P42</td><td>Low</td><td></td></tr>
<tr><td>CCM_CLK80M</td><td>I</td><td>CC-Link clock input (80 MHz)</td><td>-</td><td>-</td><td>-</td></tr>
</table></td><td>21</td><td>[2.1.14 CC-Link Pins (Intelligent Device Station)]
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th><th>Level during & after Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>O</td><td>Link error LED control output</td><td>P20</td><td>Low</td><td>Hi-Z</td></tr>
<tr><td>CCM_ERRZ</td><td>O</td><td>Not used</td><td>P21</td><td>Low</td><td></td></tr>
<tr><td>CCM_RUNZ</td><td>O</td><td>Run LED control output</td><td>P26</td><td>Low</td><td></td></tr>
<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>I</td><td>Transfer rate setting input</td><td>P62-P65</td><td>-</td><td></td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>I</td><td>Station no. setting switch input</td><td>P70-P77</td><td>-</td><td></td></tr>
<tr><td>CCM_LNKRUNZ</td><td>O</td><td>Link run LED control output</td><td>P50</td><td>Low</td><td>Hi-Z (High)</td></tr>
<tr><td>CCM_RDLEDZ</td><td>O</td><td>Receive data LED control output</td><td>P51</td><td>Low</td><td></td></tr>
<tr><td>CCM_SDLEDZ</td><td>O</td><td>Transmit data LED control output</td><td>RP00</td><td>Low</td><td></td></tr>
<tr><td>CCM_IRLZ</td><td>O</td><td>Interrupt signal output from communications circuit</td><td>P35</td><td>Low</td><td></td></tr>
<tr><td>CCM_WDTENZ</td><td>I</td><td>Watchdog timer error input</td><td>P13</td><td>Low</td><td></td></tr>
<tr><td>CCM_MSTZ</td><td>O</td><td>Not used</td><td>P37</td><td>Low</td><td></td></tr>
<tr><td>CCM_SMSTZ</td><td>O</td><td>Not used</td><td>RP01</td><td>Low</td><td></td></tr>
<tr><td>CCM_RD</td><td>I</td><td>Communications circuit data reception pin</td><td>P53</td><td>-</td><td></td></tr>
<tr><td>CCM_SD</td><td>O</td><td>Communications circuit data transmission pin</td><td>P54</td><td>-</td><td></td></tr>
<tr><td>CCM_SDGCZ</td><td>O</td><td>Communications circuit transmit data & gate control pin</td><td>P42</td><td>Low</td><td></td></tr>
<tr><td>CCM_CLK80M</td><td>I</td><td>CC-Link clock input (80 MHz)</td><td>-</td><td>-</td><td>-</td></tr>
</table></td></tr>
</table>

No.3-3 3 Memory Maps

Note regarding the instruction RAM mirror area was

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>40</td><td>[Figure 3.1 Memory Map (All)]

N/A</td><td>41</td><td>[Figure 3.1 Memory Map (All)]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.</td></tr>
<tr><td>43</td><td>[Figure 3.5 External MCU Interface Space]

N/A</td><td>44</td><td>[Figure 3.5 External MCU Interface Space]

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr>
</table>
</td></tr>
</table>

No.3-4 8.2 Port Configuration

"Application and Operation" for the port function control registers and the port function control expansion registers was modified.

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>182</td><td>[8.2 Port Configuration]

<table>
<tr><th rowspan="2">Register Name</th><th colspan="2">Application and Operation</th></tr>
<tr><th>Read</th><th>Write</th></tr>
<tr><td>Port function control registers (PFCn, RPFCm)</td><td>If more than two pin functions are multiplexed on port pins, the corresponding register is used to read which functions are selected.</td><td>If more than two pin functions are multiplexed on port pins, the corresponding register is used to select which functions are to be used.</td></tr>
<tr><td>Port function control expansion registers (PFCEn, RPFCEm)</td><td>If more than three pin functions are multiplexed on port pins, the corresponding register is used to read which functions are selected.</td><td>If more than three pin functions are multiplexed on port pins, the corresponding register is used to select which functions are to be used in combination with the PFCn register.</td></tr>
</table></td><td>183</td><td>[8.2 Port Configuration]

<table>
<tr><th rowspan="2">Register Name</th><th colspan="2">Application and Operation</th></tr>
<tr><th>Read</th><th>Write</th></tr>
<tr><td>Port function control registers (PFCn, RPFCm)</td><td rowspan="2">Used to read which function is selected for the multiplexed pin.</td><td rowspan="2">Used to select the function of the multiplexed pin.</td></tr>
<tr><td>Port function control expansion registers (PFCEn, RPFCEm)</td></tr>
</table></td></tr>
</table>

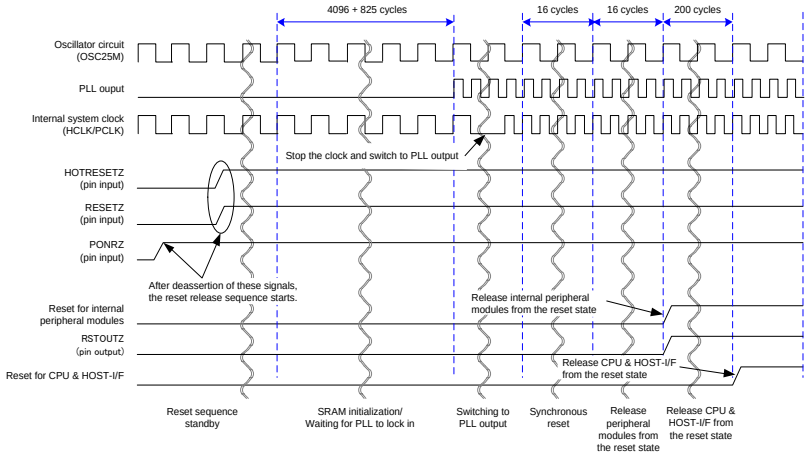
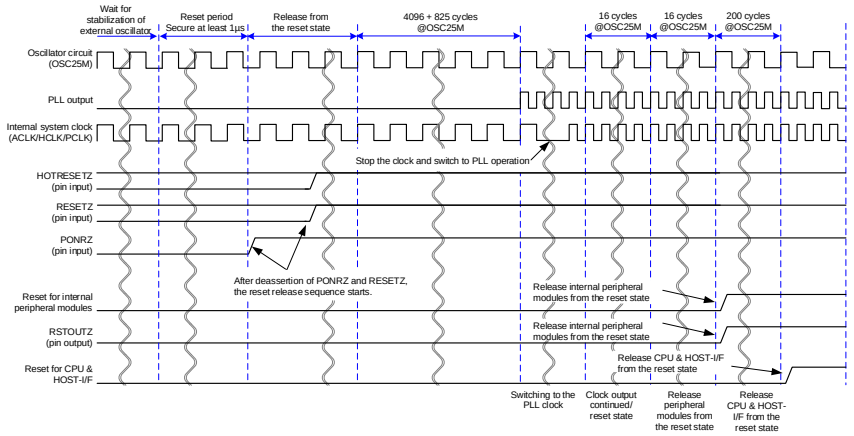
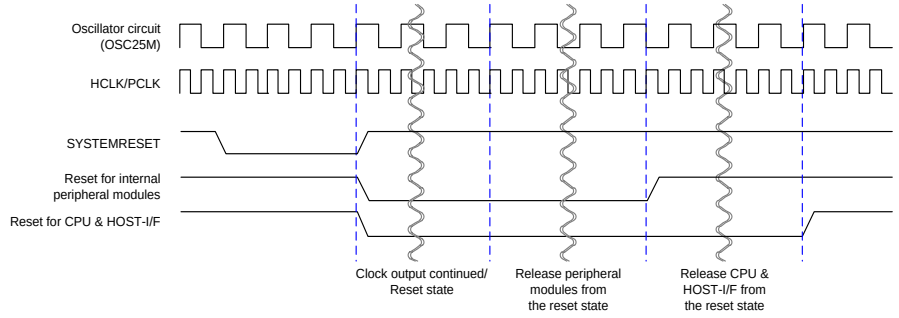
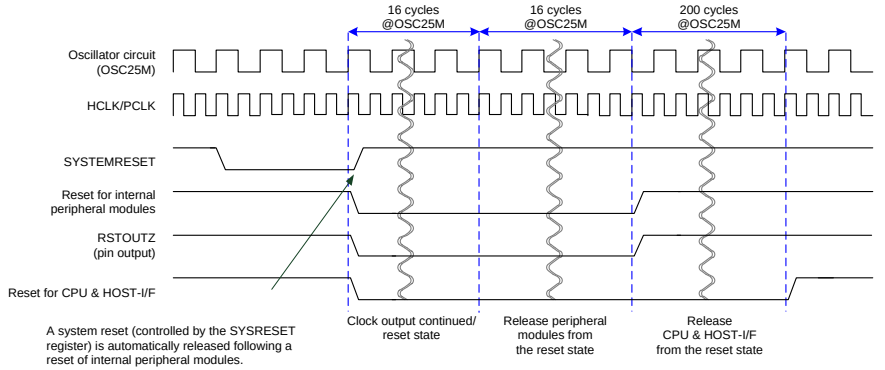
No.3-5 8.2 Port Configuration

Caution on the port configuration was modified.

<table>
<tr><th colspan="2">V4.01</th><th colspan="2">V5.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>182</td><td>[8.2 Port Configuration]
Caution: If a port pin having multiple multiplexed functions which include an external interrupt input is set to control mode by using the PMCn and RPMCm registers, and the multiplexed function is an input, the external interrupt input is also multiplexed.</td><td>183</td><td>[8.2 Port Configuration]
Caution: Operation is not guaranteed if an unsupported function is allocated to the multiplexed pin. For example, if multiplexed function 4 is allocated to the P00 pin, which does not support multiplexed function 4, operation does not proceed correctly. For the allocation of multiplexed pins, see section 8.4, List of Selectable Multiplexed Functions.</td></tr>
</table>

No.4-1 2.4 Operations for Reset

Timing charts for reset at power-on and system reset were modified.

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>2-9</td><td>[Figure 2.2 Timing of Reset at Power On]
 
</td><td>2-9</td><td>[Figure 2.2 Timing of Reset at Power On]
 
</td></tr>
<tr><td></td><td>[Figure 2.3 Timing of Reset at System Reset]
 
</td><td></td><td>[Figure 2.3 Timing of Reset at System Reset]
 
</td></tr>
</table>

No.4-2 5.1 Selecting the Boot Mode

Signal name "STCSZ0" was modified to "CSZ0".

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>5-1</td><td>[Table 5.1 Selecting the Boot Mode]
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Boot Area</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>Memory connected to the STCSZ0 pin of the external bus interface</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Serial flash ROM</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot (debugger used ONLY)</td><td>Instruction RAM</td></tr>
</table>
[(1) External memory boot mode]
The CPU is booted from the external memory connected to the STCSZ0 pin of the external bus interface.</td><td>5-1</td><td>[Table 5.1 Selecting the Boot Mode]
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Boot Area</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>Memory connected to the CSZ0 pin of the external bus interface</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Serial flash ROM</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot (debugger used ONLY)</td><td>Instruction RAM</td></tr>
</table>
[(1) External memory boot mode]
The CPU is booted from the external memory connected to the CSZ0 pin of the external bus interface.</td></tr>
</table>

No.4-3 7.3.4.1 MIIM Register (GMAC_MIIM)

Caution was modified.

V10.00		V11.00	
Page	Description	Page	Revised Description
7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** **Caution: The setting of this register is effective for the management interface selected by the MAC select register (MACSEL). In other cases, writing to this register has no effect and the value read is undefined.**	7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** **Caution: The setting of this register is only effective when the general-purpose Ethernet port is selected by the MAC select register (MACSEL). In other cases, writing to this register has no effect and the value read is undefined.**

No.4-4 7.3.4.5 RX MODE Register (GMAC_RXMODE) Description of the SFRXFIFO bit was modified.

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>7-12</td><td>[7.3.4.5 RX MODE Register (GMAC_RXMODE)]
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>29</td><td>SFRXFIFO</td><td>Store & Forward For RX FIFO
1: Store & Forward mode
The reception DMA controller does not start to operate until data up to the end of the frame is written in RX FIFO.
0: Cut through mode</td></tr>
</table></td><td>7-13</td><td>[7.3.4.5 RX MODE Register (GMAC_RXMODE)]
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>29</td><td>SFRXFIFO</td><td>Store & Forward For RX FIFO
1: Store & Forward mode
The reception DMA controller starts to operate after data up to the end of the frame is written to the RX FIFO buffer.
0: Cut-through mode
The reception DMA controller starts to operate after the number of words set in the RRTTH2-0 bits is written to the RX FIFO buffer.</td></tr>
</table></td></tr>
</table>

No.4-5 7.3.4.6 TXMODE Register (GMAC_TXMODE)

Description of the SF bit was modified and Note 2 was added.

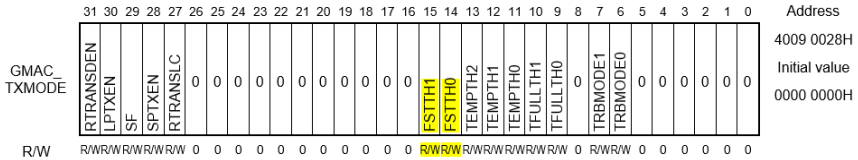
<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td rowspan="2">7-14</td><td>[7.3.4.6 TXMODE Register (GMAC_TXMODE)]
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>29</td><td>SF</td><td>Store & Forward
1: Transmission starts after the end of a frame is written to the TX FIFO buffer. If you are using a TCP/IP accelerator, this must be selected.
0: Transmission starts after words of data specified in the FSTTH1-0 bits are written to the TX FIFO buffer.</td></tr>
</table></td><td rowspan="2">7-14</td><td>[7.3.4.6 TXMODE Register (GMAC_TXMODE)]
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>29</td><td>SF</td><td>Store & Forward
1: Transmission starts after the end of a frame is written to the TX FIFO buffer.
If you are using a TCP/IP accelerator, this must be selected.
0: Setting prohibited Note 2</td></tr>
</table></td></tr>
<tr><td>Note. LPTXEN must be set to 1 since the frame size may exceed the maximum size of 1518 bytes while management tag insertion of the Ethernet switch is enabled (the SWTAGEN bit in the ETHSWMTC register is 1).</td><td>Notes 1. LPTXEN must be set to 1 since the frame size may exceed the maximum size of 1518 bytes while management tag insertion of the Ethernet switch is enabled (the SWTAGEN bit in the ETHSWMTC register is 1).
2. Setting the SF bit to 0 is prohibited. Always start operation after setting this bit to 1. For details, see section 7.5.1, Transmitting Data in Cut-Through Mode.</td></tr>
</table>

No.4-6 7.3.4.6 TXMODE Register

(GMAC_TXMODE) The FSTTH bits were changed to

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>7-14</td><td>

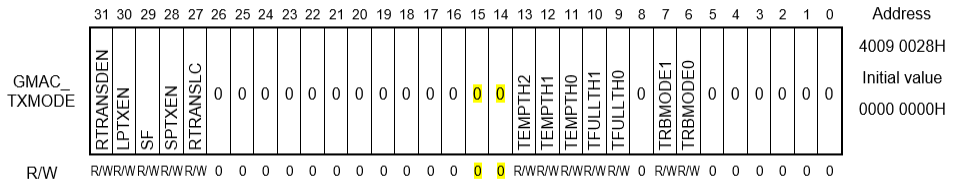
[7.3.4.6 TXMODE Register (GMAC_TXMODE)]



Bit Position	Bit Name	Description
15, 14	FSTTH1-0	Frame Start Threshold Transmission starts when the number of data words written to the TX FIFO buffer exceeds this value. 00: 4 words 01: 8 words 10: 16 words 11: 32 words

</td><td>7-14</td><td>

[7.3.4.6 TXMODE Register (GMAC_TXMODE)]



Bit Position	Bit Name	Description
15, 14	–	Reserved. The write value should be 0. Reading these bits returns 0.

</td></tr>
</table>

No.4-7 7.4.1.2 Flow of Processing for Issuing the Hardware Function Call

Figure 7.4 Flow of Processing for Issuing the Hardware Function, modified

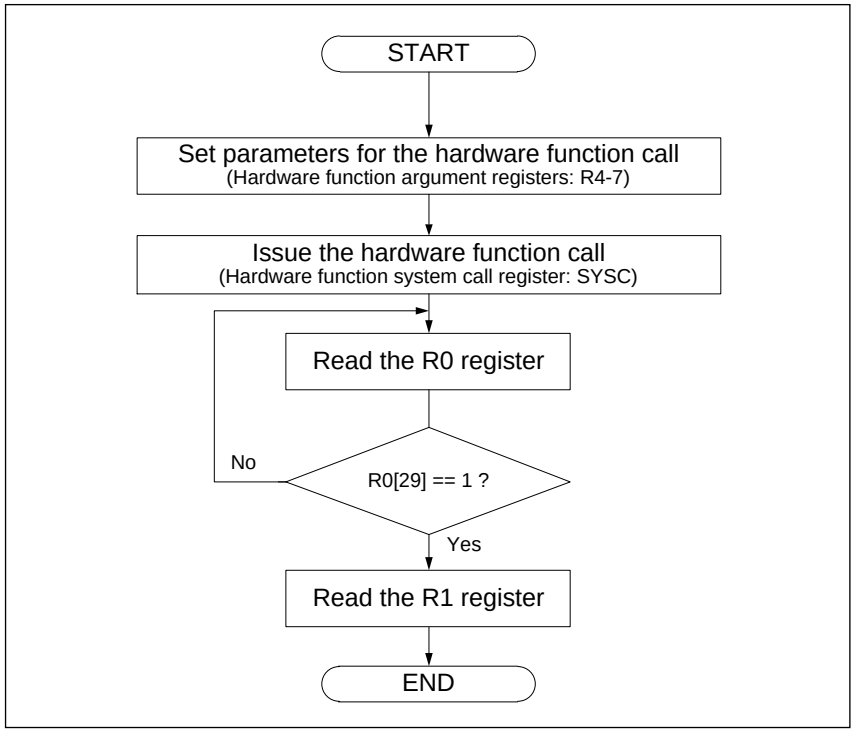
<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>7-32</td><td>[7.4.1.2 Flow of Processing for Issuing the Hardware Function Call]
 

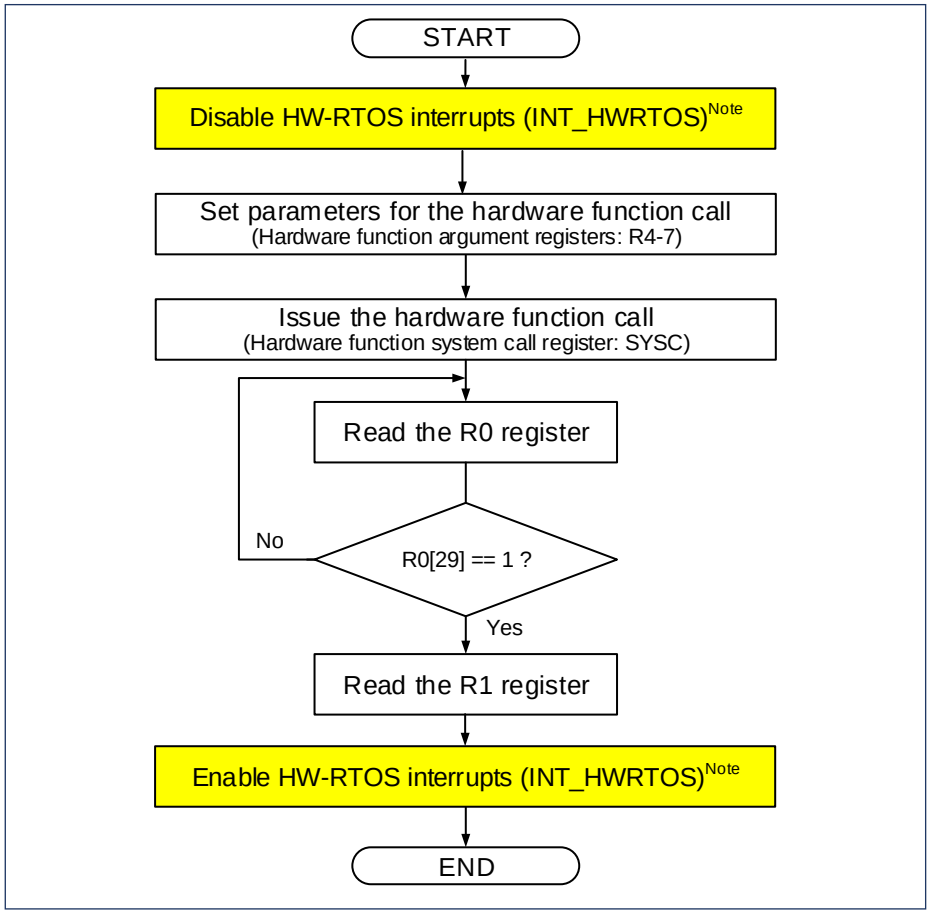
Figure 7.4 Flow of Processing for Issuing the Hardware Function</td><td>7-33</td><td>[7.4.1.2 Flow of Processing for Issuing the Hardware Function Call]
 

Figure 7.4 Flow of Processing for Issuing the Hardware Function

Note: This processing is required only when the hardware real-time OS is used.</td></tr>
</table>

No.4-8 7.4.1.3 Buffer Allocator

The description on an generation of an exception,

V10.00		V11.00	
Page	Description	Page	Revised Description
7-33	**[(1) Functional Overview]** To use the buffer RAM, secure the required area (hereafter “buffer”) beforehand, and then issue the hardware function calls provided for the buffer allocator. Writing to an area which has not been secured by the CPU has no effect, but access to such area by the hardware function DMAC leads to the generation of an exception.	7-34	**[(1) Functional Overview]** To use the buffer RAM, secure the required area (hereafter "buffer") beforehand, and then issue the hardware function calls provided for the buffer allocator. When writing to an area which has not been secured, access by the CPU or MAC DMA controller generates an interrupt, whereas access to such area by the buffer RAM DMA controller generates an interrupt or returns an exception to the return value register R0 depending on the type of hardware function calls.

No.4-9 7.4.1.3 Buffer Allocator

Table 7.2 HWFNC_LongBuffer_Get: Return value registers, modified

V10.00		V11.00	
Page	Description	Page	Revised Description
7-36	**[Table 7.2 HWFNC_LongBuffer_Get]** R1[31:0] First logical address of the buffer [31:27] 5’b00001 [26] 1 [25:18] LLID [17: 0] 0	7-37	**[Table 7.2 HWFNC_LongBuffer_Get]** R1[31:0] First logical address of the buffer [31:27] 5’b00001 [26:24] 3'b100 [23:18] LLID [17: 0] 0

No.4-10 7.4.1.3 Buffer Allocator

Table 7.3 HWFNC_ShortBuffer_Get: Return value registers, modified

V10.00		V11.00	
Page	Description	Page	Revised Description
7-37	**[Table 7.3 HWFNC_ShortBuffer_Get]** R1[31:0] First logical address of the buffer [31:27] 5’b00001 [26] 0 [25:18] SBID [18: 0] 0	7-38	**[Table 7.3 HWFNC_ShortBuffer_Get]** R1[31:0] First logical address of the buffer [31:27] 5’b00001 [26:25] 2'b00 [24:18] SBID [17: 0] 0

No.4-11 7.4.1.4 MAC DMA Controller, (2) DMA for the Reception MAC

Example modified

V10.00		V11.00	
Page	Description	Page	Revised Description
7-44	**[(b) Usage・Procedure for reading and releasing buffers]** [Example of reading and releasing a buffer] (1) Read the BUFID register (2) Shift the bits [27:16] read from BUFID 16 bits to the right to obtain the number of received words. (3) The bits [15:0] read from the BUFID are bits [26:11] of the address where the acquired buffer starts. The individual bits of the address where the acquired buffer starts are configured as follows. [31:27]: 00001b [26:19]: Equivalent to the bits [15:8] in the BUFID ([26] of the start address is always 1; [25:19] are LLID[6:0]) [18:11]: Equivalent to the bits [7:0] in the BUFID (always 0) [10: 0]: Always 0 (4) After using the buffer, specify the start address as an argument and issue the buffer release function call to release the buffer.	7-45	**[(b) Usage・Procedure for reading and releasing buffers]** [Example of reading and releasing a buffer] (1) Read the BUFID register (2) Shift the bits [27:16] read from BUFID 16 bits to the right to obtain the number of received words. (3) The bits [15:0] read from the BUFID are bits [26:11] of the address where the acquired buffer starts. The individual bits of the address where the acquired buffer starts are configured as follows. [31:27]: 00001b [26:18]: Equivalent to the bits [15:7] in the BUFID [17:11]: Equivalent to the bits [6:0] in the BUFID [10: 0]: Always 0 (4) After using the buffer, specify the start address as an argument and issue the buffer release function call to release the buffer.

No.4-12 7.4.1.4 MAC DMA Controller, (2) DMA for the Reception MAC

The description modified

V10.00		V11.00	
Page	Description	Page	Revised Description
7-45	**[(c) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0. Access to an access-prohibited area (an area other than the buffer RAM, etc.) while the hardware function call is running leads to the return of an exception code in the return value register R0.	7-46	**[(c) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0. If an error occurs while the hardware function call is running, an interrupt is generated.

No.4-13 7.4.1.4 MAC DMA Controller, (3) DMA for the Transmission MAC

The description modified

V10.00		V11.00	
Page	Description	Page	Revised Description
7-50	**[(d) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0.	7-51	**[(d) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0. If an error occurs while the hardware function call is running, an interrupt is generated.

No.4-14 7.4.1.4 MAC DMA Controller, (3) DMA for the Transmission MAC

The description modified

V10.00		V11.00	
Page	Description	Page	Revised Description
7-50	**[(d) List of hardware function calls, Table 7.11 HWFNC_MACDMA_TX_Errstat]** R0[1:0] / Result / [0]: Memory Access Violation [1]: Memory Access Timeout	7-52	**[(d) List of hardware function calls, Table 7.11 HWFNC_MACDMA_TX_Errstat]** R0[1:0] / Result / [0]: Memory Access Violation • Access to the buffer that is not acquired • The number of transfer bytes is not correct • The start address of the descriptor is not on a 64-bit boundary. [1]: Memory Access Timeout • The start address of a transmission descriptor turns to be an end value (FFFF FFFFh) • Releasing the buffer automatically is failed

No.4-15 7.4.1.5 Buffer RAM DMA Controller, (2) DMA Transfer The description modified

V10.00		V11.00	
Page	Description	Page	Revised Description
7-52	**[(d) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0. Access to an access-prohibited area (an area other than the buffer RAM, etc.) while the hardware function call is running leads to the return of an exception code in the return value register R0.	7-54	**[(d) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0. Access to an access-prohibited area (an area other than the buffer RAM, etc.) while the hardware function call is running leads HWFNC_Direct_Memory_Transfer and HWFNC_Direct_Memory_Replace to return an exception to the return value register R0, whereas it leads HWFNC_INTBUFF_DMA_Start and HWFNC_INTBUFF_DMA_Start (Descriptor) to generate an interrupt.

No.4-16 7.4.1.5 Buffer RAM DMA Controller, (2) DMA Transfer

The description on argument registers, modified

V10.00		V11.00	
Page	Description	Page	Revised Description
7-52	**[(d) List of hardware function calls]** Argument registers R4[31:0] — Address where the destination area for transfer starts — Specifies the address where the destination area for transfer starts. R5[31:0] — Address where the source area for transfer starts — Specifies the address where the source address for transfer starts.	7-52	**[(d) List of hardware function calls, Table 7.12 HWFNC_Direct_Memory_Transfer]** Argument registers R4[31:0] — Address where the source area for transfer starts — Specifies the address where the source area for transfer starts. R5[31:0] — Address where the destination area for transfer starts — Specifies the address where the destination area for transfer starts.

No.4-17 7.4.2 Interrupts

The condition to generate an MACDMA transmission error interrupt, that is related to operations for transmission, modified

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>7-56</td><td>[Table 7.16 Interrupts Related to Operations for Transmission]
<table><tr><th>Interrupt Name</th><th>Symbol</th><th>Conditions for Asserting and De-asserting Interrupts</th></tr><tr><td>MACDMA transmission error interrupt</td><td>INTETHTXDERR</td><td>This interrupt is generated when the address field of a descriptor is outside the range of the buffer, the number of bytes for transfer is invalid, or a descriptor is not set to start on a 64-bit boundary.
Modify the settings of the transmission descriptor for retransmission.
Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.</td></tr></table></td><td>7-58</td><td>[Table 7.16 Interrupts Related to Operations for Transmission]
<table><tr><th>Interrupt Name</th><th>Symbol</th><th>Conditions for Asserting and De-asserting Interrupts</th></tr><tr><td>MACDMA transmission error interrupt</td><td>INTETHTXDERR</td><td>This interrupt is generated, when an error occurs while the transmission MAC DMA is operating. As there are several error sources, HWFNC_MACDMA_TX_Errstat is used to obtain the error source.
Modify the settings of the transmission descriptor for retransmission.
Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.</td></tr></table></td></tr>
</table>

No.4-18 7.4.2 Interrupts

The buffer RAM area access error was added to interrupts related to other operations

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>7-58</td><td>[Table 7.18 Interrupts Related to Other Operations]
<table><tr><th>Interrupt Name</th><th>Symbol</th><th>Conditions for Asserting and De-asserting Interrupts</th></tr><tr><td colspan="3">N/A</td></tr></table></td><td>7-60</td><td>[Table 7.18 Interrupts Related to Other Operations]
<table><tr><th>Interrupt Name</th><th>Symbol</th><th>Conditions for Asserting and De-asserting Interrupts</th></tr><tr><td>Buffer RAM area access error</td><td>INTBRAMERR</td><td>This interrupt is generated, if the buffer that is not acquired by the CPU is accessed. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.</td></tr></table></td></tr>
</table>

No.4-19 7.5 Notes

Notes regarding transmission in cut-through mode and transmission and reception of jumbo frames were added.

V10.00		V11.00	
Page	Description	Page	Revised Description
-	**[7.5.5 Transmitting Data in Cut-Through Mode]** N/A	7-87	**[7.5.5 Transmitting Data in Cut-Through Mode]** Setting the SF bit (b29) of the TX Mode register (GMAC_TXMODE) to 0 may lead to generation of an unexpected TX FIFO underflow interrupt. To avoid this, always set this bit to 1 (Store & Forward mode).
	[7.5.6 Jumbo Frames] N/A		**[7.5.6 Jumbo Frames]** This product does not support transmission and reception of frames exceeding 1,518 bytes, i.e. jumbo frames.

No.4-20 9.7 Memory Access Timing Examples

"STCSZn" was modified to "CSZn".

V10.00		V11.00	
Page	Description	Page	Revised Description
9-17 to 9-24	**[9.7 Memory Access Timing Examples]** The concerned signal name is "STCSZn" in the charts below. Figure 9.8 SRAM Read Cycles Figure 9.9 SRAM Read Cycles (with Wait Settings) Figure 9.10 SRAM Read Cycles (External Wait Insertion) Figure 9.11 SRAM Write Cycles (with No Wait) Figure 9.12 SRAM Write Cycles (with Wait States) Figure 9.13 SRAM Write Cycles (External Wait Insertion) Figure 9.14 PageROM Read Cycles (Single Transfer) Figure 9.15 PageROM Read Cycles (Four Burst Transfer)	9-17 to 9-24	**[9.7 Memory Access Timing Examples]** The concerned signal name is aligned to "CSZn" in the charts below. Figure 9.8 SRAM Read Cycles Figure 9.9 SRAM Read Cycles (with Wait Settings) Figure 9.10 SRAM Read Cycles (External Wait Insertion) Figure 9.11 SRAM Write Cycles (with No Wait) Figure 9.12 SRAM Write Cycles (with Wait States) Figure 9.13 SRAM Write Cycles (External Wait Insertion) Figure 9.14 Page ROM Read Cycles (Single Transfer) Figure 9.15 Page ROM Read Cycles (Four Burst Transfer)

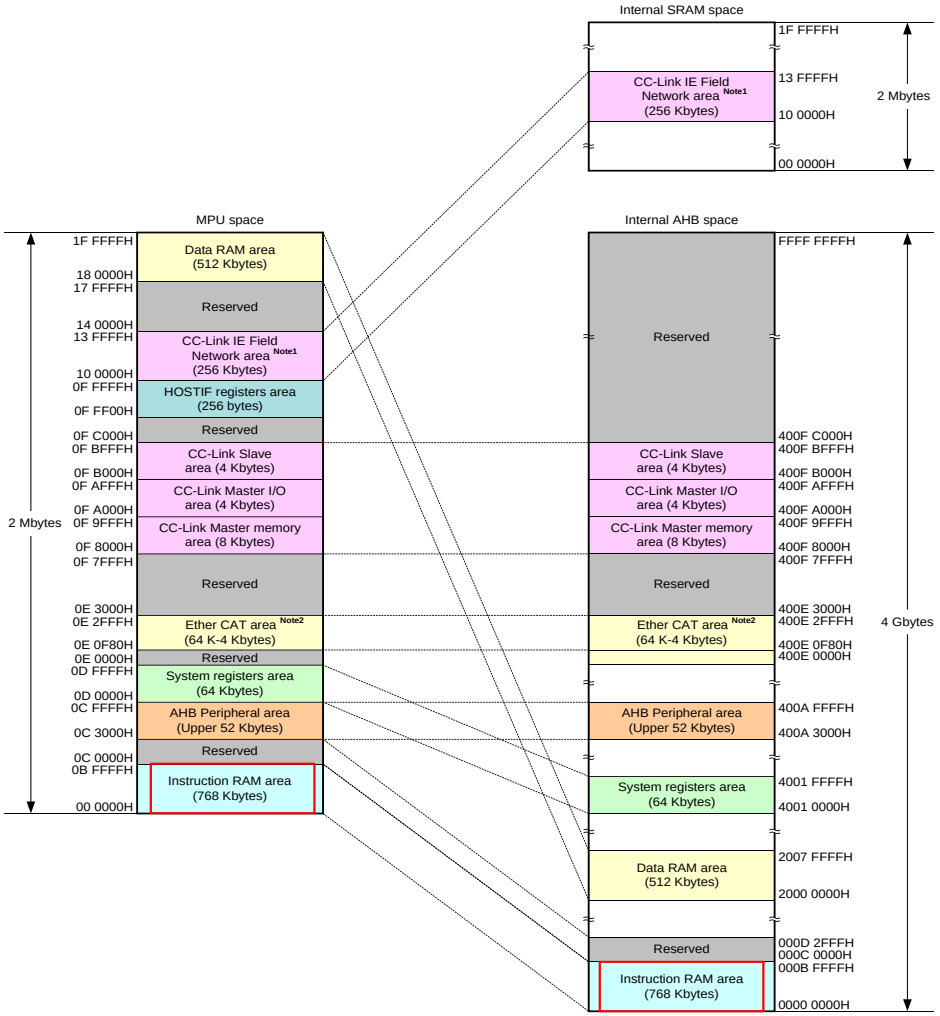
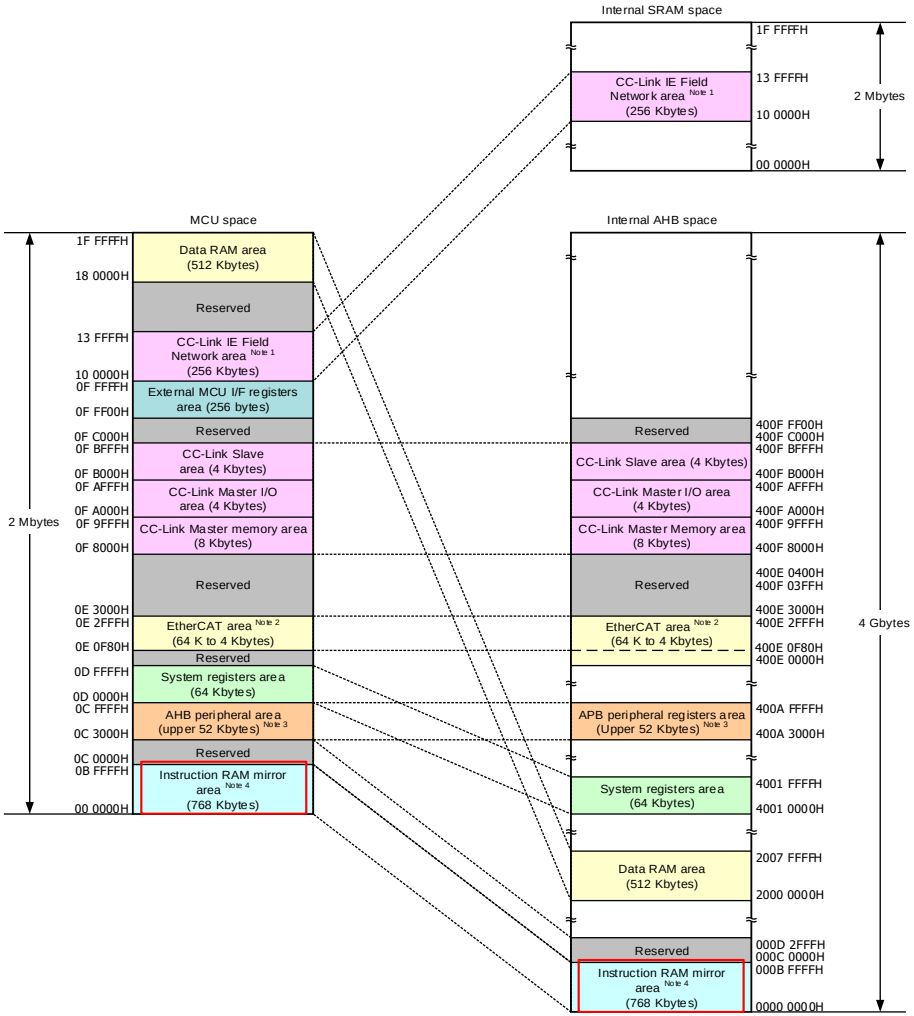
No.4-21 9.7 Memory Access Timing Examples

The number of address setup waits in the SRAM write cycles was corrected.

V10.00		V11.00	
Page	Description	Page	Revised Description
9-20	**[Figure 9.11 SRAM Write Cycles (with No Wait)]** BSC : SBS3-SBS0 = 1111B (32 bits), SMCn: WWn3-WWn0 = 0000B/0001B (1 wait cycle), DWn3-DWn0 = 0000B (no wait), ACn3-ACn0 = 0000B/0001B (no wait)	9-20	**[Figure 9.11 SRAM Write Cycles (with No Wait)]** BSC : SBS3-SBS0 = 1111B (32 bits), SMCn: WWn3-WWn0 = 0000B/0001B (1 wait cycle), DWn3-DWn0 = 0000B (no wait), ACn3-ACn0 = 0000B/0001B (1 wait cycle)

No.4-22 11.1 Memory Maps

The instruction RAM area was modified to the instruction RAM mirror area.

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>11-3</td><td>[Figure 11.1 External MCU Interface Space]
 
</td><td>11-3</td><td>[Figure 11.1 External MCU Interface Space]
 
</td></tr>
</table>

No.4-23 11.1 Memory Map

Note regarding the instruction RAM mirror area was

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>11-3</td><td>[11.1 Memory MAP]
Notes 1. This is only provided in the R-IN32M3-CL.
2. This is only provided in the R-IN32M3-EC.
3. The upper 52 Kbytes of the AHB peripheral registers area covers the range from the GPIO area to the synchronous burst memory controller control registers.
For details, see the memory map of the R-IN32M3 Series User's Manual.</td><td>11-4</td><td>[11.1 Memory Map]
Notes 1. This is only provided in the R-IN32M3-CL.
2. This is only provided in the R-IN32M3-EC.
3. The upper 52 Kbytes of the AHB peripheral registers area covers the range from the GPIO area to the synchronous burst memory controller control registers.
For details, see the memory map of the R-IN32M3 Series User's Manual.
4. The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture.
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr>
</table>
</td></tr>
</table>

No.4-24 11.2.5 Control Registers, (2) HOSTIF Bus Control Register (HIFBCC)

The instruction RAM area was modified to the instruction RAM mirror area.

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>11-17</td><td>[(2) HOSTIF Bus Control Register (HIFBCC)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>1</td><td>RBUFON1</td><td>Enables or disables advance reading of the instruction RAM area.
0: Advance reading is disabled.
1: Advance reading is enabled.</td></tr>
</table></td><td>11-17</td><td>[(2) HOSTIF Bus Control Register (HIFBCC)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>1</td><td>RBUFON1</td><td>Enables or disables advance reading of the instruction RAM mirror area.
0: Advance reading is disabled.
1: Advance reading is enabled.</td></tr>
</table></td></tr>
<tr><td>11-18</td><td>[Table 11.7 Address Range for which Advance Reading and Page ROM Reading are Selectable]

<table>
<tr><th rowspan="2">Target Macro</th><th colspan="2">Address Range</th><th colspan="2">Related Enable Bits</th></tr>
<tr><th>MPU Space</th><th>Internal AHB Space</th><th>Advance Reading</th><th>Page ROM</th></tr>
<tr><td>Instruction RAM</td><td>0B FFFFH
to
00 0000H</td><td>000B FFFFH
to
0000 0000H</td><td>HIFBCC.
RBUFON1</td><td>HIFPRC.
PAGEON1</td></tr>
</table>.</td><td>11-18</td><td>[Table 11.7 Address Range for which Advance Reading and Page ROM Reading are Selectable]

<table>
<tr><th rowspan="2">Target Macro</th><th colspan="2">Address Range</th><th colspan="2">Related Enable Bits</th></tr>
<tr><th>MPU Space</th><th>Internal AHB Space</th><th>Advance Reading</th><th>Page ROM</th></tr>
<tr><td>Instruction RAM mirror area</td><td>0B FFFFH
to
00 0000H</td><td>000B FFFFH
to
0000 0000H</td><td>HIFBCC.
RBUFON1</td><td>HIFPRC.
PAGEON1</td></tr>
</table>.</td></tr>
</table>

No.4-25 11.2.5 Control Registers (2) HOSTIF Bus Control Register (HIFBCC)

Caution regarding access to the instruction RAM mirror area while advance reading is enabled, added

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>11-18</td><td>[(2) HOSTIF Bus Control Register (HIFBCC)]

Caution: Some areas cannot be read in advance depending on the target macro even if advance reading is enabled.</td><td>11-18</td><td>[(2) HOSTIF Bus Control Register (HIFBCC)]

Cautions 1. Some areas cannot be read in advance depending on the target macro even if advance reading is enabled.
2. If the last 16-byte area of the instruction RAM mirror area is read while advance reading is enabled, this will lead to assertion of the HERROUTZ pin.</td></tr>
</table>

No.4-26 11.2.5 Control Registers, (4) HOSTIF page ROM control register (HIFPRC)

The instruction RAM area was modified to the instruction RAM mirror area.

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>11-20</td><td>[(4) HOSTIF page ROM control register (HIFPRC)]

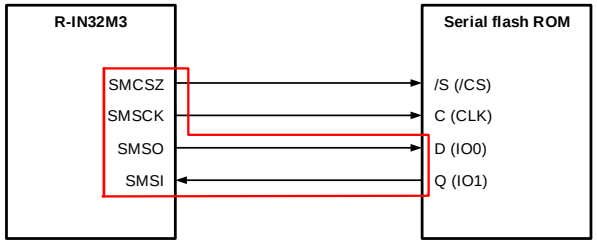
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>1</td><td>PAGEON1</td><td>Page ROM reading of the instruction RAM area is set up.
0: SRAM reading
1: Page ROM reading</td></tr>
</table>
.</td><td>11-20</td><td>[(4) HOSTIF page ROM control register (HIFPRC)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>1</td><td>PAGEON1</td><td>Page ROM reading of the instruction RAM mirror area is set up.
0: SRAM reading
1: Page ROM reading</td></tr>
</table>
.</td></tr>
</table>

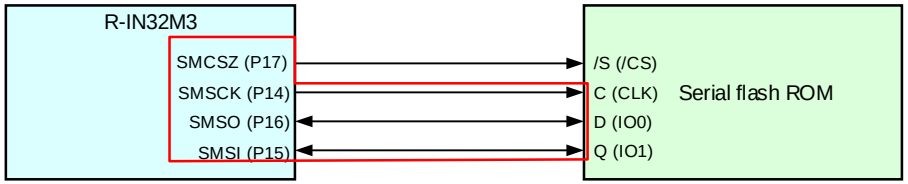
No.4-27 12.3 Connection with Serial Flash ROM

The names of R-IN pins in Figure 12.1 were modified

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>12-12</td><td>[Figure 12.1 Connection with Serial Flash ROM]



.</td><td>12-12</td><td>[Figure 12.1 Connection with Serial Flash ROM]



.</td></tr>
</table>

No.4-28 13.1.1 Overview

Description of Skipping was modified.

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>13-2</td><td>[13.1.1 Overview]
• Skipping
A continuous access size and separation access size can be set respectively for the area for access in DMA transfer.
After access to a set size for continuous access, the set separation access size can be skipped before access to the next address.</td><td>13-2</td><td>[13.1.1 Overview]
• Skipping
A continuous access size and skip space size can be set respectively for the areas for access in DMA transfer. After access to a set size for continuous access, the set skip space size can be skipped before access to the next address.</td></tr>
</table>

No.4-29 13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)

Note regarding external DMA transfer request inputs that are selected as DMA transfer trigger sources was added.

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>13-85</td><td>[13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)]

<table>
<tr><th>IFCn6-IFCn0</th><th>Selection of a DMA Transfer Trigger Source</th></tr>
<tr><td>01H</td><td>DMAREQZ0 pin (DMA transfer request) input (Only the setting of the DTFR0 register is effective.)</td></tr>
<tr><td>02H</td><td>02H DMAREQZ1 pin (DMA transfer request) input (Only the setting of the DTFR1 register is effective.)</td></tr>
<tr><td>03H</td><td>03H RTDMAREQZ0 pin (DMA transfer request) input (Only the setting of the RTDTFR register is effective.)</td></tr>
</table>
[13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)]

N/A</td><td>13-85</td><td>[13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)]

<table>
<tr><th>IFCn6-IFCn0</th><th>Selection of a DMA Transfer Trigger Source</th></tr>
<tr><td>01H</td><td>DMAREQZ0 pin (DMA transfer request) input Note</td></tr>
<tr><td>02H</td><td>DMAREQZ1 pin (DMA transfer request) input Note</td></tr>
<tr><td>03H</td><td>RTDMAREQZ0 pin (DMA transfer request) input Note</td></tr>
</table>
[13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)]

Note: External DMA transfer request inputs (inputs on the DMAREQZ0, DMAREQZ1, and RTDMAREQZ pins) can be individually set as DMA transfer trigger requests with the corresponding registers listed below.
DMAREQZ0 pin: DTFR0 register
DMAREQZ1 pin: DTFR1 register
RTDMAREQZ pin: RTDTFR register</td></tr>
</table>

No.4-30 13.6 Interrupt Output

The column "Switch between Pulse Output and Interrupt Output", deleted.

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>13-89</td><td>

[Table 13.9 General DMA Controller Interrupt Output]

<table>
<tr><th>Interrupt Signal</th><th>Interrupt Source</th><th>Interrupt Detection Mask</th><th>Switch between Pulse Output and Interrupt Output</th><th>Interrupt Output Mask</th></tr>
<tr><td rowspan="2">INTDMAn</td><td>The DMA transaction is completed.</td><td>CHCFGn register DEM = 1</td><td rowspan="3">DCTRL register
LVINT = 0: Pulse output
LVINT = 1: Level output</td><td rowspan="2">CHSTATn. INTM = 1</td></tr>
<tr><td>An invalid descriptor is read in link mode.</td><td>DIM in the header = 1</td></tr>
<tr><td>INTDMEERR</td><td>An error response is returned in response to a transfer request issued by the master interface.</td><td>— (Not available)</td><td>— (Not available)</td></tr>
</table>

[Table 13.10 Interrupt Output of DMA Controller for Real-Time Ports]

<table>
<tr><th>Interrupt Signal</th><th>Interrupt Source</th><th>Interrupt Detection Mask</th><th>Switch between Pulse Output and Interrupt Output</th><th>Interrupt Output Mask</th></tr>
<tr><td rowspan="2">INTRTDMA</td><td>The DMA transaction is completed.</td><td>RTCHCFG register DEM = 1</td><td rowspan="3">RTDCTRL register
LVINT = 0: Pulse output
LVINT = 1: Level output</td><td rowspan="2">RTCHSTAT. INTM = 1</td></tr>
<tr><td>An invalid descriptor is read in link mode.</td><td>DIM in the header = 1</td></tr>
<tr><td>INTRTDMEERR</td><td>An error response is returned in response to a transfer request issued by the master interface.</td><td>— (Not available)</td><td>— (Not available)</td></tr>
</table>

</td><td>13-89</td><td>

[Table 13.9 General DMA Controller Interrupt Output]

<table>
<tr><th>Interrupt Signal</th><th>Interrupt Source</th><th>Interrupt Detection Mask</th><th>Interrupt Output Mask</th></tr>
<tr><td rowspan="2">INTDMAn</td><td>The DMA transaction is completed.</td><td>CHCFGn register DEM = 1</td><td rowspan="2">CHSTATn. INTM = 1</td></tr>
<tr><td>An invalid descriptor is read in link mode.</td><td>DIM in the header = 1</td></tr>
<tr><td>INTDMEERR</td><td>An error response is returned in response to a transfer request issued by the master interface.</td><td>— (Not available)</td><td>— (Not available)</td></tr>
</table>

[Table 13.10 Interrupt Output of DMA Controller for Real-Time Ports]

<table>
<tr><th>Interrupt Signal</th><th>Interrupt Source</th><th>Interrupt Detection Mask</th><th>Interrupt Output Mask</th></tr>
<tr><td rowspan="2">INTRTDMA</td><td>The DMA transaction is completed.</td><td>RTCHCFG register DEM = 1</td><td rowspan="2">RTCHSTAT. INTM = 1</td></tr>
<tr><td>An invalid descriptor is read in link mode.</td><td>DIM in the header = 1</td></tr>
<tr><td>INTRTDMEERR</td><td>An error response is returned in response to a transfer request issued by the master interface.</td><td>— (Not available)</td><td>— (Not available)</td></tr>
</table>

</td></tr>
</table>

No.4-31 17.4.2 Master/Slave Connections [1/2]

Diagram of connections between one master and one slave was modified.

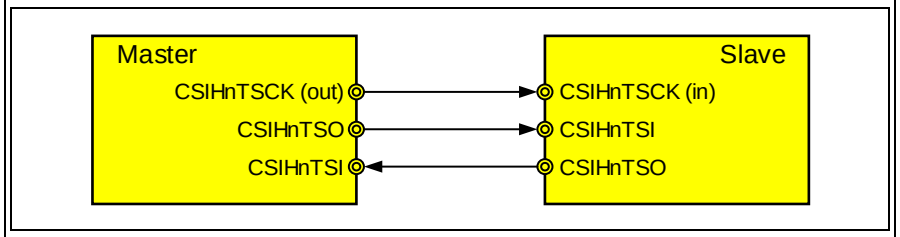
<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>17-38</td><td>[(1) One master and one slave]
 

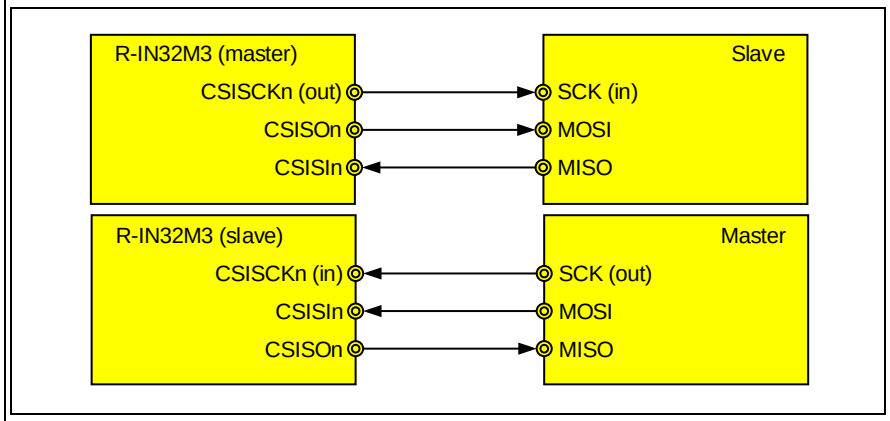
Figure 17.4 Direct Master/Slave Connection</td><td>17-38</td><td>[(1) One master and one slave]
 

Figure 17.4 Direct Master/Slave Connection</td></tr>
</table>

No.4-31 17.4.2 Master/Slave Connection [2/2]

Diagram of connections between one master and two slaves was modified, CSIH pin names were changed, and the CSIHnTSSI pin was deleted.

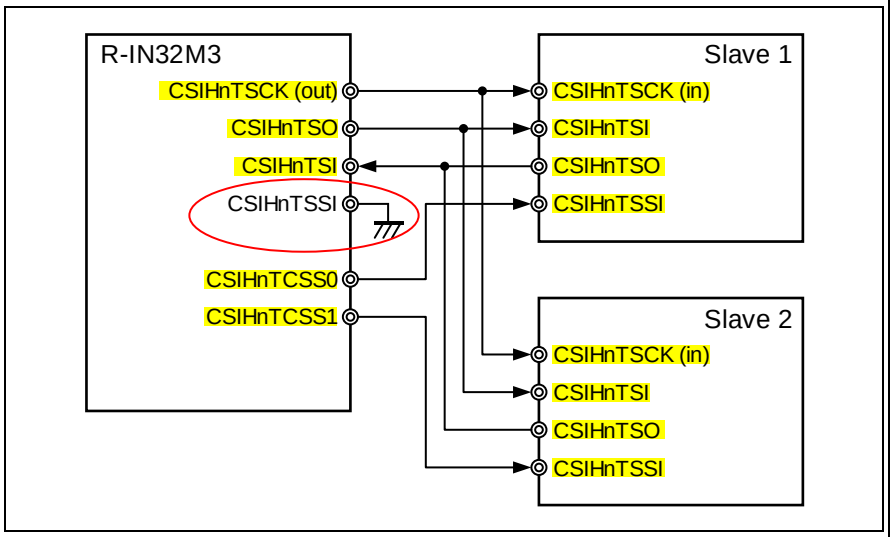
<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>17-38</td><td>[(2) One master and two slaves]
The following figure illustrates the connections between an R-IN32M3 as a master and two slaves.
In this example, an R-IN32M3 can be configured to supply one chip select (CS) signal to each slave.
This signal is connected to the slave select input CSIHnTSSI of the slave.
 

Figure 17.5 Connection between One Master and Two Slaves

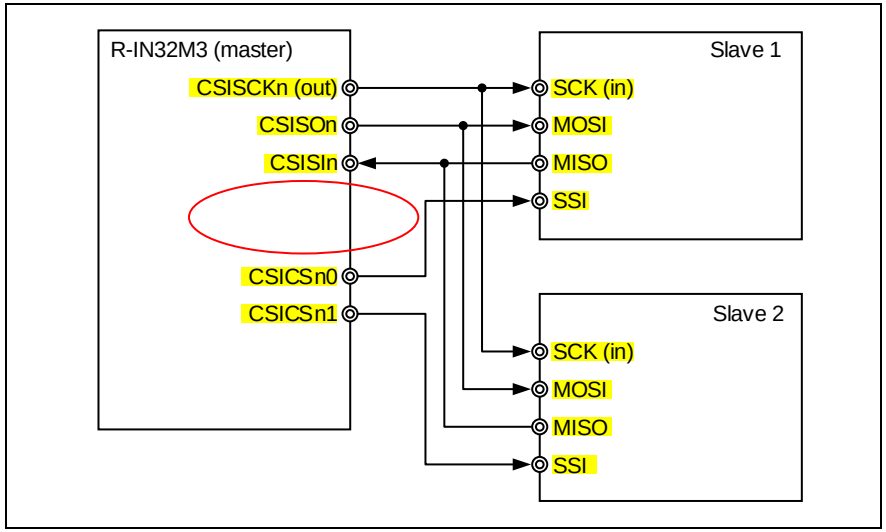
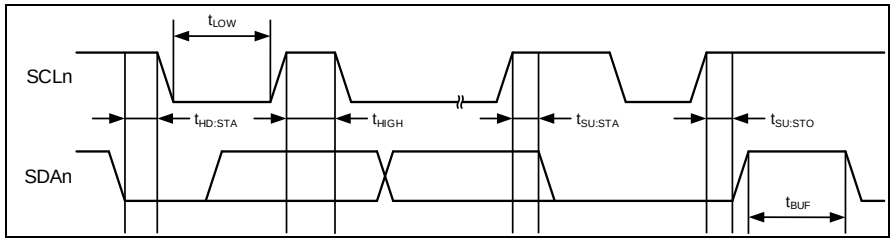
The default chip select level is active low. In other words, when the slave select input signal (CSIHnTSSI) of a slave is at the low level, that slave is selected as a CSIH slave (and enabled). However, to use a chip select signal (CS) for another device, programming that sets the chip select signal output level to active high is possible.
If a slave is not selected, it will neither receive nor transmit data. In addition, its output CSIHnTSO is set to input mode in order to avoid interference with the output of another slave that was selected.</td><td>17-38</td><td>[(2) One master and two slaves]
The following figure illustrates the connections between an R-IN32M3 as a master and two slaves.
In this example, an R-IN32M3 can be configured to supply one chip select (CS) signal to each slave.
This signal is connected to the slave select input SSI of the slave.
 

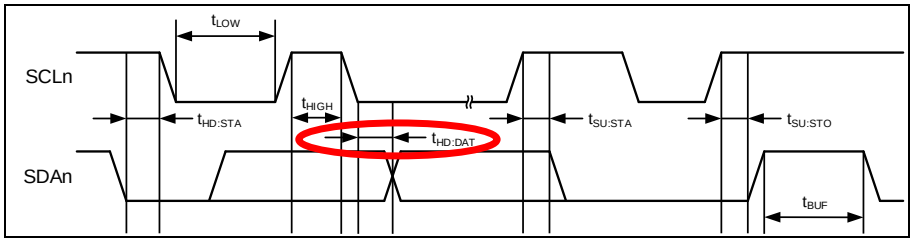
Figure 17.5 Connection between One Master and Two Slaves

The default chip select level is active low. In other words, when the slave select input signal (SSI) of a slave is at the low level, that slave is selected as a CSIH slave (and enabled). However, to use a chip select signal (CS) for another device, programming that sets the chip select signal output level to active high is possible.
If a slave is not selected, it will neither receive nor transmit data. In addition, its output MISO is set to input mode in order to avoid interference with the output of another slave that was selected.</td></tr>
<tr><td>17-39</td><td>[(3) CSIHnTSO output control]
The CSIH can output CSIHnTSO when all of the following conditions are satisfied:
• The CSIH is enabled (CSIHnCTL0.CSIHnPWR = 1).
• The CSIH is operated in transmit-only or transmit/receive mode (CSIHnCTL0.CSIHnTXE = 1).
By using this function, signal congestions on the external CSIHnTSO signal line can be avoided.</td><td>17-39</td><td>[(3) CSISOn output control]
The CSIH can output CSISOn when all of the following conditions are satisfied:
• The CSIH is enabled (CSIHnCTL0.CSIHnPWR = 1).
• The CSIH is operated in transmit-only or transmit/receive mode (CSIHnCTL0.CSIHnTXE = 1).
By using this function, signal congestions on the external CSISOn signal line can be avoided.</td></tr>
</table>

No.4-32 18.3 Registers (6) IICBn high-level width setting register (IICBnWH)

Generation timing of $t_{SU:STA}$ was modified and $t_{HD:DAT}$ was added in the timing chart.

<table>
<tr><th colspan="2">V10.00</th><th colspan="2">V11.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>18-13</td><td>
Table 18.4 Conditions for Generating Serial Output Timing
<table>
<tr><th>Symbol</th><th>Description</th><th>Standard Mode</th><th>Fast Mode</th></tr>
<tr><td>$t_{HD:STA}$</td><td>Start condition hold time</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>t_{LOW}</td><td>SCL low-level width period</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>t_{HIGH}</td><td>SCL high-level width period</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>$t_{SU:STA}$</td><td>Start condition setup time</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>$t_{SU:STO}$</td><td>Stop condition setup time</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>t_{BUF}</td><td>Bus free time
(interval between stop condition and start condition)</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>$t_{HD:DAT}$</td><td>Data hold time</td><td>IICB0WL[9:2] / PCLK</td><td>IICB0WL[9:2] / PCLK</td></tr>
</table>


</td><td>18-13</td><td>
Table 18.4 Conditions for Generating Serial Output Timing
<table>
<tr><th>Symbol</th><th>Description</th><th>Standard Mode</th><th>Fast Mode</th></tr>
<tr><td>$t_{HD:STA}$</td><td>Start condition hold time</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>t_{LOW}</td><td>SCL low-level width period</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>t_{HIGH}</td><td>SCL high-level width period</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>$t_{SU:STA}$</td><td>Start condition setup time</td><td>IICB0WL / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>$t_{SU:STO}$</td><td>Stop condition setup time</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>t_{BUF}</td><td>Bus free time
(interval between stop condition and start condition)</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>$t_{HD:DAT}$</td><td>Data hold time</td><td>IICB0WL[9:2] / PCLK</td><td>IICB0WL[9:2] / PCLK</td></tr>
</table>


</td></tr>
</table>

No.4-33 18.6.1 Single Transfer Mode (3) Example of communications in single transfer mode (slave reception)

Unnecessary bit was deleted from <5> Data reception completion processing.

V10.00		V11.00	
Page	Description	Page	Revised Description
18-41	**[<5> Data reception completion processing]** • Set the IICBnCTL0.IICBnSLWT bit to 1 and the IICBnCTL0.IICBnSLAC bit to 0. • Next, exit the wait state by setting the IICBnTRG.IICBnWRET bit (to 1). The end of the data is notified to the transmitting device without outputting ACK.	18-41	**[<5> Data reception completion processing]** • Set the IICBnCTL0.IICBnSLAC bit to 0. • Next, exit the wait state by setting the IICBnTRG.IICBnWRET bit (to 1). The end of the data is notified to the transmitting device without outputting ACK.

No.4-34 21.7 System Protect Command Register (SYSPCMD)

Supplementary information was added to caution on operation after completion of writing to the system protect command register.

V10.00		V11.00	
Page	Description	Page	Revised Description
21-7	**[21.7 System Protect Command Register (SYSPCMD)]** **Cautions 1. A value is not written to the register in steps <1>, <2> and <3>.** **2. Be sure to clear this bit to 0 after the completion of writing to an applicable register.**	21-7	**[21.7 System Protect Command Register (SYSPCMD)]** **Cautions 1. A value is not written to the register in steps <1>, <2> and <3>.** **2. Be sure to clear this bit to 0 (setting for protection) after the completion of writing to an applicable register.**

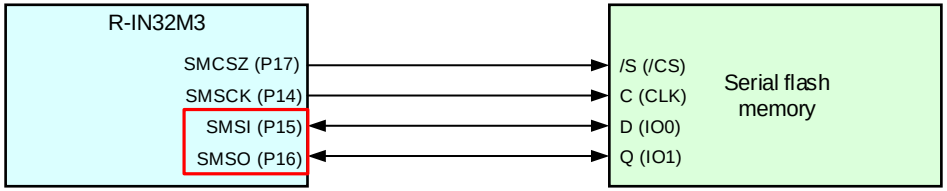
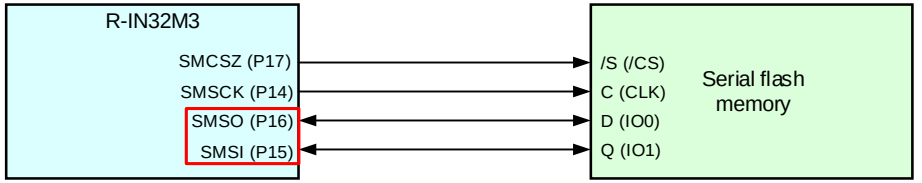
No.4-35 22. Debugging

The recommended in-circuit emulator (ICE), modified

V10.00		V11.00	
Page	Description	Page	Revised Description
22-1	**[22. Debugging)]** The recommended in-circuit emulators (ICE) to be connected to an R-IN32M3 are: I-jet (without trace feature) and JTAGjet (with trace feature) from IAR Systems, and adviceLUNA from Yokogawa Digital Computer Corporation.	22-1	**[22. Debugging]** The recommended in-circuit emulators (ICE) to be connected to an R-IN32M3 are: I-jet (without trace feature) and JTAGjet (with trace feature) from IAR Systems, and adviceLUNA II from DTS INSIGHT Corporation.

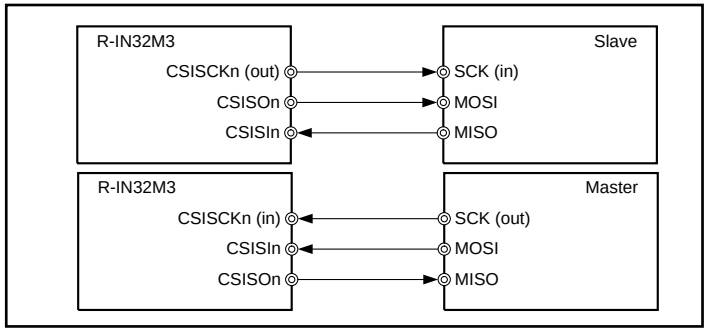
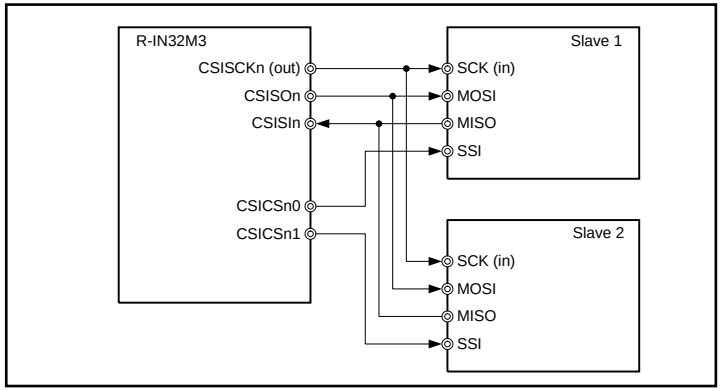
No.5-1 12. Serial Flash ROM Connection Pins

The names of R-IN pins were modified in the connection example.

V3.00		V4.00	
Page	Description	Page	Revised Description
37	**[Figure 12.1 Connection Example with Serial Flash ROM]** 	37	**[Figure 12.1 Connection Example with Serial Flash ROM]** 

No.5-2 17. CSIH Pins

A section was newly added.

V3.00		V4.00	
Page	Description	Page	Revised Description
-	N/A	42	**[17. CSIH Pins]** Newly added 17. CSIH Pins Examples of connections of an R-IN32M3 with a CSI master and slave are given below. 17.1 One Master and One Slave The following figure illustrates the connections between one master and one slave.  17.2 One Master and Two Slaves The following figure illustrates the connections between an R-IN32M3 as a master and two slaves. In this example, an R-IN32M3 supplies one chip select (CS) signal to each of the slaves. This signal is connected to the slave select input (SSI) of the slave. 

No.5-3 22.4 BSCAN Non-Supported Pins Non-supported pins were added.

<table>
<tr><th colspan="2">V3.00</th><th colspan="2">V4.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>49</td><td>[Table 21.1 List of BSCAN Non-Supported Pins]

R-IN32M3-EC
XT1
XT2
PONRZ
:
LX
EXTRES
.</td><td>50</td><td>[Table 22.1 List of BSCAN Non-Supported Pins]

R-IN32M3-EC
XT1
XT2
PONRZ
:
LX
EXTRES
FB
P0_SD_N
P1_SD_N
.</td></tr>
</table>

No.5-4 22.6 Notes on Using BSDL

A section was newly added.

<table>
<tr><th colspan="2">V3.00</th><th colspan="2">V4.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>-</td><td>N/A</td><td>51</td><td>[22.6 Notes on Using BSDL]

When the BSDL file is used, the control cell that is not used on the BSDL may cause the following errors. When the error occurs, treat it as a pseudo error.

Error log <Partially excerpted>:

Error, Line 1112, Control cell 236 does not enable any driver.
Error, Line 1112, Control cell 238 does not enable any driver.
Error, Line 1112, Control cell 240 does not enable any driver.
Error, Line 1112, Control cell 242 does not enable any driver.
Error, Line 1112, Control cell 244 does not enable any driver.
Error, Line 1112, Control cell 246 does not enable any driver.</td></tr>
</table>

No.5-5 25. Thermal Design

Section title was modified.

V3.00		V4.00	
Page	Description	Page	Revised Description
53	**[24 Guide to Design]** 24 Guide to Thermal Design This section describes the thermal characteristics of the R-IN32M3, and includes notes that require attention in the design of the board on which the device is mounted in terms of the dissipation of heat and the prevention of abnormal heating. Since the R-IN32M3-EC incorporates an Ethernet PHY module, large-capacity memory, and a regulator, it requires greater consideration of heat than most devices. Design the board and casing in consideration of heat dissipation.	54	**[25.Thermal Design]** 25 Thermal Design This section describes the thermal characteristics of the R-IN32M3, and includes notes that require attention in the design of the board on which the device is mounted in terms of the dissipation of heat and the prevention of abnormal heating. Since the R-IN32M3-EC incorporates an Ethernet PHY module, large-capacity memory, and a regulator, it requires greater consideration of heat than most devices. Design the board and casing in consideration of heat dissipation.

No.5-6 26. Countermeasure for Noise

Description on stopping clock output as a countermeasure for noise was added.

V3.00		V4.00	
Page	Description	Page	Revised Description
-	N/A	64	**[26. Countermeasure for Noise]** Newly added 26.1 Stopping Clock Output If the BUSCLK pin is not in use, output on the pin from an R-IN32M3 can be stopped. See section 2.2.2, Clock Control Registers (CLKGTD0, CLKGTD1) in the *R-IN32M3 Series User's Manual: Peripheral Modules* regarding control of the GCBCLK bit in the CLKGTD0 register, which enables or disables output from the BUSCLK pin.

No.6-1 1.2 Development Environment

The information on the recommended in-circuit emulator was changed.

<table>
<tr><th colspan="2">V5.00</th><th colspan="2">V6.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>2</td><td>[Table 1.1 List of Software Development Tools (Tool Chain)]
<table>
<tr><th>Tool Chain</th><th>IDE</th><th>Compiler</th><th>Debugger</th><th>ICE</th></tr>
<tr><td>KEIL MDK-ARM</td><td>µVision V5.18.0.0 (ARM)</td><td>µVision V5.18.0.0 (ARM)</td><td>µVision V5.18.0.0 (ARM)</td><td>ULINK2 ULINKpro (ARM)</td></tr>
<tr><td>GNU</td><td>-</td><td>Sourcery G++ Lite for ARM EABI 2012.09-63 (Mentor Graphics)</td><td>microVIEW-PLUS Ver.5.11PL3 (Yokogawa Digital Computer)</td><td>adviceLUNA 2.03-00 (Yokogawa Digital Computer)</td></tr>
<tr><td>IAR</td><td>Embedded Workbench for ARM V6.60.1 (IAR Systems)</td><td>Embedded Workbench for ARM V6.60.1 (IAR Systems)</td><td>Embedded Workbench for ARM V6.60.1 (IAR Systems)</td><td>I-jet JTAGjet-Trace-CM (IAR Systems)</td></tr>
</table></td><td>2</td><td>[Table 1.1 List of Software Development Tools (Tool Chain)]
<table>
<tr><th>Tool Chain</th><th>IDE</th><th>Compiler</th><th>Debugger</th><th>ICE</th></tr>
<tr><td>Keil MDK-Arm</td><td>µVision V5.18.0.0 (Arm)</td><td>µVision V5.18.0.0 (Arm)</td><td>µVision V5.18.0.0 (Arm)</td><td>ULINK2 ULINKpro (Arm)</td></tr>
<tr><td>GNU</td><td>-</td><td>Sourcery G++ Lite for ARM EABI 2012.09-63 (Mentor Graphics)</td><td>microVIEW-PLUS Ver.5.11PL3 (DTS INSIGHT Corporation)</td><td>adviceLUNA 2.03-00 (DTS INSIGHT Corporation)</td></tr>
<tr><td>IAR</td><td colspan="3">Embedded Workbench for Arm (Please use the latest version) (IAR Systems)</td><td>I-jet JTAGjet-Trace-CM (IAR Systems)</td></tr>
</table></td></tr>
</table>

No.6-2 3.2.1 Memory Maps

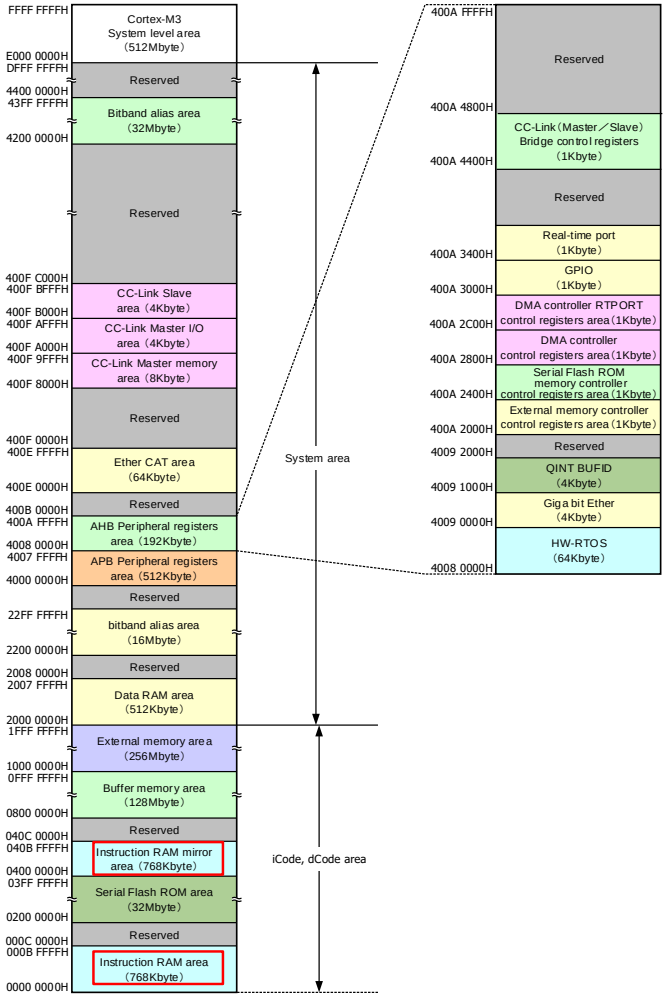
Note regarding the instruction RAM mirror area was

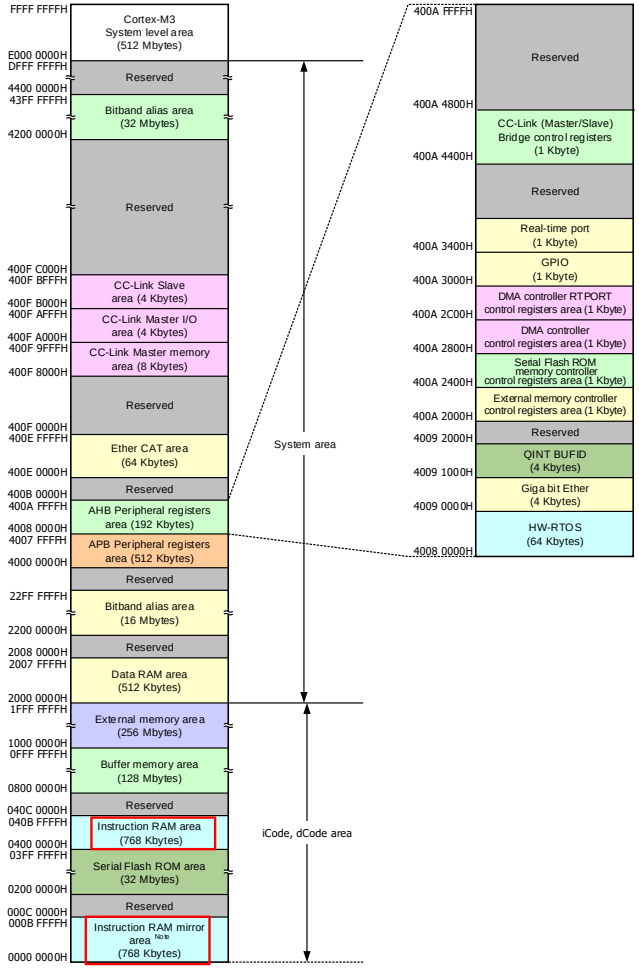
<table>
<tr><th colspan="2">V5.00</th><th colspan="2">V6.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>11</td><td>[3.2.1 Memory Map]
N/A</td><td>11</td><td>[3.2.1 Memory Maps]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.</td></tr>
<tr><td>12</td><td>[3.2.1 Memory Map]
N/A</td><td>12</td><td>[3.2.1 Memory Maps]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.</td></tr>
<tr><td>15</td><td>[3.2.1 Memory Map]
N/A</td><td>15</td><td>[3.2.1 Memory Maps]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
</table></td></tr>
<tr><td>16</td><td>[3.2.1 Memory Map]
N/A</td><td>16, 17</td><td>[3.2.1 Memory Maps]
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr>
</table></td></tr>
</table>

No.6-3 3.2.1 Memory Maps [1/2]

Locations of "Instruction RAM area" and "Instruction RAM mirror area" were corrected.

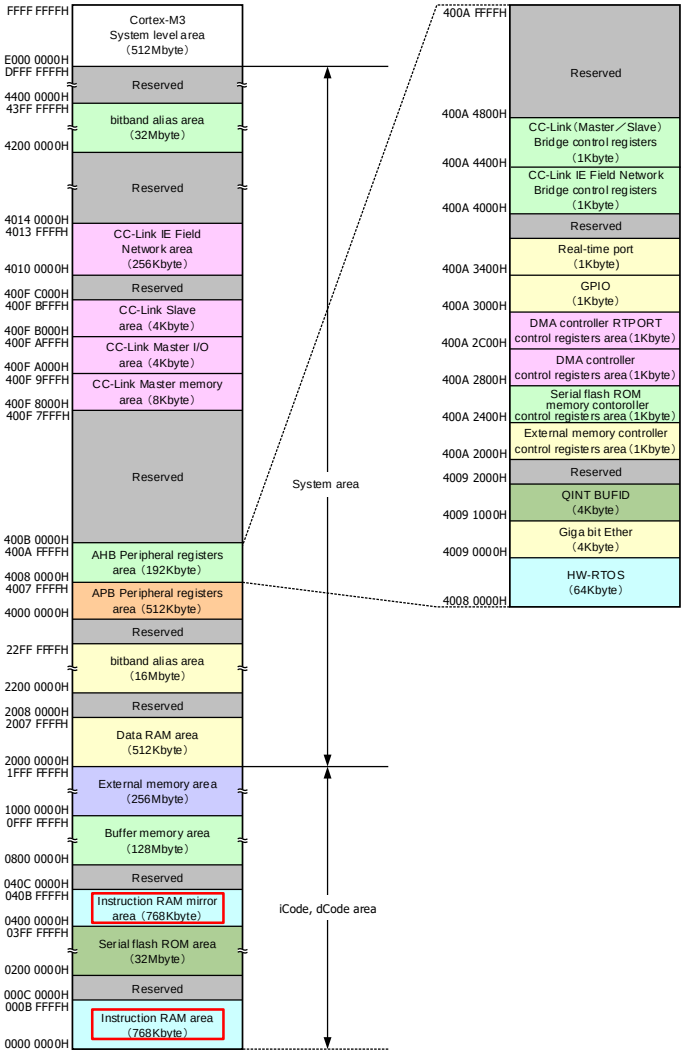
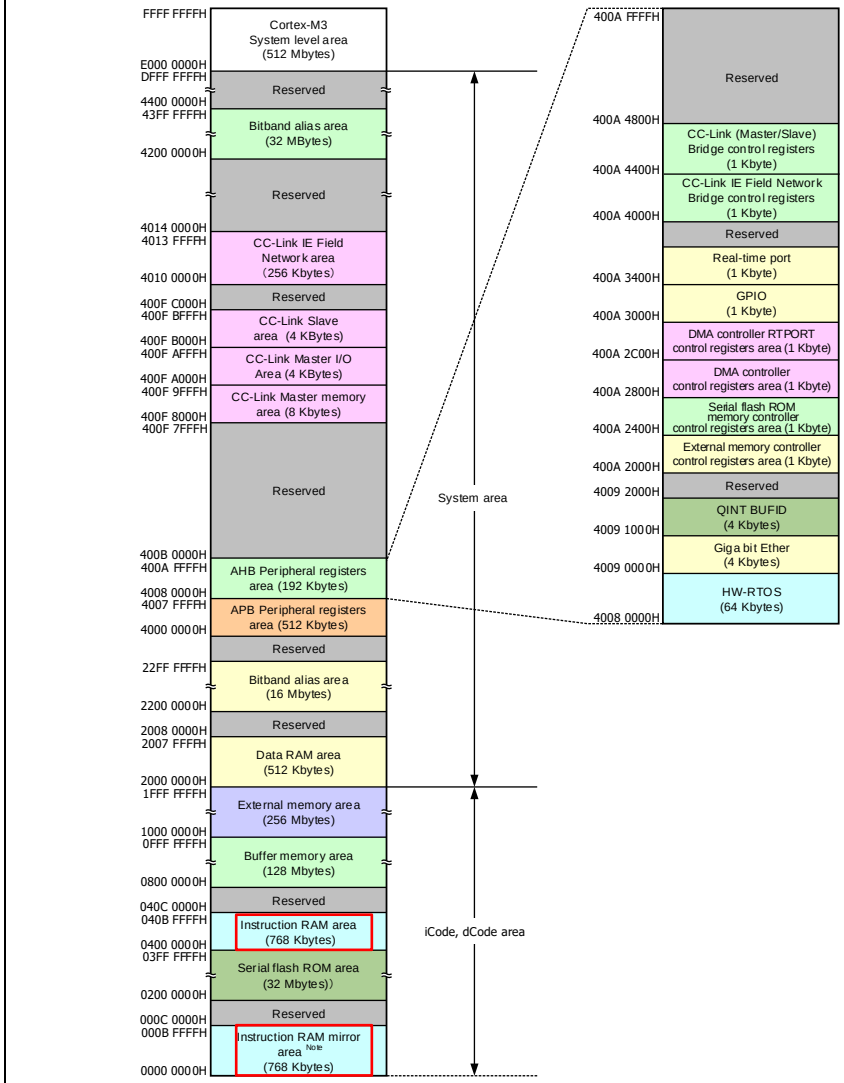
V5.00		V6.00	
Page	Description	Page	Revised Description
11	**[Figure 3.2 Entire Memory Map (R-IN32M3-EC)]**	11	**[Figure 3.2 Entire Memory Map (R-IN32M3-EC)]**





No.6-3 3.2.1 Memory Maps [2/2]

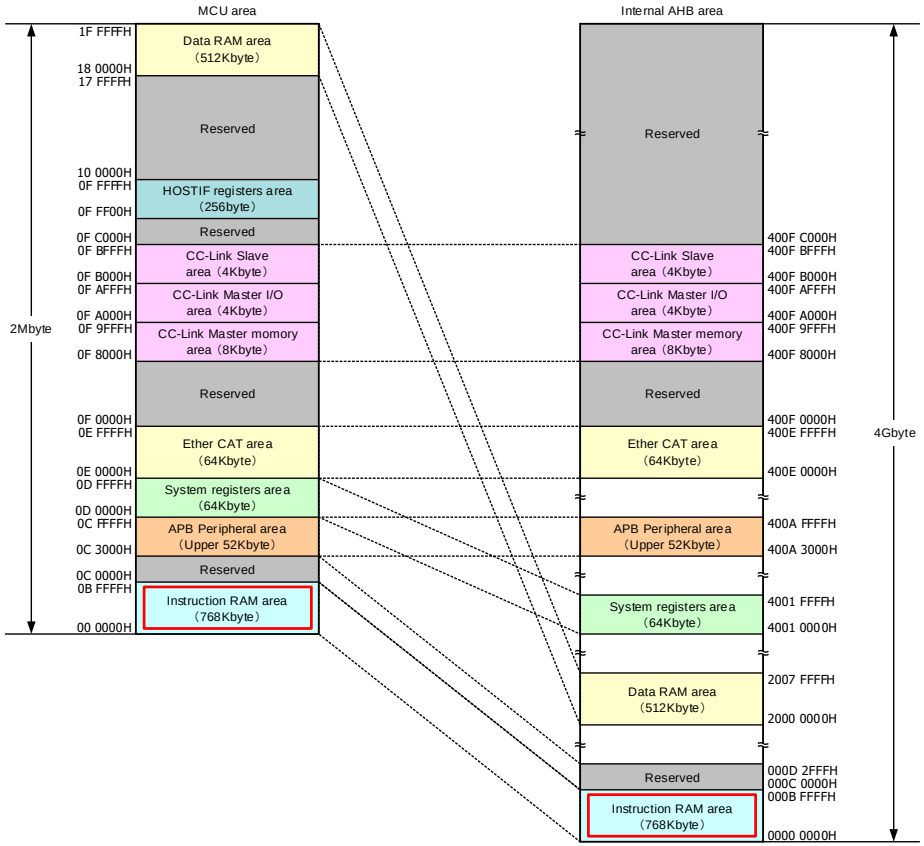
Locations of "Instruction RAM area" and "Instruction RAM mirror area" were corrected.

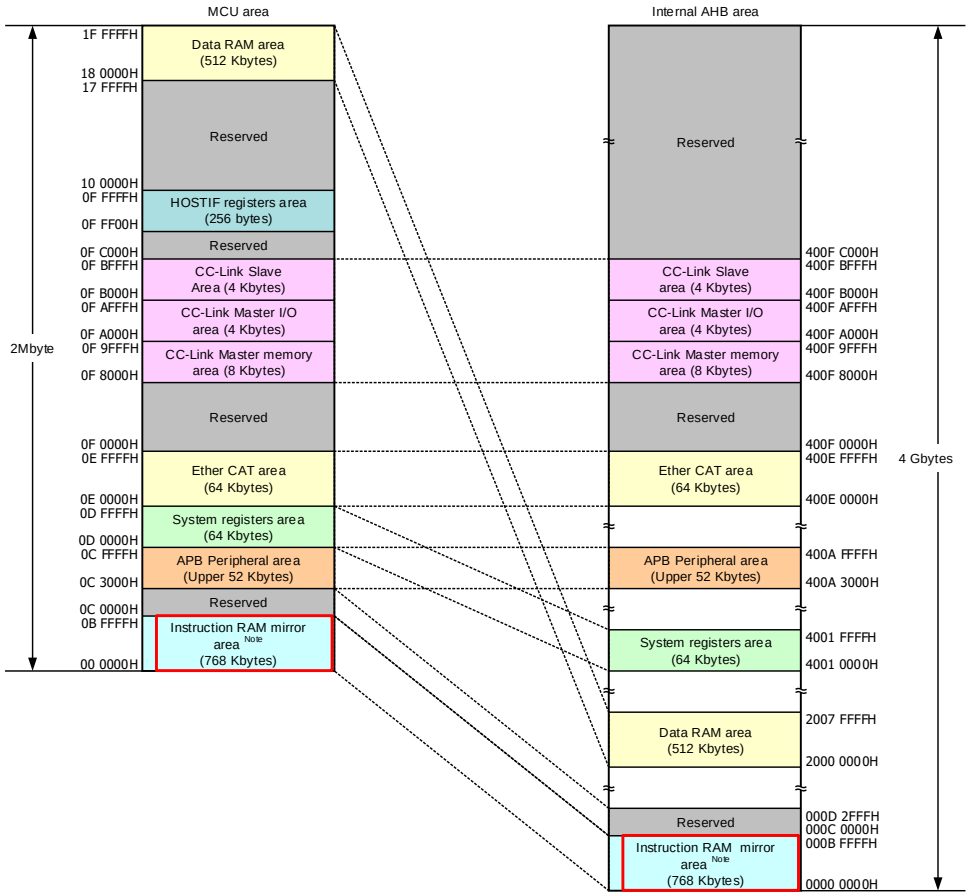
V5.00		V6.00	
Page	Description	Page	Revised Description
12	**[Figure 3.3 Entire Memory Map (R-IN32M3-CL)]** 	12	**[Figure 3.3 Entire Memory Map (R-IN32M3-CL)]** 

No.6-4 3.2.1 Memory Maps [1/2]

"Instruction RAM area" was corrected to "Instruction RAM mirror area".

V5.00		V6.00	
Page	Description	Page	Revised Description
15	**[Figure 3.7 External MCU Interface Space (R-IN32M3-EC)]**	15	**[Figure 3.7 External MCU Interface Space (R-IN32M3-EC)]**

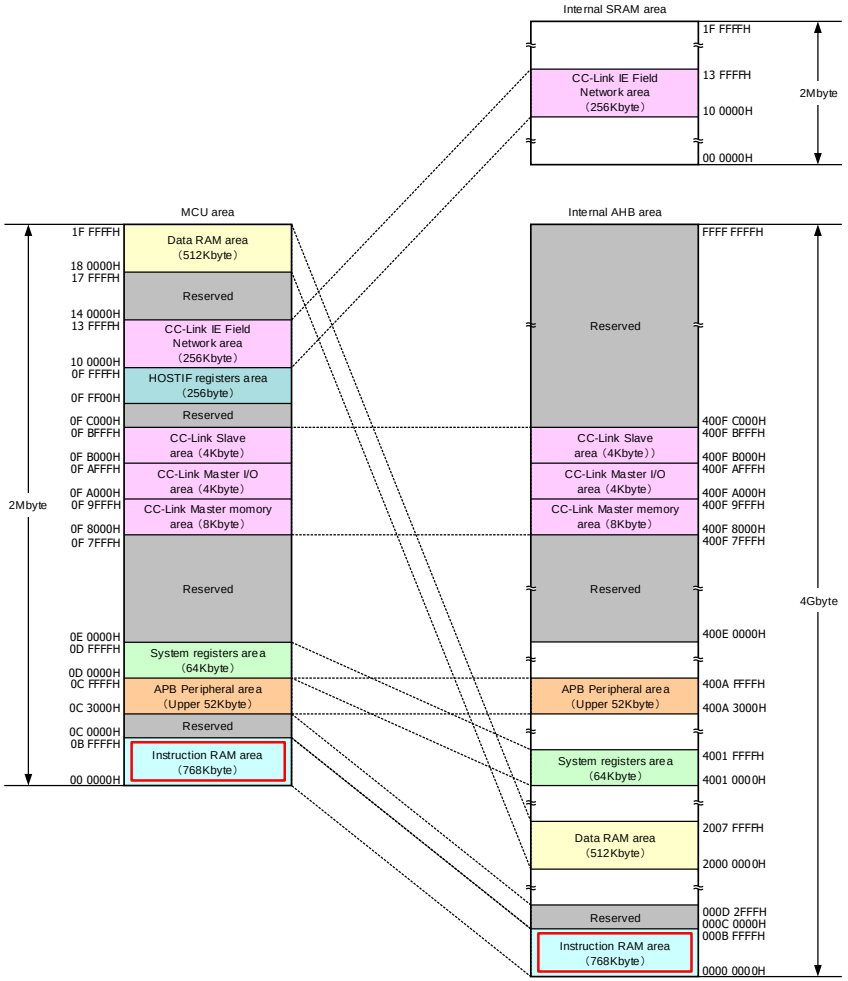


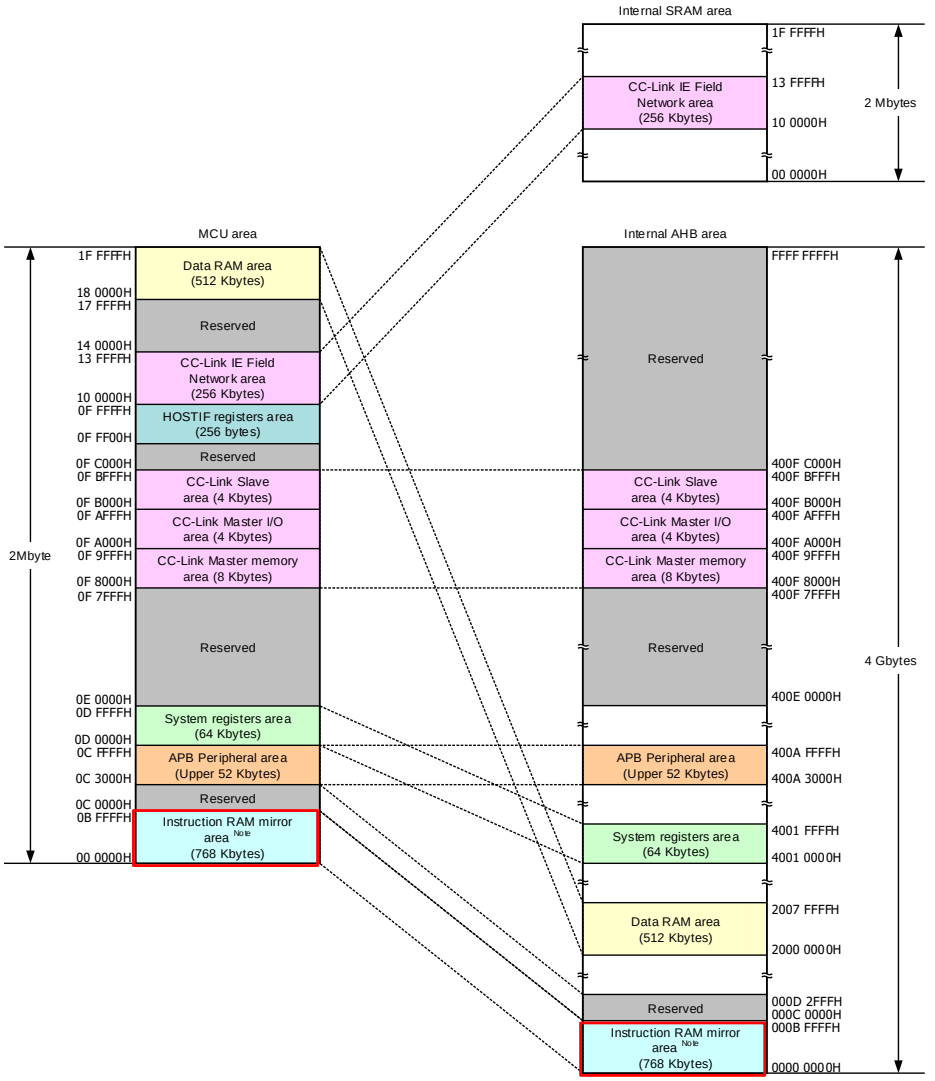


No.6-4 3.2.1 Memory Maps [2/2]

"Instruction RAM area" was corrected to "Instruction RAM mirror area".

V5.00		V6.00	
Page	Description	Page	Revised Description
16	**[Figure 3.8 External MCU Interface Space (R-IN32M3-CL)]**	16	**[Figure 3.8 External MCU Interface Space (R-IN32M3-CL)]**





No.6-5 6.4.1 Initialization of IIC Controller

Timing setting values were modified and supplementary information was added.

V5.00		V6.00	
Page	Description	Page	Revised Description
35	**[(4) Function]** This function makes initial settings for the IIC controller of the selected channel. ER_PARAM is returned if the selected channel is not 0 or 1. • IIC clock setting > Fast mode: 400 kHz • IIC timing setting > Stop and start interval : 80×PCLK > Setup cycles Start condition : 80×PCLK Stop condition : 45×PCLK Write data : 2×PCLK > Hold cycles Start condition : 45×PCLK Data : 80×PCLK Write data : 0×PCLK Read data : 2×PCLK **Remark: The IIC clock setting "400 kHz" is based on the assumption that both the rise and fall times of SDAn and SCLn are 20 ns. Change the register settings appropriately according to your usage environment. For details, refer to the R-IN32M4 Series User's Manual; Peripheral Modules.**	36	**[(4) Function]** This function makes initial settings for the IIC controller of the selected channel. ER_PARAM is returned if the selected channel is not 0 or 1. • IIC clock setting > Fast mode: 400 kHz • IIC timing setting > Stop and start interval : 130 × PCLK cycle (ns) SCL low-level width : 130 × PCLK cycle (ns) SCL high-level width : 116 × PCLK cycle (ns) > Setup cycles Start condition : 116 × PCLK cycle (ns) Stop condition : 116 × PCLK cycle (ns) > Hold cycles Start condition : 116 × PCLK cycle (ns) Data : 32 × PCLK cycle (ns) **Remarks 1. The IIC clock setting "400 kHz" is based on the assumption that both the rise and fall times of SDAn and SCLn are 20 ns. Change the register settings appropriately according to your usage environment. For details, refer to the R-IN32M3 Series User's Manual: Peripheral Modules.** **2. PCLK cycle = 10 ns**

No.6-6 6.5.5 Confirmation of Received Data (for Slave)

The description was corrected. (Tx mode → Rx mode)

V5.00		V6.00	
Page	Description	Page	Revised Description
46	**[(4) Function]** When the selected CSI controller is in Rx mode, the return value is presence of CSI received data. When the CSI controller is in master mode, ER_ NOTYET (no received data) is always returned because received data is not stored. ER_PARAM is returned if the channel selection argument is not 0 or 1. If the CSI controller is not in Tx mode, ER_INVAL (mode error) is returned.	47	**[(4) Function]** When the selected channel is in Rx mode, the return value is presence of CSI received data. When the CSI controller is in master mode, ER_ NOTYET (no received data) is always returned because received data is not stored. ER_PARAM is returned if the channel selection argument is not 0 or 1. If the CSI controller is not in Rx mode, ER_INVAL (mode error) is returned.

No.6-7 6.9 CAN Control

The section on the CAN control was added.

V5.00		V6.00	
Page	Description	Page	Revised Description
-	N/A	57 to 76	**[6.9 CAN Control]** The following sections were added. 6.9.1 Enabling CAN controller 6.9.2 Initialization of CAN Controller 6.9.3 Forced Termination of CAN Controller 6.9.4 Acquisition of CAN Operating Mode 6.9.5 Setting CAN Operating Mode 6.9.6 Acquisition of CAN Reception Data (CANID, Data, DLC) 6.9.7 Acquisition of CAN Reception Data (Data, DLC) 6.9.8 Setting CAN Transmission Data (CAN_ID, Data, DLC) 6.9.9 Setting CAN Transmission Data 6.9.10 Request of CAN Data Transmission 6.9.11 Acquisition of CAN Data Transmission Information 6.9.12 Acquisition of Reception Buffer Number of CAN Data 6.9.13 Acquisition of CAN Cannel Status 6.9.14 Clearing CAN Channel Status 6.9.15 Acquisition of CAN Bus Status

No.7-1 3. Specified Parts and Recommended Parts

One zener diode, added

<table>
<tr><th colspan="2">V1.01</th><th colspan="2">V1.02</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>4</td><td>[Table 3.1 Recommended Parts]

<table>
<tr><th>Product Name</th><th>Model Name^{Note1}</th><th>Manufacturer</th></tr>
<tr><td>Filter</td><td>MCT7050-A401</td><td>Sinka Japan Co.,ltd.</td></tr>
<tr><td>RS485 transceiver</td><td>SN75ALS181NS</td><td>Texas Instruments Japan, Inc.</td></tr>
<tr><td>Zener diode</td><td>RD6.2Z</td><td>Renesas Electronics.</td></tr>
</table></td><td>4</td><td>[Table 3.1 Recommended Parts]

<table>
<tr><th>Product Name</th><th>Model Name^{Note1}</th><th>Manufacturer</th></tr>
<tr><td>Filter</td><td>MCT7050-A401</td><td>Sinka Japan Co., ltd.</td></tr>
<tr><td>RS485 transceiver</td><td>SN75ALS181NS</td><td>Texas Instruments Japan, Inc.</td></tr>
<tr><td rowspan="2">Zener diode</td><td>RD6.2Z</td><td>Renesas Electronics.</td></tr>
<tr><td>STZU6.2NT146</td><td>ROHM Co., Ltd.</td></tr>
</table></td></tr>
</table>

No.7-2 5. CC-Link Remote Device Station Pins

The function of the IOTENSU pin, Low fixed, was

<table>
<tr><th colspan="2">V1.01</th><th colspan="2">V1.02</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>6</td><td>[Table 5.1 Correspondence between CC-Link Remote Device Station Pins and R-IN32M3 Series Pins]
<table><tr><th>CC-Link Pin Name</th><th>R-IN32M3 Pin Name</th><th>Shared Port</th><th>Description</th></tr><tr><td>IOTENSU</td><td>CCS_IOTENSU</td><td>P22</td><td>Initial setting pin</td></tr></table></td><td>6</td><td>[Table 5.1 Correspondence between CC-Link Remote Device Station Pins and R-IN32M3 Series Pins]
<table><tr><th>CC-Link Pin Name</th><th>R-IN32M3 Pin Name</th><th>Shared Port</th><th>Description</th></tr><tr><td>IOTENSU</td><td>CCS_IOTENSU</td><td>P22</td><td>Initial setting pin (Low fixed)</td></tr></table></td></tr>
<tr><td>8</td><td>[Table 5.2 Correspondence between CC-Link Remote Device Station Pins and R-IN32M4-CL2 Pins]
<table><tr><th>CC-Link Pin Name</th><th>R-IN32M4-CL2 Pin Name</th><th>Shared Port</th><th>Description</th></tr><tr><td>IOTENSU</td><td>CCS_IOTENSU</td><td>P22</td><td>Initial setting pin</td></tr></table></td><td>8</td><td>[Table 5.2 Correspondence between CC-Link Remote Device Station Pins and R-IN32M4-CL2 Pins]
<table><tr><th>CC-Link Pin Name</th><th>R-IN32M4-CL2 Pin Name</th><th>Shared Port</th><th>Description</th></tr><tr><td>IOTENSU</td><td>CCS_IOTENSU</td><td>P22</td><td>Initial setting pin (Low fixed)</td></tr></table></td></tr>
</table>

No.7-3 6.1 Setting the Number of Occupied Stations

Caution on the IOTENSU pin, modified

V1.01		V1.02	
Page	Description	Page	Revised Description
9	**[6.1 Setting the Number of Occupied Stations]** **Caution When the IOTENSU terminal is set to "H," the number of I/O points is fixed at 32, regardless of the Number of Occupied Stations setting.**	9	**[6.1 Setting the Number of Occupied Stations]** **Caution: Fix the IOTENSU pin to the low level. Setting the pin to the high level is prohibited.**

No.7-4 14.1 Circuit Design in General, (3) Questions and Answers Related to Switches, Connectors, and Terminal Blocks

Answer updated and items added

<table>
<tr><th colspan="2">V1.01</th><th colspan="2">V1.02</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>72</td><td>[14.1 Circuit Design in General, (3) Questions and Answers Related to Switches, Connectors, and Terminal Blocks]
<table>
<tr><th></th><th>Question</th><th>Answer</th></tr>
<tr><td>2</td><td>Regarding the setting of the station number
We are planning to fix the station number instead of using a rotary switch. Does this specification pose any problems?</td><td>Station number setting is mandatory. This is because if the customer cannot set the station number freely, it may not be possible to configure a system.
It is, however, all right to use dip switches or software processing instead of a rotary switch.</td></tr>
<tr><td>3</td><td>We want to install a communication connector (RS485) on the bottom surface of the station. Does this pose any problems? (We will make it possible to insert and remove the connector.)</td><td>It is all right to layout the connector as you like.</td></tr>
<tr><td>4</td><td>There is no specification for the external form. Can we decide the following as we like?
[1] The shape, layout, color, and size of the LEDs
[2] The type of connectors (we are considering
the use of Conbicon connectors made by Phoenix.)
[3] The size and type of rotary and dip switches (we are considering the use of S-3011A switches made by Copal.)</td><td>There is no specification for parts except the specified parts.
[1] Any design can be used for the LEDs.
[2] Use 2-piece connectors. If 2-piece connectors cannot be used, please specify in your manual that this product cannot be replaced in the link operation status (without shutting down the entire link). (Online connection and disconnection are not possible.)
[3] Any design can be used for the switches.</td></tr>
</table></td><td>72</td><td>[14.1 Circuit Design in General, (3) Questions and Answers Related to Switches, Connectors, and Terminal Blocks]
<table>
<tr><th></th><th>Question</th><th>Answer</th></tr>
<tr><td>2</td><td>Regarding the setting of the station number
We are planning to fix the station number instead of using a rotary switch. Does this specification pose any problems?</td><td>According to the CC-link standard, the station number should be freely configurable.</td></tr>
<tr><td>3</td><td>Could the station number be set by software?</td><td>There is no register to set the station number directly.
Station number is set by pin setting of "station number setting switch input terminal (CCS_STATION_NO_0-CCS_STATION_NO_7)".
When no switch is mounted, it is possible to set the station number by connecting the pins of "station number setting switch input terminal" to any general-purpose ports and setting the station number from the general-purpose port by software.
After setting the station number, the reset of CC-Link block should be released.</td></tr>
<tr><td>4</td><td>We want to install a communication connector (RS485) on the bottom surface of the station. Does this pose any problems? (We will make it possible to insert and remove the connector.)</td><td>It is all right to layout the connector as you like.</td></tr>
<tr><td>5</td><td>There is no specification for the external form. Can we decide the following as we like?
[1] The shape, layout, color, and size of the LEDs
[2] The type of connectors (we are considering
the use of Conbicon connectors made by Phoenix.)
[3] The size and type of rotary and dip switches (we are considering the use of S-3011A switches made by Copal.)</td><td>There is no specification for parts except the specified parts.
[1] Any design can be used for the LEDs.
[2] Use 2-piece connectors. If 2-piece connectors cannot be used, please specify in your manual that this product cannot be replaced in the link operation status (without shutting down the entire link). (Online connection and disconnection are not possible.)
[3] Any design can be used for the switches.</td></tr>
</table></td></tr>
</table>