

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.



RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
 RenesasTechnology Corp.

Product Category	MPU&MCU	Document No.	TN-380-A066A/E	Rev.	1.00
Title	Revisions for Timer Y Specifications in 38D2 Group Datasheet.		Information Category	Technical Notification	
Applicable Product	M38D24G4-XXXFP/HP, M38D24G4FP/HP M38D24G6-XXXFP/HP, M38D24G6FP/HP M38D28G8-XXXFP/HP, M38D28G8FP/HP M38D29GC-XXXFP/HP, M38D29GCFP/HP M38D29GF-XXXFP/HP, M38D29GFFP/HP M38D29FFF/HP, M38D29T-RLFS	Lot No. --	Reference Document	38D2 Group Datasheet	

Timer Y specifications in the 38D2 Group datasheet (Rev.2.01 REJ03B0177-0201) have been revised as follows.

Corrections

The real time port control bits (bits 1 and 0 in the timer Y mode register) for the real time port function of the 38D2 Group timer Y have been revised.

The real time port control bits control P46 and P47 together. "002" and "112" are the only valid setting values for these bits. Do not set "012" and "102" to these bits.

As per the above, the following descriptions in the datasheet have been revised.

- (1) Real time port control description
- (2) Structure of timer Y related registers
- (3) Block diagram of timer Y

Applicable descriptions in the 38D2 Group datasheet Rev.2.01 will be revised and uploaded in Rev.3.00.

Descriptions

- (1) Real time port control description

<Before corrections>

When the real time port function is valid, data for the real time port is output from ports P46 and P47 each time the timer Y underflows.(However, if the real time port control bit is changed from "0" to "1" after the data for real time port is set, data is output independent of the timer Y operation.) When the data for the real time port is changed while the real time port function is valid, the changed data is output at the next underflow of timer Y. Before using this function, set the corresponding port direction registers to output mode.

<After corrections>

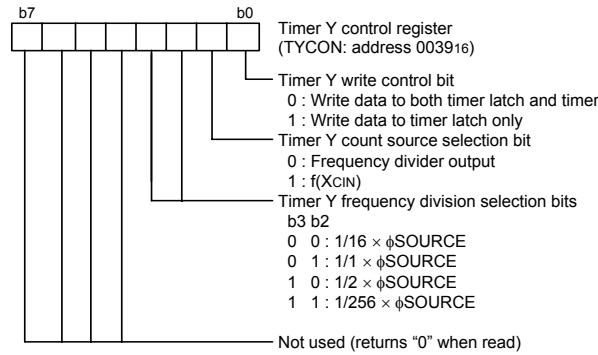
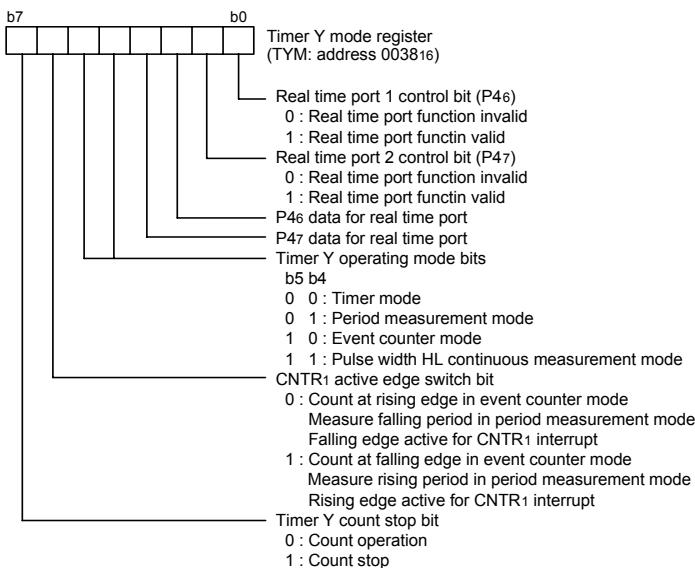
When the real time port function is valid, data for the real time port is output from ports P46 and P47 each time the timer Y underflows.

(However, if the real time port control bits are changed from "002" to "112" after both data for real time ports are set, data are output independent of the timer Y operation.) When either or both data for real time ports are changed while the real time port function is valid, the changed data is output at the next underflow of timer Y.

When switching the setting of the real time port control bits between valid and invalid, write to the timer Y mode register in byte units with the LDM or STA instruction so that both bits are switched at the same time. Also, before using this function, set the P46 and P47 port direction registers to output.

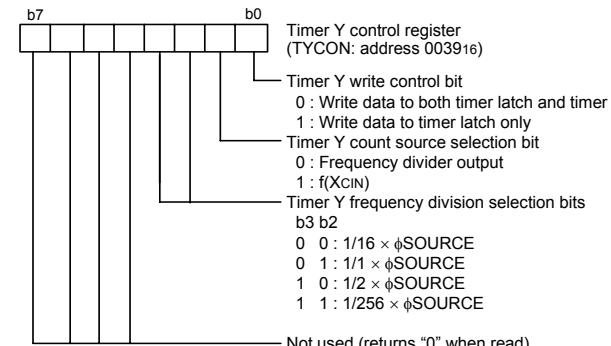
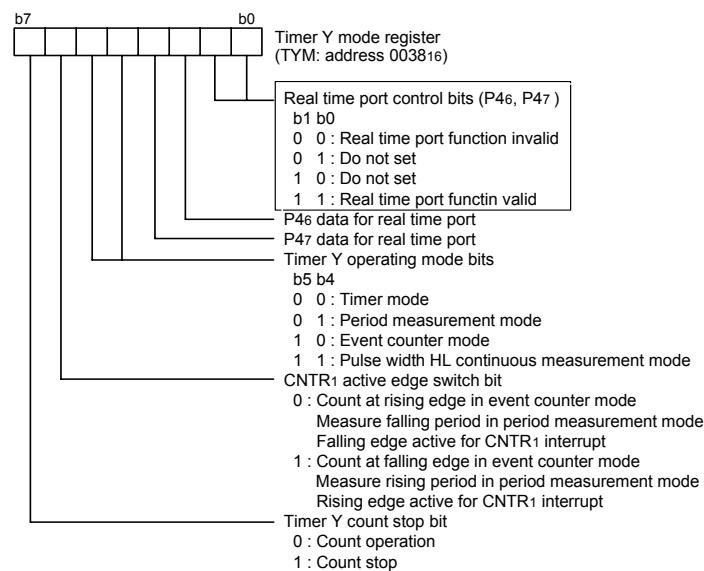
(2) Structure of timer Y related registers

<Before corrections>



φ SOURCE: represents the supply source of internal clock φ.
XIN input: in the frequency/2, 4 or 8 mode,
Internal on-chip oscillator divided by 4 in the on-chip
oscillator mode, and Sub clock in the low-speed mode.

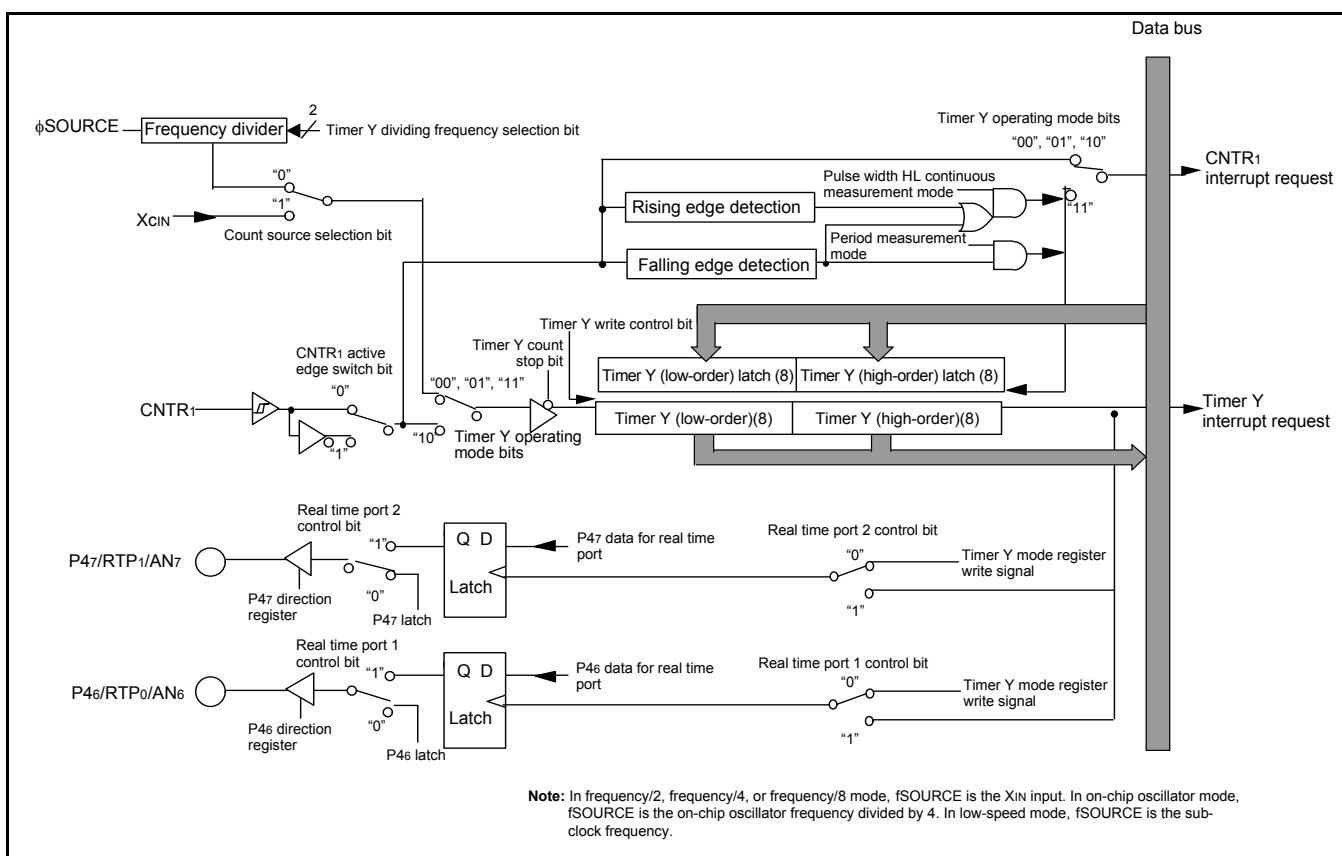
<After corrections>



φ SOURCE: represents the supply source of internal clock φ.
XIN input: in the frequency/2, 4 or 8 mode,
Internal on-chip oscillator divided by 4 in the on-chip
oscillator mode, and Sub clock in the low-speed mode.

(3) Block diagram of timer Y

<Before corrections>



<After corrections>

