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Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-740-A109A/E	Rev.	1.00
Title	Revision of Serial I/O2 Specification in 7542 Group Datasheet		Information Category	Technical Notification		
Applicable Product	M37542RSS M37542M2-XXXXFP/GP/SP/HP, M37542M2T-XXXXFP/GP M37542M2V-XXXXFP/GP M37542M4-XXXXFP/GP/SP/HP, M37542M4T-XXXXFP/GP M37542M4V-XXXXFP/GP M37542F8FP/GP/SP/*HP (*:Only ES version, MP: no plan) M37542F8TFP/GP, M37542F8VFP/GP	Lot No.	Reference Document	7542 Group Datasheet		

As for the 7542 Group Datasheet, the Specification for Serial I/O2 is revised as shown below.

Please confirm the contents of revision.

<Contents of revision>

In the 7542 Group, the output structure of the TxD2 pin is CMOS output only.

The N-channel open-drain output of the TxD2 pin is not available.

Accordingly, we revise the Datasheet [Rev.2.06] by eliminating the description of the N-channel open-drain output of the TxD2 pin in Serial I/O2, and release it as Rev.3.00.

<Revised Page in the Datasheet>

Refer to the attached document "Revised Page in 7542 Group Datasheet."

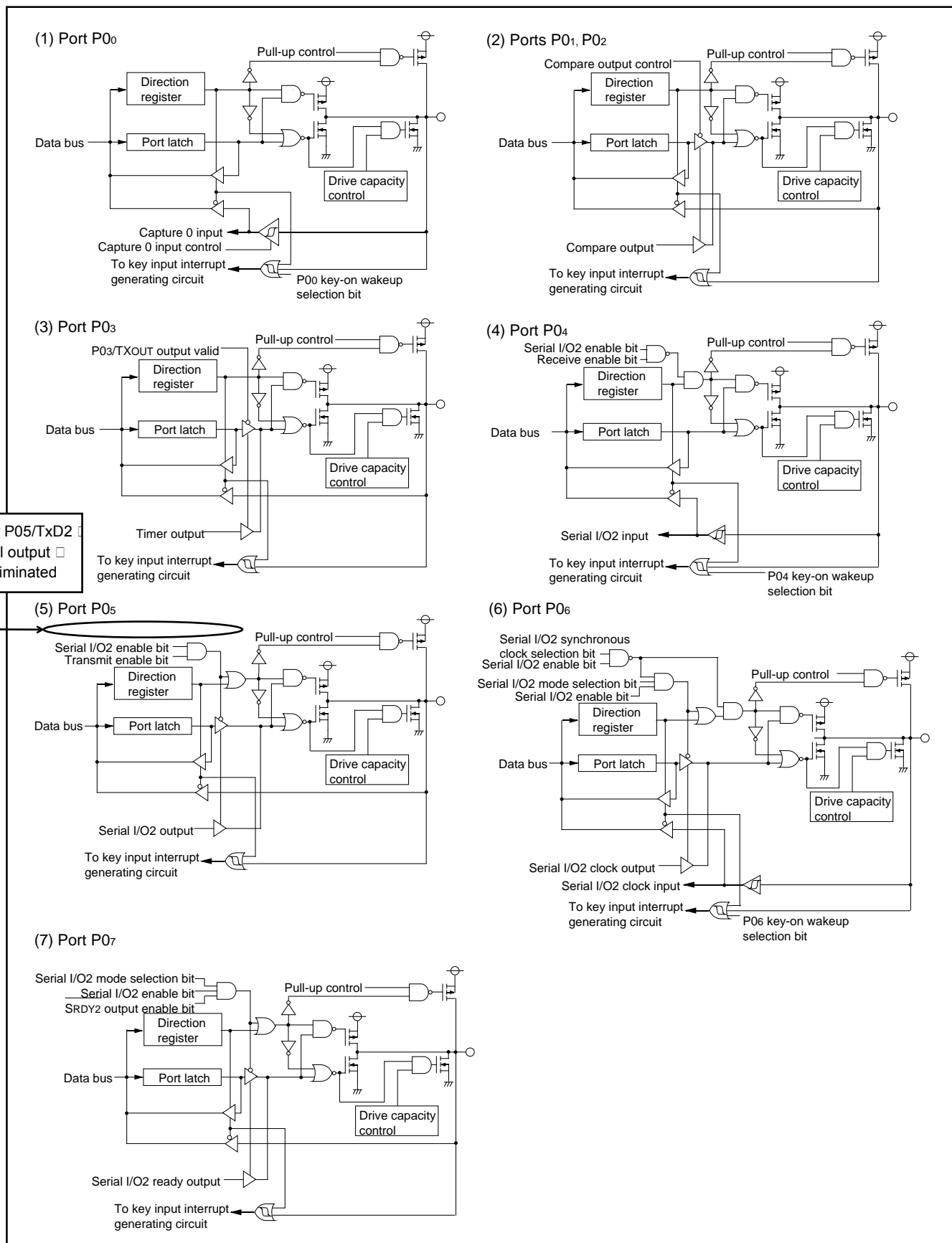


Fig. 20 Block diagram of ports (1)

Serial I/O

The 7542 Group has Serial I/O1 and Serial I/O2. Except that Serial I/O1 has the bus collision detection function and the Tx/D2 output structure for Serial I/O2 is CMOS only, they have the same function.

Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

Description of Tx/D2 output structure in Serial I/O2 added.

(1) Clock Synchronous Serial I/O1 Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6) to "1".

For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

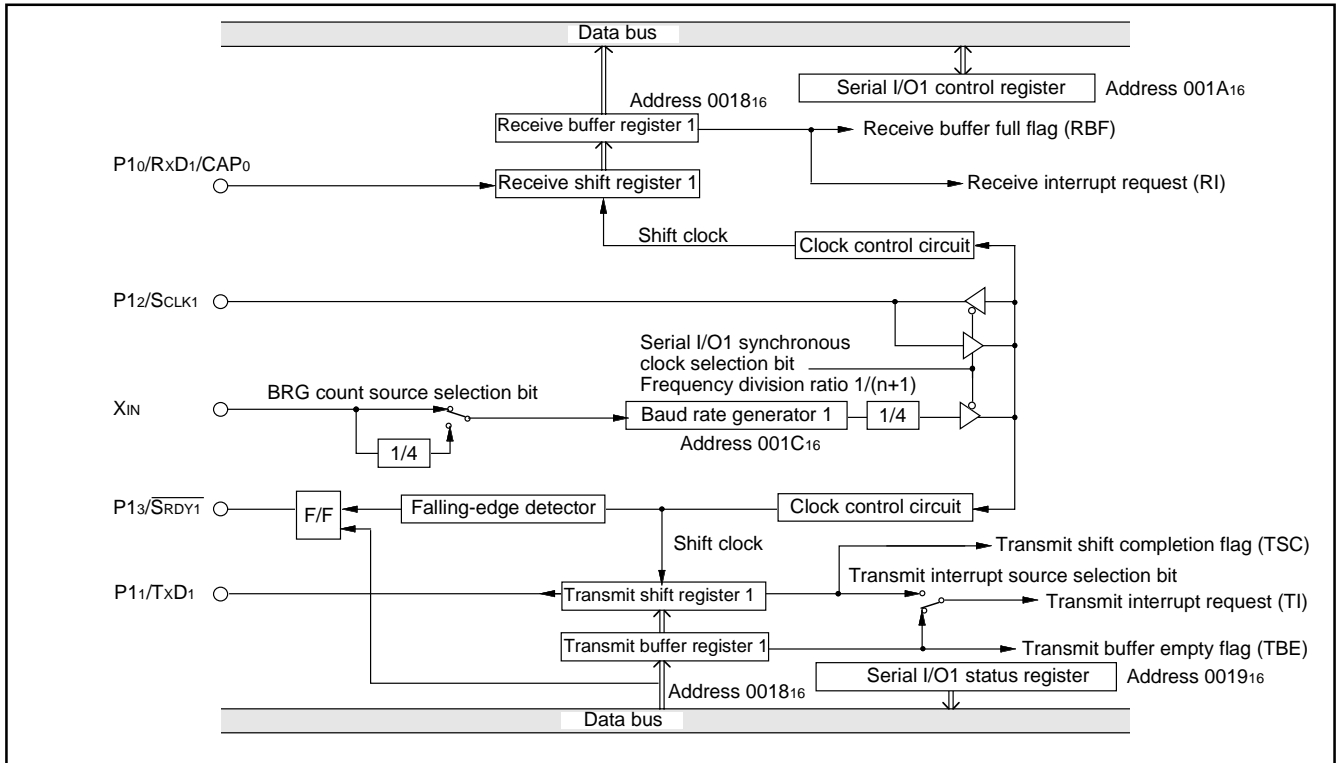
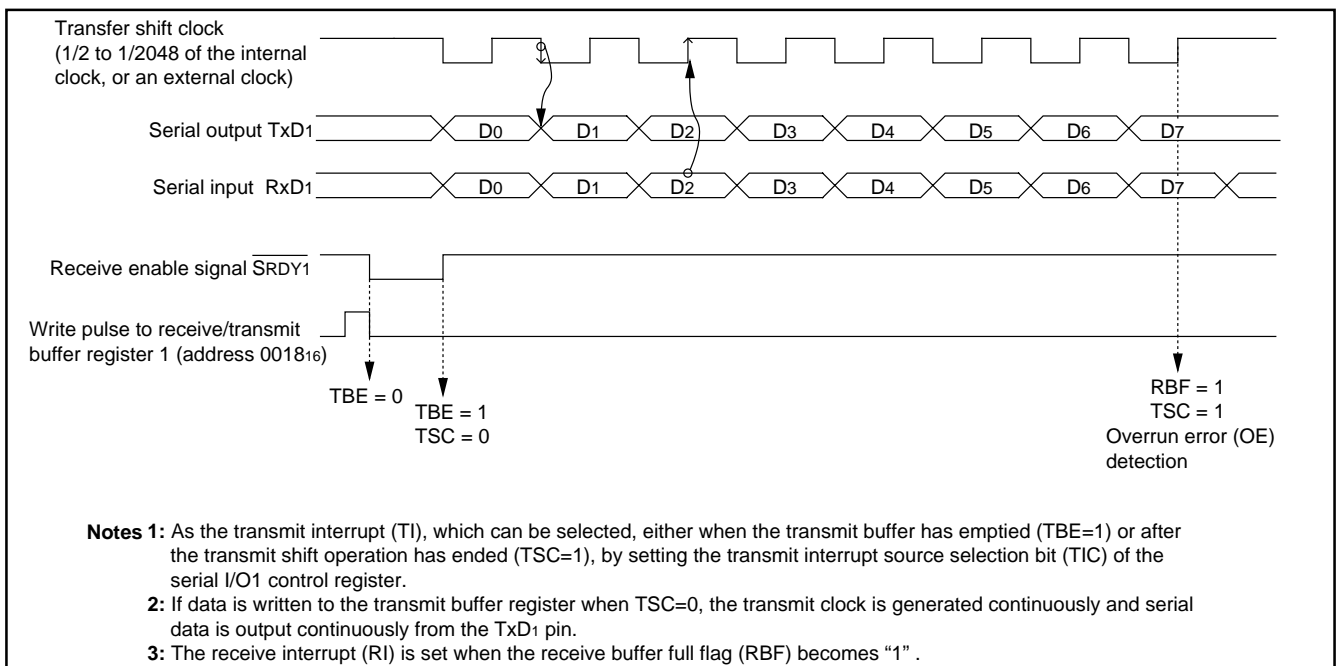


Fig. 52 Block diagram of clock synchronous serial I/O1



- Notes 1:** As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
- 2:** If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the Tx/D1 pin.
- 3:** The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1".

Fig. 53 Operation of clock synchronous serial I/O1 function

[Transmit buffer register 2/receive buffer register 2 (TB2/RB2)] 002E16

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O2 status register (SIO2STS)] 002F16

The read-only serial I/O2 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O2 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O2 enable bit SIOE (bit 7 of the serial I/O2 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O2 status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O2 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O2 control register (SIO2CON)] 003016

The serial I/O2 control register consists of eight control bits for the serial I/O2 function.

[UART2 control register (UART2CON)] 003116

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer.

[Baud rate generator 2 (BRG2)] 003216

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■ Notes on Serial I/O2**• Serial I/O interrupt**

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ⑤ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O2 is enabled.

The functions of P06 and P07 are switched with the setting values of a serial I/O2 mode selection bit and a serial I/O2 synchronous clock selection bit as follows.

(1) Serial I/O2 mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

Setup of a serial I/O2 synchronous clock selection bit

"0" : P06 pin turns into an output pin of a synchronous clock.

"1" : P06 pin turns into an input pin of a synchronous clock.

Setup of a $\overline{\text{SRDY2}}$ output enable bit (SRDY)

"0" : P07 pin can be used as a normal I/O pin.

"1" : P07 pin turns into a $\overline{\text{SRDY2}}$ output pin.

(2) Serial I/O2 mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

Setup of a serial I/O2 synchronous clock selection bit

"0" : P06 pin can be used as a normal I/O pin.

"1" : P06 pin turns into an input pin of an external clock.

When clock asynchronous (UART) type serial I/O is selected, it is P07 pin. It can be used as a normal I/O pin.

Description of P05/TxD2 P-channel output disable bit eliminated

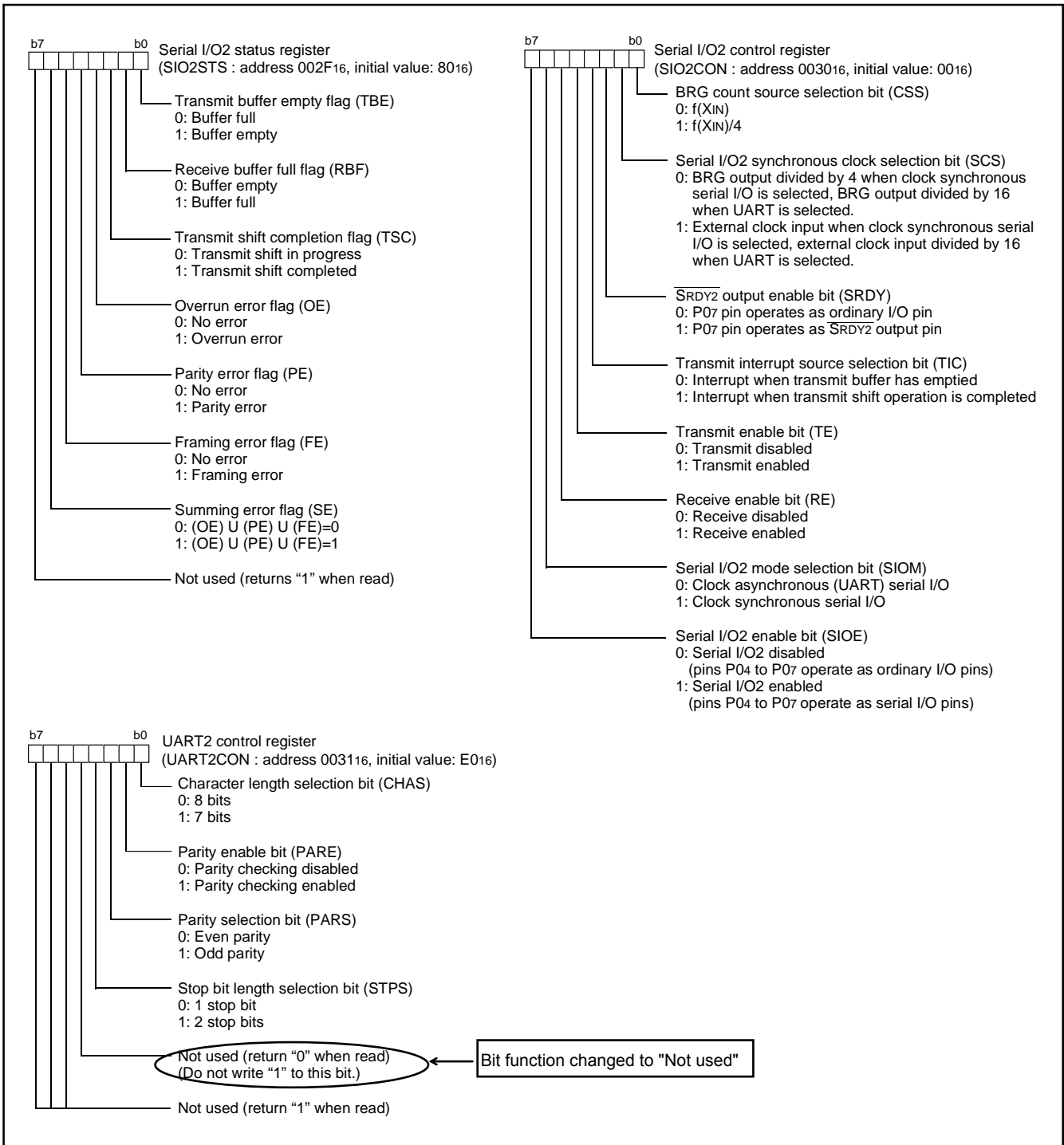


Fig. 64 Structure of serial I/O2-related registers

Electrical Characteristics (General purpose)

Table 16 Electrical characteristics (1)

(FLASH ROM version: VCC = 2.7 to 5.5V, Mask ROM version: VCC = 2.2 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00–P07, P10–P14, P20–P27, P30–P37 (Note 1)	IOH = -5 mA VCC = 4.0 to 5.5 V	VCC-1.5			V
		IOH = -1.0 mA Mask ROM: VCC = 2.2 to 5.5 V FLASH ROM: VCC = 2.7 to 5.5 V	VCC-1.0			V
VOL	"L" output voltage P00–P07, P30–P37 (Drive capacity = "L") P10–P14, P20–P27	IOL = 5 mA VCC = 4.0 to 5.5 V			1.5	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 1.0 mA Mask ROM: VCC = 2.2 to 5.5 V FLASH ROM: VCC = 2.7 to 5.5 V			1.0	V
VOL	"L" output voltage P00–P07, P30–P37 (Drive capacity = "H")	IOL = 15 mA VCC = 4.0 to 5.5 V			2.0	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 1.0 mA Mask ROM: VCC = 2.2 to 5.5 V FLASH ROM: VCC = 2.7 to 5.5 V			1.0	V
VT+–VT–	Hysteresis CNTR0, INT0, INT1, CAP0, CAP1 (Note 2) P00–P07 (Note 3)			0.4		V
VT+–VT–	Hysteresis RXD0, SCLK0, RXD1, SCLK1			0.5		V
VT+–VT–	Hysteresis RESET			0.5		V
IiH	"H" input current P00–P07, P10–P14, P20–P27, P30–P37	VI = VCC (Pin floating. Pull up transistors "off")			5.0	μA
IiH	"H" input current RESET	VI = VCC			5.0	μA
IiH	"H" input current XIN	VI = VCC		4.0		μA
IiL	"L" input current P00–P07, P10–P14, P20–P27, P30–P37	VI = VSS (Pin floating. Pull up transistors "off")			-5.0	μA
IiL	"L" input current RESET	VI = VSS			-5.0	μA
IiL	"L" input current XIN	VI = VSS		-4.0		μA
IiL	"L" input current P00–P07, P30–P37	VI = VSS (Pull up transistors "on")		-0.2	-0.5	mA
VRAM	RAM hold voltage	When clock stopped	2.0		5.5	V
ROSC	On-chip oscillator oscillation frequency	VCC = 5.0 V, Ta = 25 °C	1000	2000	3000	kHz
DOSC	Oscillation stop detection circuit detection frequency	VCC = 5.0 V, Ta = 25 °C	62.5	125	187.5	kHz

Notes: 1: P11 is measured when the P11/TXD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is "0".

2: RXD1, SCLK1, INT0, and INT1 (P36 selected) have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).

3: It is available only when operating key-on wake up.

Description of P05 eliminated.

Electrical Characteristics (Extended operating temperature version)

Table 29 Electrical characteristics (1)

(FLASH ROM version: VCC = 2.7 to 5.5V, Mask ROM version: VCC = 2.4 to 5.5 V, VSS = 0 V, Ta = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00–P07, P10–P14, P20–P27, P30–P37 (Note 1)	IOH = -5 mA VCC = 4.0 to 5.5 V	VCC-1.5			V
		IOH = -1.0 mA Mask ROM: VCC = 2.4 to 5.5 V FLASH ROM: VCC = 2.7 to 5.5 V	VCC-1.0			V
VOL	"L" output voltage P00–P07, P30–P37 (Drive capacity = "L") P10–P14, P20–P27	IOL = 5 mA VCC = 4.0 to 5.5 V			1.5	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 1.0 mA Mask ROM: VCC = 2.4 to 5.5 V FLASH ROM: VCC = 2.7 to 5.5 V			1.0	V
VOL	"L" output voltage P00–P07, P30–P37 (Drive capacity = "H")	IOL = 15 mA VCC = 4.0 to 5.5 V			2.0	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 1.0 mA Mask ROM: VCC = 2.4 to 5.5 V FLASH ROM: VCC = 2.7 to 5.5 V			1.0	V
VT+–VT–	Hysteresis CNTR0, INT0, INT1, CAP0, CAP1 (Note 2) P00–P07 (Note 3)			0.4		V
VT+–VT–	Hysteresis RXD0, SCLK0, RXD1, SCLK1			0.5		V
VT+–VT–	Hysteresis RESET			0.5		V
IiH	"H" input current P00–P07, P10–P14, P20–P27, P30–P37	VI = VCC (Pin floating. Pull up transistors "off")			5.0	μA
IiH	"H" input current RESET	VI = VCC			5.0	μA
IiH	"H" input current XIN	VI = VCC		4.0		μA
IiL	"L" input current P00–P07, P10–P14, P20–P27, P30–P37	VI = VSS (Pin floating. Pull up transistors "off")			-5.0	μA
IiL	"L" input current RESET	VI = VSS			-5.0	μA
IiL	"L" input current XIN	VI = VSS		-4.0		μA
IiL	"L" input current P00–P07, P30–P37	VI = VSS (Pull up transistors "on")		-0.2	-0.5	mA
VRAM	RAM hold voltage	When clock stopped	2.0		5.5	V
ROSC	On-chip oscillator oscillation frequency	VCC = 5.0 V, Ta = 25 °C	1000	2000	3000	kHz
DOSC	Oscillation stop detection circuit detection frequency	VCC = 5.0 V, Ta = 25 °C	62.5	125	187.5	kHz

Notes: 1: P11 is measured when the P11/TXD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is "0".

2: RXD1, SCLK1, INT0, and INT1 (P36 selected) have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).

3: It is available only when operating key-on wake up.

Description of P05 eliminated.