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Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	Micro-controller			No	TN-SH7-397A/E	
THEME	Revision of the incorrect information in the SH7144 Hardware Manual and information on the use of the I^2C bus interface	Classification of Information	1. Spec change 2. Supplement of Documents 3. Limitation of Use	4. Change of Mask 5. Change of Production Line		
PRODUCT NAME	SH7144 series	Lot No. ALL	Reference Documents	SH7144 Series Hardware Manual	Rev. 1.0	Effective Date Permanent

Incorrect information in the SH7144 Hardware Manual has been revised. In addition, the limitation on use of the I^2C bus interface is now described.

1. Incorrect information

Revision 1: Model names in list of on-chip memory capacities on page 2

(Incorrect)

Version	Model Name	ROM	RAM	Remarks
Flash memory version	HD64F7144	256 kbytes	8 kbytes	
	HD64F7145	256 kbytes	8 kbytes	
Mask ROM version	HD6437144	256 kbytes	8 kbytes	
	HD6437145	256 kbytes	8 kbytes	

(Correct)

Version	Model Name	ROM	RAM	Remarks
Flash memory version	HD64F7144**F50***	256 kbytes	8 kbytes	
	HD64F7145**F50***	256 kbytes	8 kbytes	
Mask ROM version	HD6437144**F50***	256 kbytes	8 kbytes	
	HD6437145**F50***	256 kbytes	8 kbytes	

Note: Under development

Revision 2: Model names in list of number of general I/O ports on page 2

(Incorrect)

Model Name	I/O Ports	Input Ports
HD64F7144/HD6437144	74	8
HD64F7145/HD6437145	98	8

(Correct)

Model Name	I/O Ports	Input Ports
HD64F7144**F50*** /HD6437144**F50***	74	8
HD64F7145**F50*** /HD6437145**F50***	98	8

Note: Under development

Revision 3: Model names in package list on page 2

(Incorrect)

Model Name	Package	Code	Body Size	Pin Pitch
HD64F7144/HD6437144	QFP-112	FP-112B	20.0 ×20.0 mm	0.65 mm
HD64F7145/HD6437145	LQFP-144	FP-144F	20.0 ×20.0 mm	0.5 mm

(Correct)

Model Name	Package	Code	Body Size	Pin Pitch
HD64F7144**F50*** /HD6437144**F50***	QFP-112	FP-112B	20.0 ×20.0 mm	0.65 mm
HD64F7145**F50*** /HD6437145**F50***	LQFP-144	FP-144F	20.0 ×20.0 mm	0.5 mm

Note: Under development

Revision 4: Clock mode select in Table 3.2 on page 44

(Incorrect)

Clock Mode Number	Pin Setting		Clock Ratio (Input Clock = 1)	
	MD3	MD2	System Clock (ϕ)	Peripheral Clock (Pϕ)
0	0	0	x 1	x 1
1	0	1	x 2	x 2
2	1	0	x 4	x 4*
3	1	1	x 4	x 2

(Correct)

Clock Mode Number	Pin Setting		Clock Ratio (Input Clock = 1)		
	MD3	MD2	System Clock (ϕ)	Peripheral Clock (Pϕ)	System Clock Output (CK)
0	0	0	x 1	x 1	**x 1**
1	0	1	x 2	x 2	**x 2**
2	1	0	x 4	x 4*	**x 4**
3	1	1	x 4	x 2	**x 4**

Revision 5: List of type names in Appendix C on page 714

(Incorrect)

Version			Model Name	Package (Package Code)
SH7144	Flash memory version	Standard Product	HD64F7144	QFP-112 (FP-112B)
	Mask ROM version	Standard Product	HD6437144	QFP-112 (FP-112B)
SH7145	Flash memory version	Standard Product	HD64F7145	LQFP-144 (FP-144F)
	Mask ROM version	Standard Product	HD6437145	LQFP-144 (FP-144F)

(Correct)

Version			Model Name	Package (Package Code)
SH7144	Flash memory version	Standard Product	HD64F7144**F50***	QFP-112 (FP-112B)
	Mask ROM version	Standard Product	HD6437144**F50***	QFP-112 (FP-112B)
SH7145	Flash memory version	Standard Product	HD64F7145**F50***	LQFP-144 (FP-144F)
	Mask ROM version	Standard Product	HD6437145**F50***	LQFP-144 (FP-144F)

Note: Under development

2. Information on Use of I^2C Bus Interface

(1) In slave transmit operation of the I^2C bus interface module, when ICDR is read from or ICCR is read from or written to at the moment address reception is switched to data transmission, erroneous data may be transmitted.

In normal transmit operation, when a first frame is received and the received address matches, the TRS bit is automatically set to 1 and transmit mode is entered if the R/W bit of the 8th clock cycle is 1. The SCL pin is then fixed to low from the fall of the 9th clock of the first frame until the transmit data is written to the ICDR register.

However, when ICDR is read from or ICCR is read from or written to within 6 peripheral clock cycles (half-tone dot-meshing area in figure 1) after the rising edge of the 9th transmit/receive clock for address reception of the first frame, the SCL pin is not fixed low after the fall of the 9th clock for the first frame. The master device starts sending clock signals before the slave device has written transmit data to ICDR. As a result, data in the ICDR shift register is output to the SDA pin, and erroneous data is transmitted to the master device.

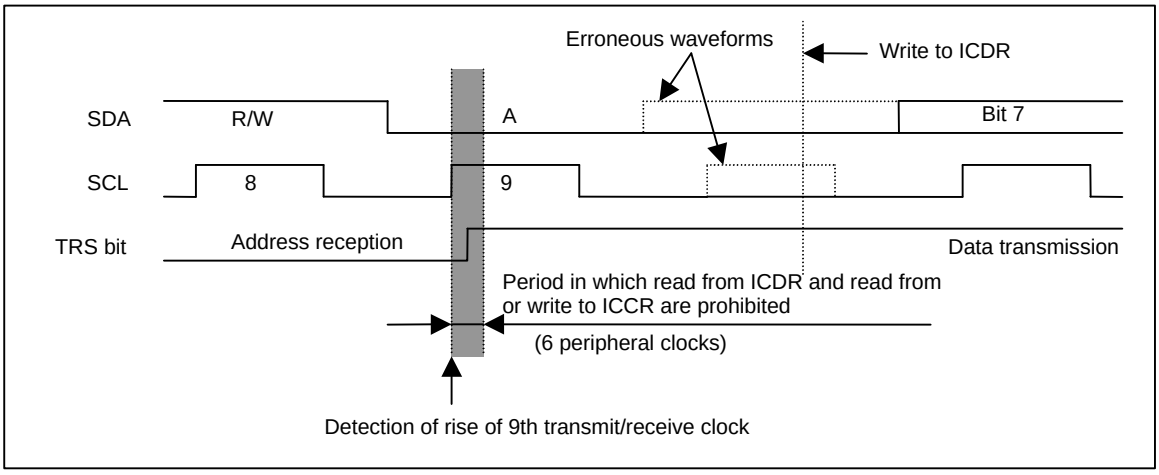

Figure 1 Scheme of Slave Transmit Operation

In slave transmit operation, do not read from ICDR or read from or write to ICCR during the period indicated by half-tone dot-meshing in figure 1.

For the interrupt processing that normally occurs in synchronization with the rising edge of the 9th transmit/receive clock, reading from ICDR or reading from or writing to ICCR causes no problems because the prohibited period ends before transiting to the interrupt processing.

To ensure that this interrupt processing is carried out, satisfy either of the following conditions.

i) Before the next slave address reception starts, complete the ICDR read operation and ICCR read/write operation.

ii) Monitor the BC2 to BC0 bits (bit counters 2 to 0) in ICMR, and when the BC2 to BC0 bits are all cleared to 0 (8th or 9th clock), wait for at least two transmit/receive clocks before reading from ICDR or reading from or writing to ICCR to avoid the period in which these operations will cause a failure.

(2) To change, without transiting to the stop condition, from slave transmit operation (TRS = 1) to next address receive operation (TRS= 0) by the input of resumption condition, clear TRS to 0 during time period (a) in figure 2, when the I2C bus interface in the SH7144 series is in slave mode.

In slave mode, the TRS bit setting in ICCR becomes valid as soon as the bit is set during the period from when the rising edge of the 9th clock or a stop condition is detected to the next rising edge at the SCL pin (period (a) in figure 2).

However, for any other period (i.e., period (b) in figure 2), the TRS bit setting is retained until the next rising edge of the 9th clock or a stop condition is detected, so that the TRS bit setting does not become valid immediately.

Accordingly, in the address reception following input of a resumption condition, the internally effective TRS bit setting remains 1 (transmit mode), and the acknowledge bit that should be transmitted at the end of address reception is not transmitted at the 9th transmit/receive clock.

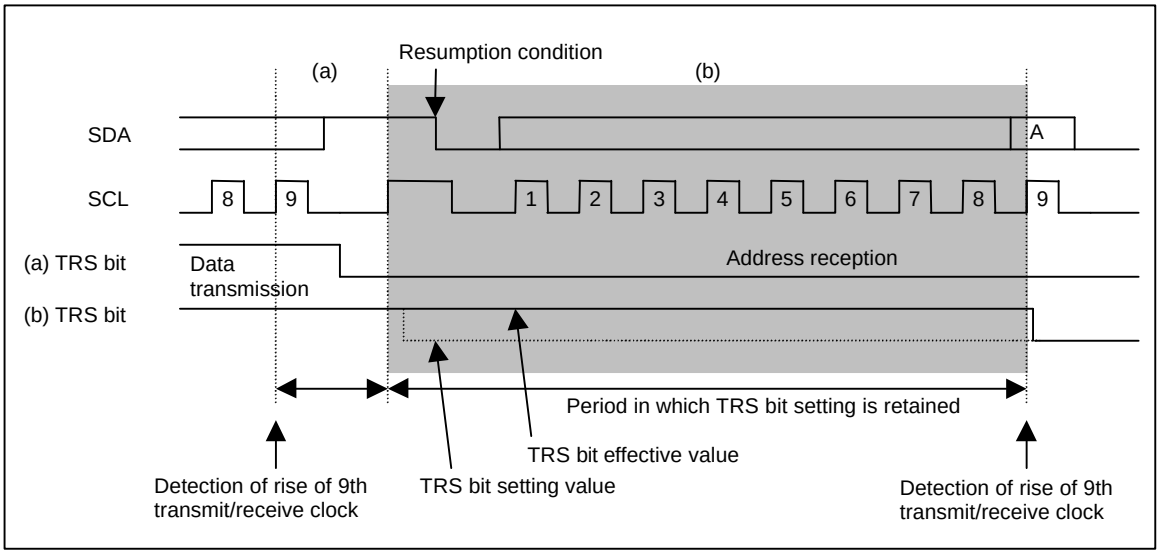

Figure 2 Scheme of TRS Bit Setting in Slave Mode