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RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SY*-A009A/E	Rev.	1.00
Title	Revised information of S7G2 User's Manual from Rev.1.10		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S7 Series S7G2	Lot No. All lots	Reference Document	S7G2 User's Manual: Microcontrollers, Rev.1.10		

1. 30.2.5 STCA Status Register (STSR)

[Before]

Address(es): EPTPC.STSR 4006 5040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	W10S	SYNTOUT	—	SYNCOUT	SYNC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4	W10S	Worst 10 Acquisition Completion Flag	0: Ten worst values not acquired yet 1: Ten worst values acquired.	R/W*1

W10S flag (Worst 10 Acquisition Completion Flag)

The W10S flag indicates that acquisition of the worst 10 values is complete.

[After]

Address(es): EPTPC.STSR 4006 5040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	W10D	SYNTOUT	—	SYNCOUT	SYNC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4	W10D	Worst 10 Acquisition Completion Flag	0: Ten worst values not acquired yet 1: Ten worst values acquired.	R/W*1

W10D flag (Worst 10 Acquisition Completion Flag)

The W10D flag indicates that acquisition of the worst 10 values is complete.

2. 30.2.6 STCA Status Notification Enable Register (STIPR)

[Before]

Address(es): EPTPC.STIPR 4006 5044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	W10S	SYNTOUT	—	SYNCOUT	SYNC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4	W10S	W10D Status Notification Enable	0: Disable notification of the STSR.W10D state 1: Enable notification of the STSR.W10D state.	R/W

[After]

Address(es): EPTPC.STIPR 4006 5044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	W10D	SYNTOUT	—	SYNCOUT	SYNC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4	W10D	W10D Status Notification Enable	0: Disable notification of the STSR.W10D state 1: Enable notification of the STSR.W10D state.	R/W

3. Table 59.27 IIC timing (1) (1 of 2)

[Before]

Table 59.27 IIC timing (1) (1 of 2)

Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.

The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

[After]

Table 59.27 IIC timing (1) (1 of 2)

Conditions:

(1) Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

(2) Use pins that have a letter appended to their names, for example “_A” or “_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

4. Table 59.28 IIC timing (2)

[Before]

Table 59.28 IIC timing (2)

(1) Setting of the SCL0_A, SDA0_A pins is not required with the port drive capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

[After]

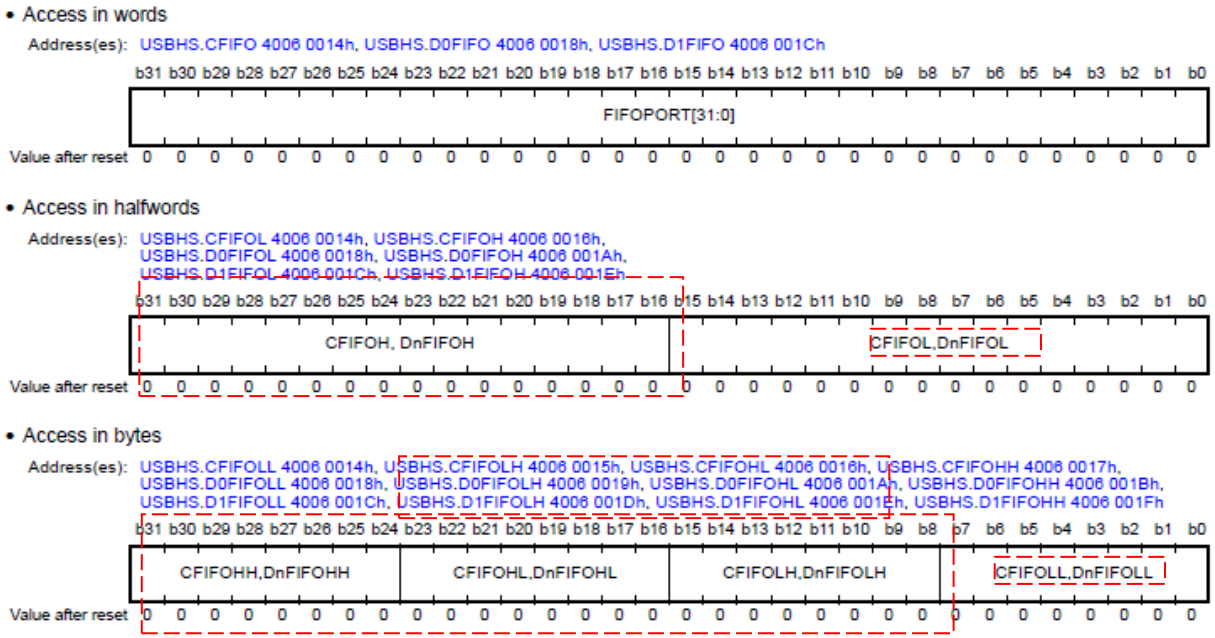
Table 59.28 IIC timing (2)

Conditions:

(1) Setting of the SCL0_A, SDA0_A pins is not required with the port drive capability bit in the PmnPFS register.

5. 33.2.7 CFIFO Port Register (CFIFO), D0FIFO Port Register (D0FIFO), D1FIFO Port Register (D1FIFO)

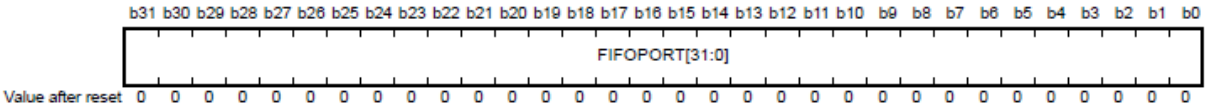
[Before]



[After]

- Access in words

Address(es): USBHS.CFIFO 4006 0014h, USBHS.D0FIFO 4006 0018h, USBHS.D1FIFO 4006 001Ch



- Access in halfwords

Address(es): USBHS.CFIFOL 4006 0014h, USBHS.CFIFOH 4006 0016h,
USBHS.D0FIFOL 4006 0018h, USBHS.D0FIFOH 4006 001Ah,
USBHS.D1FIFOL 4006 001Ch, USBHS.D1FIFOH 4006 001Eh

- Access in bytes

Address(es): USBHS.CFIFOLL 4006 0014h,
USBHS.D0FIFOLL 4006 0018h,
USBHS.D1FIFOLL 4006 001Ch,

USBHS.CFIFOHH 4006 0017h,
USBHS.D0FIFOHH 4006 001Bh,
USBHS.D1FIFOHH 4006 001Fh

6. 33.2.7 CFIFO Port Register (CFIFO), D0FIFO Port Register (D0FIFO), D1FIFO Port Register (D1FIFO)

[Before]

Table 33.6 Endian operation in 32-bit access (MBW[1:0] = 10b)

BIGEND	b31 to b24	b23 to b16	b15 to b8	b7 to b0
0	Located at N+3	Located at N+2	Located at N+1	Located at N+0
1	Located at N+0	Located at N+1	Located at N+2	Located at N+3

Table 33.7 Endian operation in 16-bit access (MBW[1:0] = 01b)

BIGEND	b31 to b24	b23 to b16	b15 to b8	b7 to b0
0	Access prohibited*1		Located at N+1	Located at N+0
1	Located at N+0	Located at N+1	Access prohibited*1	

Table 33.8 Endian operation in 8-bit access (MBW[1:0] = 00b)

BIGEND	b31 to b24	b23 to b16	b15 to b8	b7 to b0
0	Access prohibited*1			Located at N+0
1	Located at N+0	Access prohibited*1		

[After]

Table 33.6 Endian operation in 32-bit access (MBW[1:0] = 10b)

BIGEND	CFIFO, D0FIFO, D1FIFO **b31 to b24**	CFIFO, D0FIFO, D1FIFO **b23 to b16**	CFIFO, D0FIFO, D1FIFO **b15 to b8**	CFIFO, D0FIFO, D1FIFO **b7 to b0**	**Remarks**
0	Located at N+3	Located at N+2	Located at N+1	Located at N+0	Transmission data is sent from address N+0. Received data is stored from address N+0.
1	Located at N+0	Located at N+1	Located at N+2	Located at N+3	Transmission data is sent from address N+3. Received data is stored from address N+3.

Table 33.7 Endian operation in 16-bit access (MBW[1:0] = 01b)

BIGEND	CFIFOL, D0FIFOL, D1FIFOL **b15 to b8**	CFIFOL, D0FIFOL, D1FIFOL **b7 to b0**	CFIFOH, D0FIFOH, D1FIFOH **b15 to b8**	CFIFOH, D0FIFOH, D1FIFOH **b7 to b0**	**Remarks**
0	Access prohibited *1		Located at N+1	Located at N+0	Transmission data is sent from address N+0. Received data is stored from address N+0.
1	Located at N+0	Located at N+1	Access prohibited*1		Transmission data is sent from address N+1. Received data is stored from address N+1.

Table 33.8 Endian operation in 8-bit access (MBW[1:0] = 00b)

BIGEND	CFIFOLL, D1FIFOLL, D0FIFOLL	CFIFOHH, D1FIFOHH, D0FIFOHH
0	Access prohibited*1	Located at N+0
1	Located at N+0	Access prohibited*1

7. Table 59.1 Absolute maximum ratings

[Before]

Table 59.1 Absolute maximum ratings

Item	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB *2	–0.3 to +4.6	V
VBATT power supply voltage	VBATT	–0.3 to +4.6	V
Input voltage (except for 5V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5V-tolerant ports*1)	V_{in}	–0.3 to +5.8	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0 *2	–0.3 to +4.6	V
USBHS power supply voltage	VCC_USBHS	–0.3 to +4.6	V
USBHS analog power supply voltage	AVCC_USBHS	–0.3 to +4.6	V
Switching regulator power supply voltage	VCC_DCDC	–0.3 to +4.6	V
Analog input voltage	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating temperature*3 *4	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

[After]

Table 59.1 Absolute maximum ratings

Item	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB *2	–0.3 to +4.6	V
VBATT power supply voltage	VBATT	–0.3 to +4.6	V
Input voltage (except for 5V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5V-tolerant ports*1)	V_{in}	-0.3 to VCC+4.6 (max 5.8)	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0 *2	–0.3 to +4.6	V
USBHS power supply voltage	VCC_USBHS	–0.3 to +4.6	V
USBHS analog power supply voltage	AVCC_USBHS	–0.3 to +4.6	V
Switching regulator power supply voltage	VCC_DCDC	–0.3 to +4.6	V
Analog input voltage	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating temperature*3 *4	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

8. Table 59.4 I/O V_{IH}, V_{IL}

[Before]

Table 59.4 I/O V_{IH}, V_{IL}

Item			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	-	VCC + 0.3	V
			V_{IL}	–0.3	-	VCC × 0.3	
			ΔV_T	VCC × 0.05	-	-	
		IIC (except for SMBus)*2	V_{IH}	VCC × 0.7	-	5.8	
			V_{IL}	–0.3	-	VCC × 0.3	
			ΔV_T	VCC × 0.05	-	-	
		5V-tolerant ports*3	V_{IH}	VCC × 0.8	-	5.8	
			V_{IL}	–0.3	-	VCC × 0.2	
			ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2 (When V_{BATT} power supply is selected)	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3	
			V_{IL}	–0.3	-	V_{BATT} × 0.2	
			ΔV_T	V_{BATT} × 0.05	-	-	
		Other input pins*4	V_{IH}	VCC × 0.8	-	VCC + 0.3	
			V_{IL}	–0.3	-	VCC × 0.2	
			ΔV_T	VCC × 0.05	-	-	
	Ports	5V-tolerant ports*5	V_{IH}	VCC × 0.8	-	5.8	
			V_{IL}	–0.3	-	VCC × 0.2	
		Other input pins*6	V_{IH}	VCC × 0.8	-	VCC + 0.3	
			V_{IL}	–0.3	-	VCC × 0.2	

[After]

Table 59.4 I/O V_{IH}, V_{IL}

Item			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	-	VCC + 0.3	V
			V_{IL}	–0.3	-	VCC × 0.3	
			ΔV_T	VCC × 0.05	-	-	
		IIC (except for SMBus)*2	V_{IH}	VCC × 0.7	-	VCC +3.5 (max 5.8)	
			V_{IL}	–0.3	-	VCC × 0.3	
			ΔV_T	VCC × 0.05	-	-	
		5V-tolerant ports*3	V_{IH}	VCC × 0.8	-	VCC +3.5 (max 5.8)	
			V_{IL}	–0.3	-	VCC × 0.2	
			ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2 (When V_{BATT} power supply is selected)	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3	
			V_{IL}	–0.3	-	V_{BATT} × 0.2	
			ΔV_T	V_{BATT} × 0.05	-	-	
		Other input pins*4	V_{IH}	VCC × 0.8	-	VCC + 0.3	
			V_{IL}	–0.3	-	VCC × 0.2	
			ΔV_T	VCC × 0.05	-	-	
	Ports	5V-tolerant ports*5	V_{IH}	VCC × 0.8	-	VCC +3.5 (max 5.8)	
			V_{IL}	–0.3	-	VCC × 0.2	
		Other input pins*6	V_{IH}	VCC × 0.8	-	VCC + 0.3	
			V_{IL}	–0.3	-	VCC × 0.2	

9. 23.3.4 Automatic Dead Time Setting Function

[Before]

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time values (GTDVU and GTDVD values) can automatically be set to GTCCRB. The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Dead time can be separately set for the first half and second half of a waveform. Dead time for the transition in the first half of a negative waveform is set in GTDVU and that in the second half is set in GTDVD. The same dead time can also be set for the first and second halves.

GTDBU can be used as a buffer register of GTDVU, and GTDBD can be used as a buffer register of GTDVD. Buffer transfer is performed at the cycle end at an GTCNT overflow (during up-counting) or an underflow (during down-counting) or GTCNT counter clear for saw waves and at the trough for triangle waves.

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. The automatic dead time value setting to GTCCRB is performed at the next count clock cycle when registers that are used for calculating the automatic dead time value are updated.

The way to rewrite GTDVm is differed by GPT channel numbers.

[After]

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time values (GTDVU and GTDVD values) can automatically be set to GTCCRB. The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Dead time can be separately set for the first half and second half of a waveform. Dead time for the transition in the first half of a negative waveform is set in GTDVU and that in the second half is set in GTDVD. The same dead time can also be set for the first and second halves by setting GTDTCR.TDFER bit to 1.

GTDBU can be used as a buffer register of GTDVU, and GTDBD can be used as a buffer register of GTDVD. Buffer transfer is performed at the cycle end at an GTCNT overflow (during up-counting) or an underflow (during down-counting) or GTCNT counter clear for saw waves and at the trough for triangle waves.

The compare match value set by automatic dead time setting function can be confirmed by reading from GTCCRB. Writing to GTCCRB is prohibited when the automatic dead time setting function is used.

Dead time setting beyond the cycle is prohibited. When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 23.7. The adjusted value for the negative waveform is set for GTCCRB automatically. The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

In saw-wave one-shot pulse mode, when the adjusted value is beyond the cycle or the adjusted waveform toggle points are in disorder, the complementarity of the waveforms is not guaranteed.

In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCR = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 23.8.4.

When GTCCRA ≥ GTPR+GTDVm, GTPR-1 is set for GTCCRB as the upper limit value.

The automatic dead time value setting to GTCCRB is performed at the next count clock cycle when registers that are used for calculating the automatic dead time value are updated.

The way to rewrite GTDVm differs by GPT channel numbers.

Table 23.6 Compare match value after adjusting for dead time error

PWM output operating mode	Count direction	First half /second half	Condition of dead time error	Compare match value after adjusting	
				Positive waveform	Negative waveform
Saw-wave one-shot pulse mode	Up	First half	GTCCRA - GTDVU < 0	GTDVU	0
		Second half	GTCCRA + GTDVD > GTPR	GTPR-GTDVD	GTPR
	Down	First half	GTCCRA + GTDVU > GTPR	GTPR-GTDVU	GTPR
		Second half	GTCCRA - GTDVD < 0	GTDVD	0
Triangle-wave PWM mode 1/2/3	Up	(First half)	GTCCRA - GTDVU ≤ 0	GTDVU+1	1
	Down	(Second half)	GTCCRA - GTDVD < 0	GTDVD	0

10. 23.8.4.4 Restricted Specification of Output Protection Function

[Before]

The value of the GTCCRA register must be set within the range of (0 < GTCCRA < GTPR) at count start. If an incorrect value is set in the GTCCRA register during counting (a setting outside the range of 0 < GTCCRA < GTPR), the output protection function deactivates the level of one of the positive and negative outputs. The function does not operate correctly if counting starts with an incorrect value set in GTCCRA.

[After]

The value of the GTCCRA register must be set within the range of (0 < GTCCRA < GTPR) at count start. If an incorrect value is set in the GTCCRA register during counting (a setting outside the range of 0 < GTCCRA < GTPR), the output protection function deactivates the level of one of the positive and negative outputs. The function does not operate correctly if the following conditions are not satisfied:

- 0 < GTCCRA < GTPR when counting starts
- GTCCRA < GTPR + GTDVD - 1 during buffer transfer at crests
- When GTCCRA is greater than or equal to GTPR during buffer transfer at troughs, GTCCRA > GTDVU + 1.

11. 23.10.2 GTCCRn Settings during Compare Match Operation (n = A to F)

[Before]

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy the following conditions: GTDVU < GTCCRA, GTDVD < GTCCRA, and GTCCRA < GTPR.

When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made during count operation, the output protection function is activated.

You must set 0 < GTCCRA < GTPR at count start. Otherwise, the output protection function cannot be activated correctly. For details, see section 23.8.4, Output Protection Function for GTIOC Pin Output.

[After]

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy the following conditions: GTDVU < GTCCRA, GTDVD < GTCCRA, and GTCCRA < GTPR.

When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made during count operation, the output protection function is activated. However, the function does not operate correctly if the following conditions are not satisfied:

・0 < GTCCRA < GTPR when counting starts

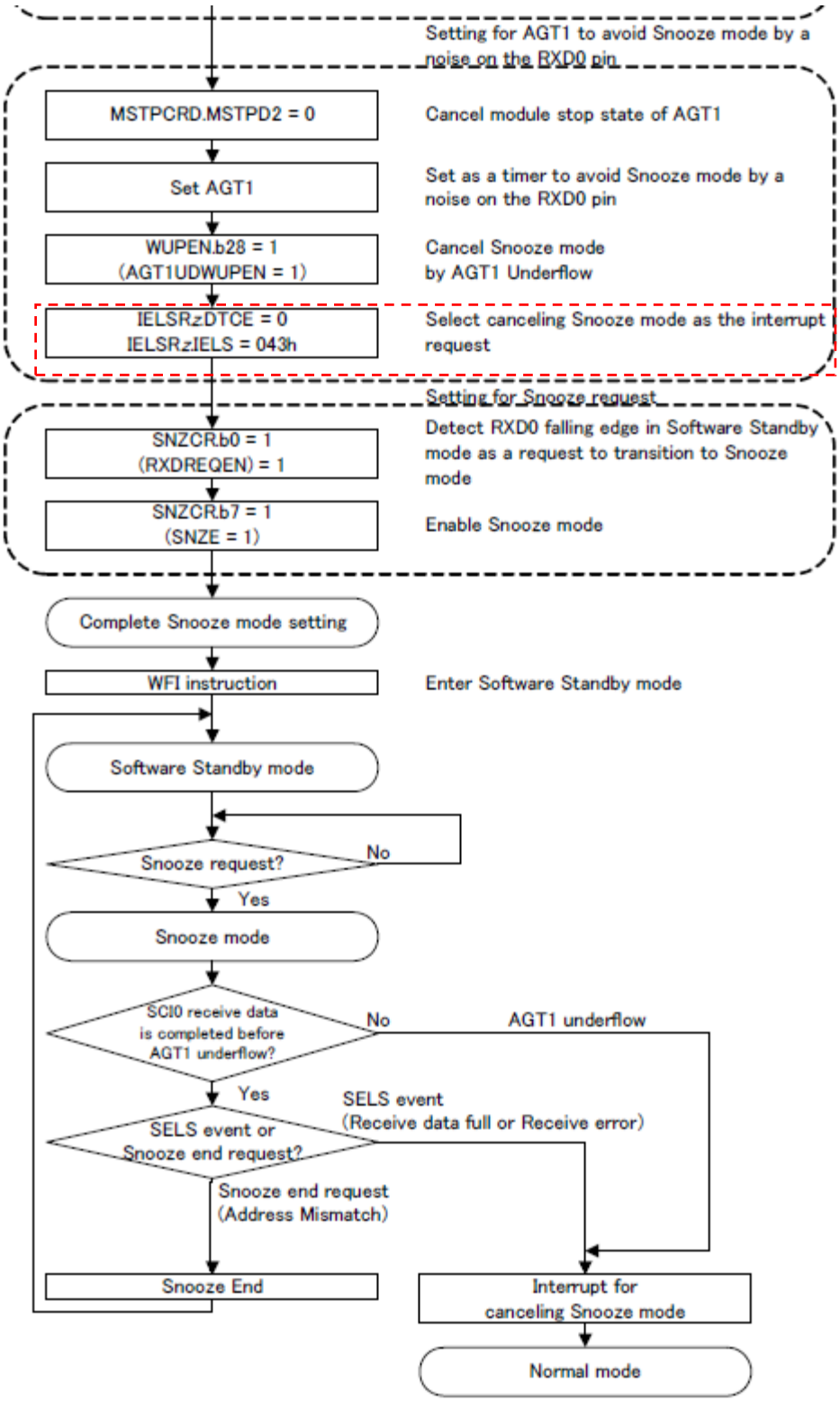
・GTCCRA < GTPR + GTDVD - 1 during buffer transfer at crests

・When GTCCRA is greater than or equal to GTPR during buffer transfer at troughs, GTCCRA > GTDVU + 1.

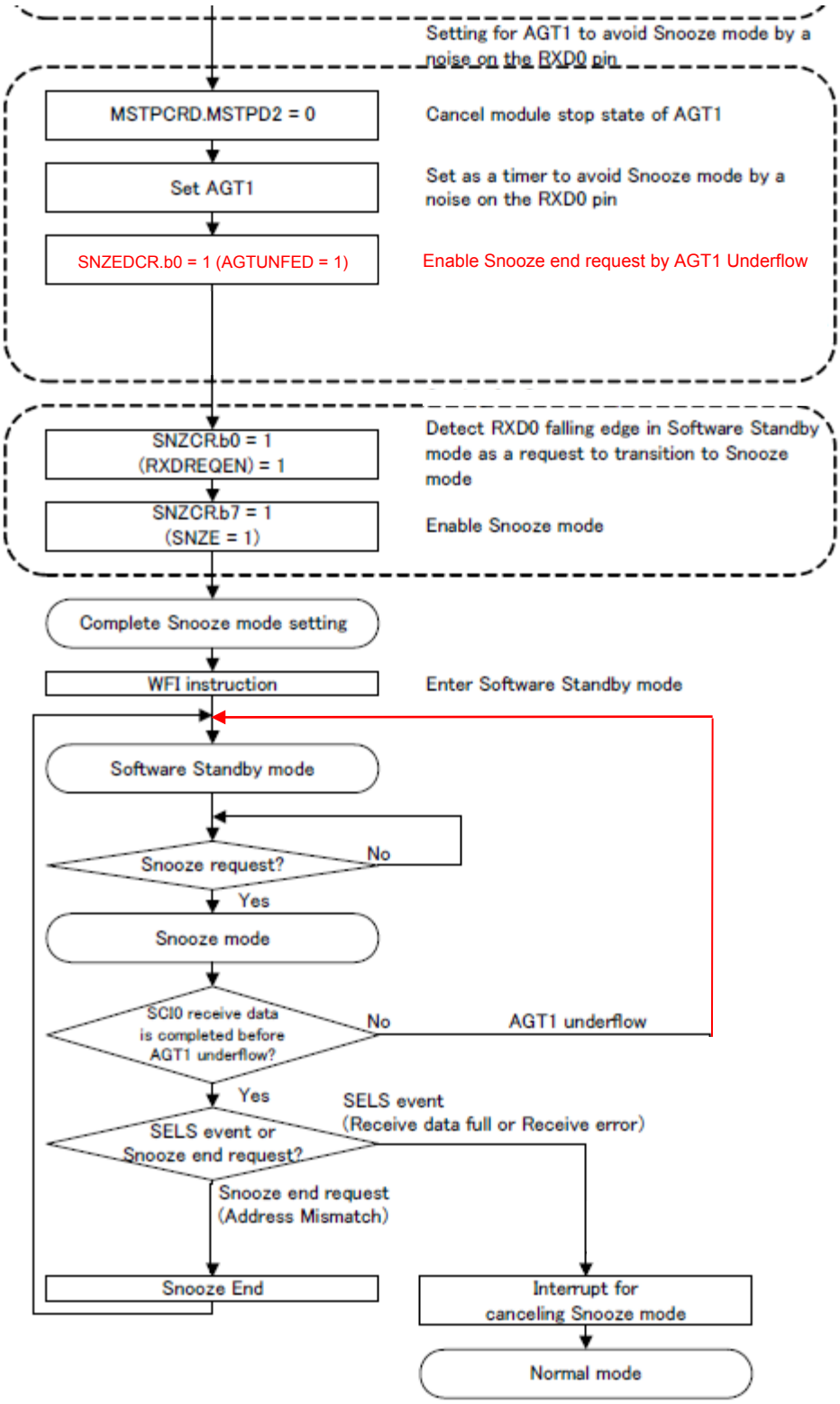
For details, see section 23.8.4, Output Protection Function for GTIOC Pin Output.

12. Figure 11.7 Setting example of using SCI0 in Snooze mode entry

[Before]



[After]


Setting for AGT1 to avoid Snooze mode by a noise on the RXD0 pin
MSTPCRD.MSTPD2 = 0
Cancel module stop state of AGT1
Set AGT1
Set as a timer to avoid Snooze mode by a noise on the RXD0 pin
SNZEDCR.b0 = 1 (AGTUNFED = 1)
Enable Snooze end request by AGT1 Underflow
SNZCR.b0 = 1 (RXDREQEN) = 1
Detect RXD0 falling edge in Software Standby mode as a request to transition to Snooze mode
SNZCR.b7 = 1 (SNZE = 1)
Enable Snooze mode
Complete Snooze mode setting
WFI instruction
Enter Software Standby mode
Software Standby mode
Snooze request?
No
Yes
Snooze mode
SCI0 receive data is completed before AGT1 underflow?
No
AGT1 underflow
Yes
SELS event or Snooze end request?
SELS event (Receive data full or Receive error)
Snooze end request (Address Mismatch)
Snooze End
Interrupt for canceling Snooze mode
Normal mode

13. Table 59.42 A/D internal reference voltage characteristics

[Before]

Item	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.20	1.25	1.30	V	-

[After]

Item	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.20	1.25	1.30	V	-
Sampling time	4.15	-	-	µs	-

14. 33.2.25 USB Address Register (USBADDR)

[Before]

Bit	Symbol	Bit name	Description	R/W
b10 to b8	STSRECOV0[2:0]	Status Recovery	・Recovery in device controller mode b10 b8 0 0 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 001b (Default state) 0 1 0: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 010b (Address state) 0 1 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 011b (Configured state) 1 0 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 011b), bits INTSTS0.DVSQ[2:0] = 001b (Default state) 1 1 0: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 011b), bits INTSTS0.DVSQ[2:0] = 010b (Address state) 1 1 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 011b), bits INTSTS0.DVSQ[2:0] = 011b (Configured state).	R/W

[After]

Bit	Symbol	Bit name	Description	R/W
b10 to b8	STSRECOV0[2:0]	Status Recovery	・Recovery in device controller mode b10 b8 0 0 1: Return to the full-speed connection and Default state 0 1 0: Return to the full-speed connection and Address state 0 1 1: Return to the full-speed connection and Configured state 1 0 0: Return to the suspend connection and Suspend state 1 0 1: Return to the high-speed connection and Default state 1 1 0: Return to the high-speed connection and Address state 1 1 1: Return to the high-speed connection and Configured state.	R/W

15. 15.3.21 Bus Error Address Register (BUSnERRADD) (n = 1 to 11)

[Before]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BERAD[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BERAD[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[After]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BERAD[31:16]															
Value after reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BERAD[15:0]															
Value after reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

16. 15.3.22 Bus Error Status Register (BUSnERRSTAT) (n = 1 to 11)

[Before]

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	-	-	-	-	-	-	ACCSTAT
Value after reset	0	0	0	0	0	0	0	0

[After]

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	-	-	-	-	-	-	ACCSTAT
Value after reset	0	0	0	0	0	0	0	x

17. 33.2.49 Deep Software Standby USB Transceiver Control/Pin Monitor Register (DPUSR0R)

[Before]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	DVBSTSHM	-	DOVCBHM	DOVCAHM	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[After]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	DVBSTSHM	-	DOVCBHM	DOVCAHM	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	x	0	x	x	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

18. 43.2.12 SD INFO1 Interrupt Mask Register (SD_INFO1_MASK)

[Before]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	SDD3INM	SDD3RMM	-	-	-	SDCDINM	SDCDRMM	ACENDM	-	RSPENDM
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

[After]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	SDD3INM	SDD3RMM	-	-	-	SDCDINM	SDCDRMM	ACENDM	-	RSPENDM
Value after reset	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1

19. 43.2.15 Transfer Data Length Register (SD_SIZE)

[Before]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	LEN[9:0]									
Value after reset	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

[After]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	LEN[9:0]									
Value after reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

20. 43.2.21 SDIO Interrupt Flag Register (SDIO_INFO1)

[Before]

Note 1. The flag value does not change even when set to 1. If 0 is written to this flag, it becomes 0.

[After]

Note 1. Only 0 can be written to clear the bit.

21. Table 13.1 Association between PRCR bits and registers to be protected

[Before]

PRCR bit	Registers to be protected
PRC1	• Registers related to the battery backup function: VBTBKRn (n = 0 to 511)

[After]

PRCR bit	Registers to be protected
PRC1	• Registers related to the battery backup function: VBTBKRn (n = 0 to 511), VBTICTLR

22. Table 19.1 ELC specifications

[Before]

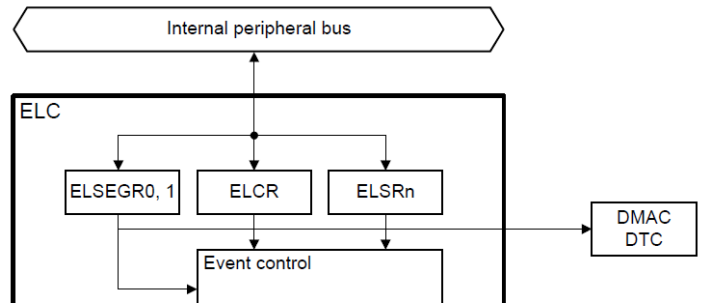
Parameter	Specifications
Event link function	270 types of event signals can be directly connected to modules. The ELC can generate an ELC event signal, and events that activate the DMAC and DTC.

[After]

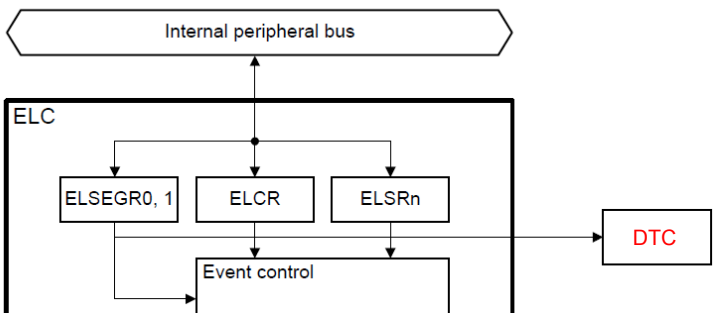
Parameter	Specifications
Event link function	270 types of event signals can be directly connected to modules. The ELC can generate an ELC event signal, and events that activate the DTC.

23. Figure 19.1 ELC block diagram (n = 0 to 18)

[Before]



[After]



24. 19.2.2 Event Link Software Event Generation Register n (ELSEGRn) (n = 0, 1)

[Before]

SEG bit (Software Event Generation)

A software event can trigger a linked DTC and DMAC event.

[After]

SEG bit (Software Event Generation)

A software event can trigger a linked DTC event.

25. Table 19.4 Module operations when event occurs

[Before]

Module	Operations when event occurs
DMAC/DTC	Start DMAC data transfer, and start DTC data transfer

[After]

Module	Operations when event occurs
DTC	Start DTC data transfer