Date: Sep. 12, 2017

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A029A/E	Rev.	1.00
Title	Revised information for current version of the User's Manuals		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S7G2, S5D9, S5D5, S3A7, S3A6, S3A3, S128, and S124 MCU Groups	Lot No. All lots	Reference Document	See below.		

This Technical Update describes corrections for published User's Manuals of Synergy Microcontrollers. You can search for the affected User's Manual by its document number shown in parenthesis ( ).

S7G2 Rev.1.20 (R01UM0001EU0120), S5D9 Rev.1.00 (R01UM0004EU0100),

S5D5 Rev.1.10 (R01UM0009EU0110), S3A7 Rev.1.20 (R01UM0002EU0120),

S3A6 Rev.1.00 (R01UM0007EU0100), S3A3 Rev.1.00 (R01UM0006EU0100),

S124 Rev.1.20 (R01UM0003EU0120), and S128 Rev.1.00 (R01UM0005EU0100)

[Changes summary]

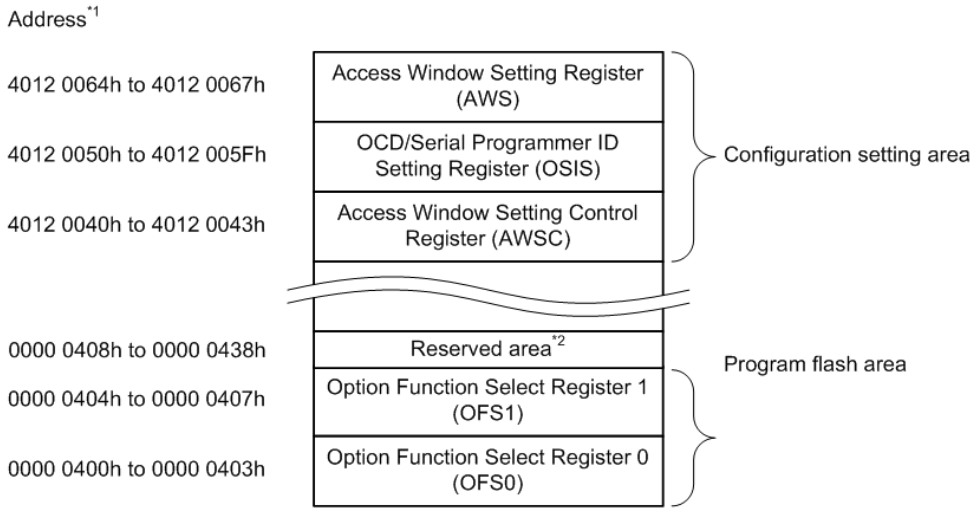
Chapter	Item	Description	S7G2	S5D9	S5D5	S3A7	S3A6	S3A3	S124	S128
Option-Setting Memory	1	Revised the reserved area	✓	-	-	-	-	-	-	-
I/O Ports	2	P402 and P404 are not 5 V-tolerant	✓	-	-	-	-	-	-	-
GPT	3	Revised description of UF, VF, WF bits in OPSCR register	✓	✓	-	✓	-	-	✓	-
	4	Revised description of EN bit in OPSCR register	✓	✓	✓	✓	✓	✓	✓	✓
	5	Revised explanation for Settings of GTCCRn in Usage Notes	✓	✓	✓	✓	✓	✓	✓	✓
AGT	6, 7	Revised the AGT block diagram and the explanation to update the value from the AGT Reload register to the counter	✓	✓	✓	✓	✓	✓	✓	✓
RTC	8	Added the TCEN bit to the RTCCRy register	✓	✓	✓	✓	✓	✓	-	-
USBFS	9, 10	Revised the example connections	-	-	-	✓	-	-	✓	-
ETHERC	11, 12	Revised description of MPR, MAHR, and MAFCR registers	✓	✓	-	-	-	-	-	-
SPI	13, 14	Added UDRF bit to description for error flag	✓	✓	-	✓	-	-	✓	-
DRW	15, 16, 17, 18	Corrected typographical errors	✓	✓	-	-	-	-	-	-
Electrical Characteristics	19	Revised recommended operating conditions of VCC and AVCC0	-	-	-	✓	✓	✓	✓	✓
	20	Added VBATWIOn I/O output characteristics	-	-	-	✓	-	-	-	-
	21	Added note about VREF condition for ACMPLP	-	-	-	-	✓	✓	-	-
	22	Revised VIH/L characteristics of RTCICn pin	✓	-	-	-	-	-	-	-
	23	Added note for 5 V-tolerant ports	✓	-	-	-	-	-	-	-
I/O Registers	24	Revised the number of access cycles	✓	-	-	-	-	-	-	-

Note:

The locations where corrections are made in the User's Manual can be in a paragraph, table, figure, sub-section, and section in a chapter. Depending on the product manuals that are affected, the chapter number can be different. For example, the SPI chapter of the S7G2 MCU User's Manual is chapter 38 but for the S124 MCU User's Manual, this is chapter 28. In the User's Manual, a section, table, or figure number is preceded by the chapter number. When a chapter, section, sub-section, table, or figure number is different, n is used to express them as explained in the following pages.

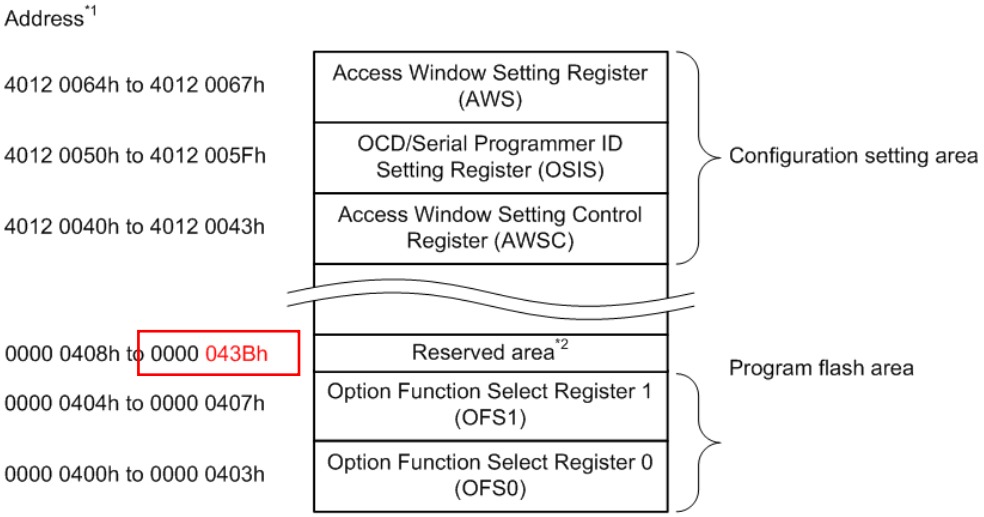
1. (S7G2) Option-Setting Memory, Figure 7.1 Option-setting memory area

[Before]



Note 1. The option-setting memory must be allocated to the flash user area.
Note 2. Do not access reserved area.

[After]



Note 1. The option-setting memory must be allocated to the flash user area.
Note 2. Do not access reserved area.

2. (S7G2) I/O Ports, Table 20.2 I/O port functions

[Before]

Port	Port name	Input pull-up	Open-drain output	Drive capacity switching	5-V tolerant
Port 4	P400, P401	✓	✓	Middle	✓
	P402 to P404	✓	✓	Low, middle	✓
	P405 to P406	✓	✓	Low, middle, high	-
	P407	✓	✓	Low, middle, high	✓
	P408 to P415	✓	✓	Low, middle, high	✓

[After]

Port	Port name	Input pull-up	Open-drain output	Drive capacity switching	5-V tolerant
Port 4	P400, P401	✓	✓	Middle	✓
	P402 to P404	✓	✓	Low, middle	-
	P405 to P406	✓	✓	Low, middle, high	-
	P407	✓	✓	Low, middle, high	✓
	P408 to P415	✓	✓	Low, middle, high	✓

3. (S7G2, S5D9, S3A7, S124) General PWM Timer (GPT), n.2.32 Output Phase Switching Control Register (OPSCR)

[Before]

UF, VF, WF bits (Input Phase Soft Setting)

The UF, VF, and WF bits set the input phase from the software settings. When OPSCR.FB bit = 0, these bits are valid.

[After]

UF, VF, WF bits (Input Phase Soft Setting)

The UF, VF, and WF bits set the input phase from the software settings. When OPSCR.FB bit = 1, these bits are valid.

4. (All Series) General PWM Timer (GPT), n.2.32 Output Phase Switching Control Register (OPSCR)

[Before]

EN bit (Enable-Phase Output Control)

When OPSCR.EN bit = 0, first set OPSCR.FB, OPSCR.UF/VF/WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.ALIGN, OPSCR.NFCS, OPSCR.GRP, OPSCR.GODF, OPSCR.NFEN, OPSCR.NFCS. Then, set his bit to 1.

[After]

EN bit (Enable-Phase Output Control)

When OPSCR.EN bit = 0, first set OPSCR.FB, OPSCR.UF/VF/WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.RV, OPSCR.ALIGN, OPSCR.GRP, OPSCR.GODF, OPSCR.NFEN, OPSCR.NFCS. Then, set his bit to 1.

5. (All Series) General PWM Timer (GPT), n.10.2 GTCCRn Settings during Compare Match Operation (n = A to F), (2) When automatic dead time setting is not made in triangle-wave PWM mode

[Before]

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA ≥ GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRA ≥ GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

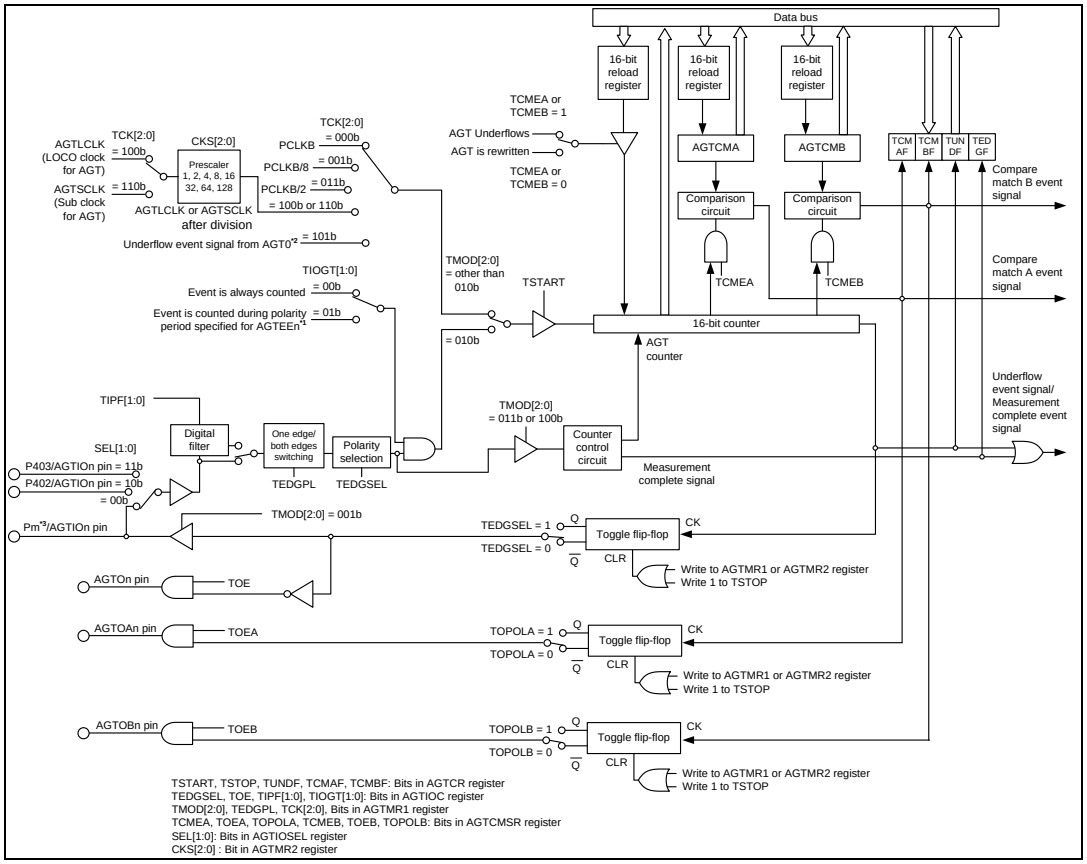
[After]

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

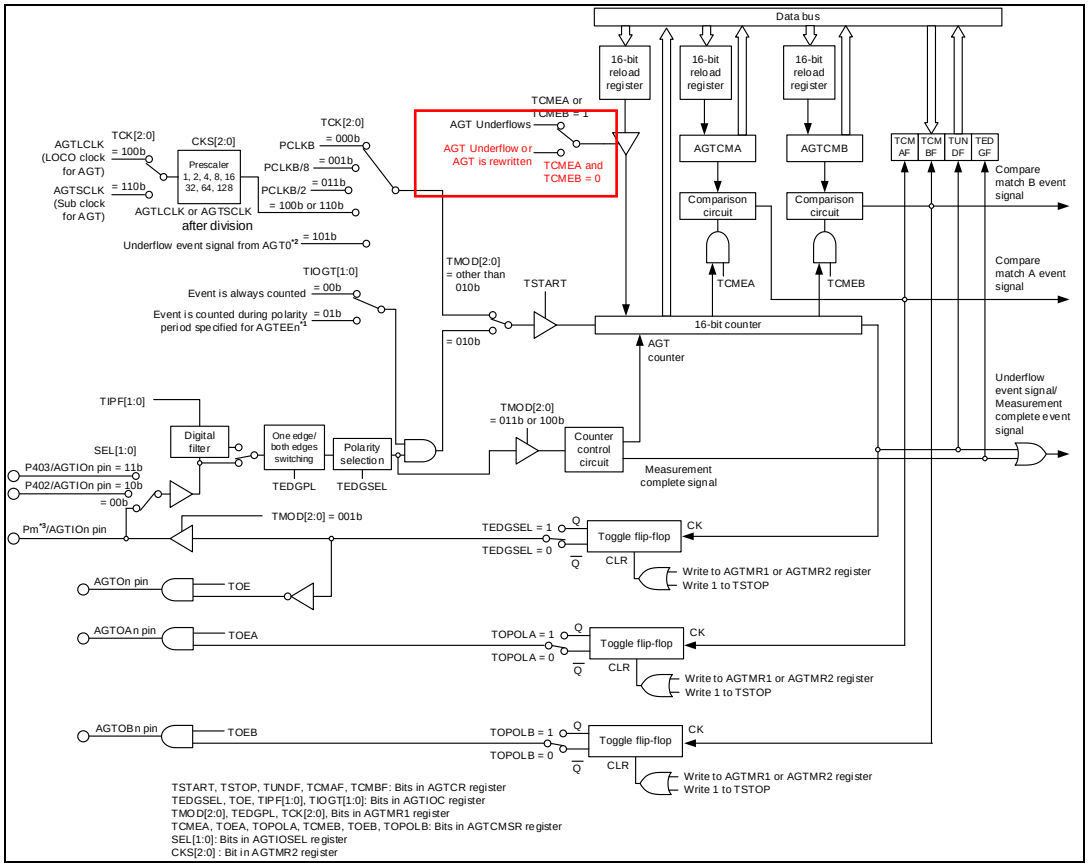
Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

6. (All Series) Asynchronous General-Purpose Timer (AGT), Figure n.1 AGT block diagram

[Before]



[After]



7. (All Series) Asynchronous General-Purpose Timer (AGT), n.3.1 Reload Register and Counter Rewrite Operation

[Before]

When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA bit or TCMEB bit is 0 (compare match A/B register is invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source.

[After]

When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA bit and TCMEB bit is 0 (compare match A/B register is invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source.

8. (S7G2, S5D9, S5D5, S3A7, S3A6, S3A3) Realtime Clock (RTC), n.2.22 Time Capture Control Register y (RTCCRy) (y = 0 to 2)

[Before]

Bit	Symbol	Bit name	Description	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

[After]

Bit	Symbol	Bit name	Description	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	TCEN	Time Capture Event Input Pin Enable	0: The time capture event input pin RTCICn is disabled 1: The time capture event input pin RTCICn is enabled. (n = 0 to 2)	R/W

TECN bit (Time Capture Event Input Pin Enable)

This bit enables or disables the time capture event input pins (RTCIC0, RTCIC1, and RTCIC2). When the functions of the time capture event input pins (RTCIC0, RTCIC1, and RTCIC2) are multiplexed, VBTICTLR should be set first. If the TCEN bit is set to 0, also set the TCCT[1:0] bits to 00b.

9. (S3A7, S124) USB 2.0 Full-Speed Module (USBFS), Figure n.5 Example OTG connection in self-powered state to Figure n.9 Example of functional connection with Battery Charging Rev.1.2 supported

[Before]

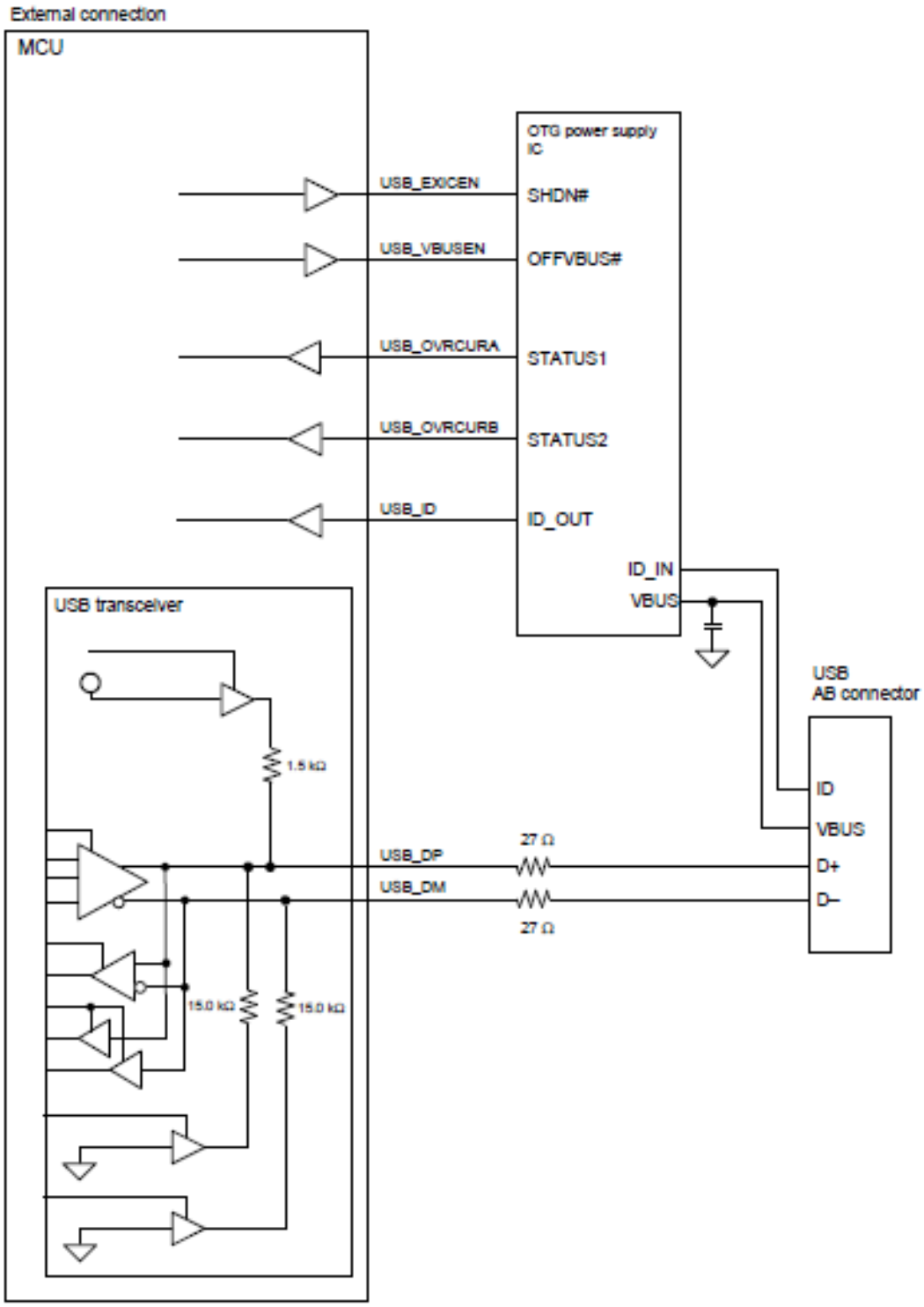


Figure n.5 Example OTG connection in self-powered state

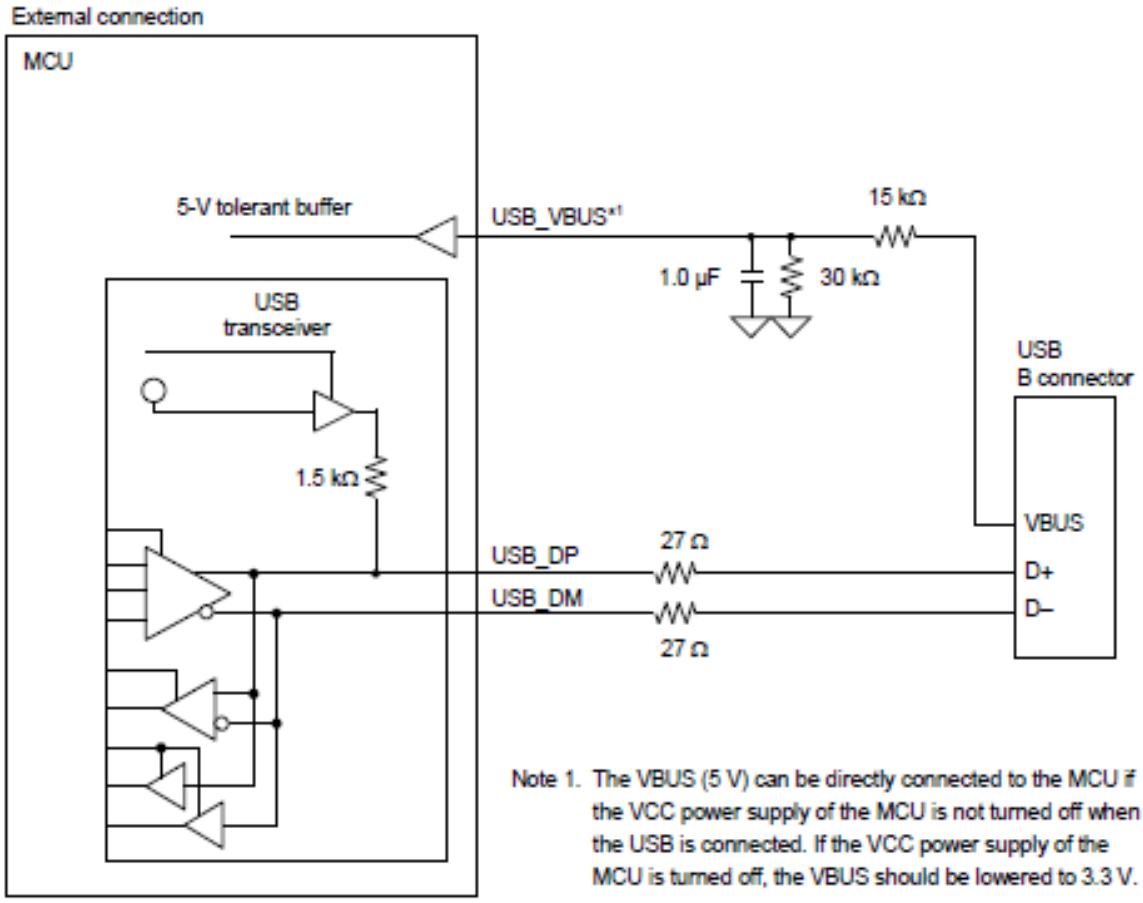


Figure n.6 Example device connection in self-powered state

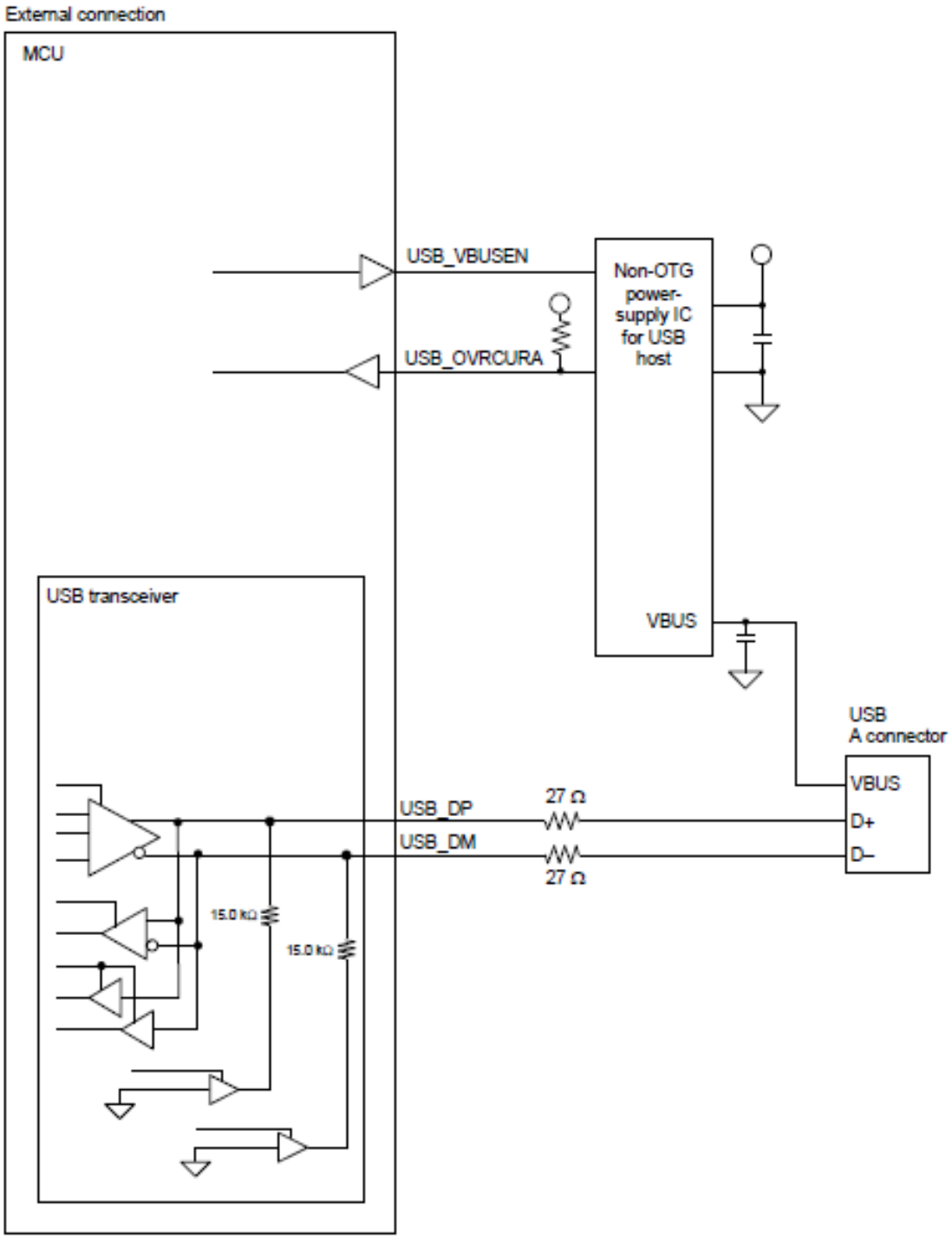


Figure n.7 Example host connection

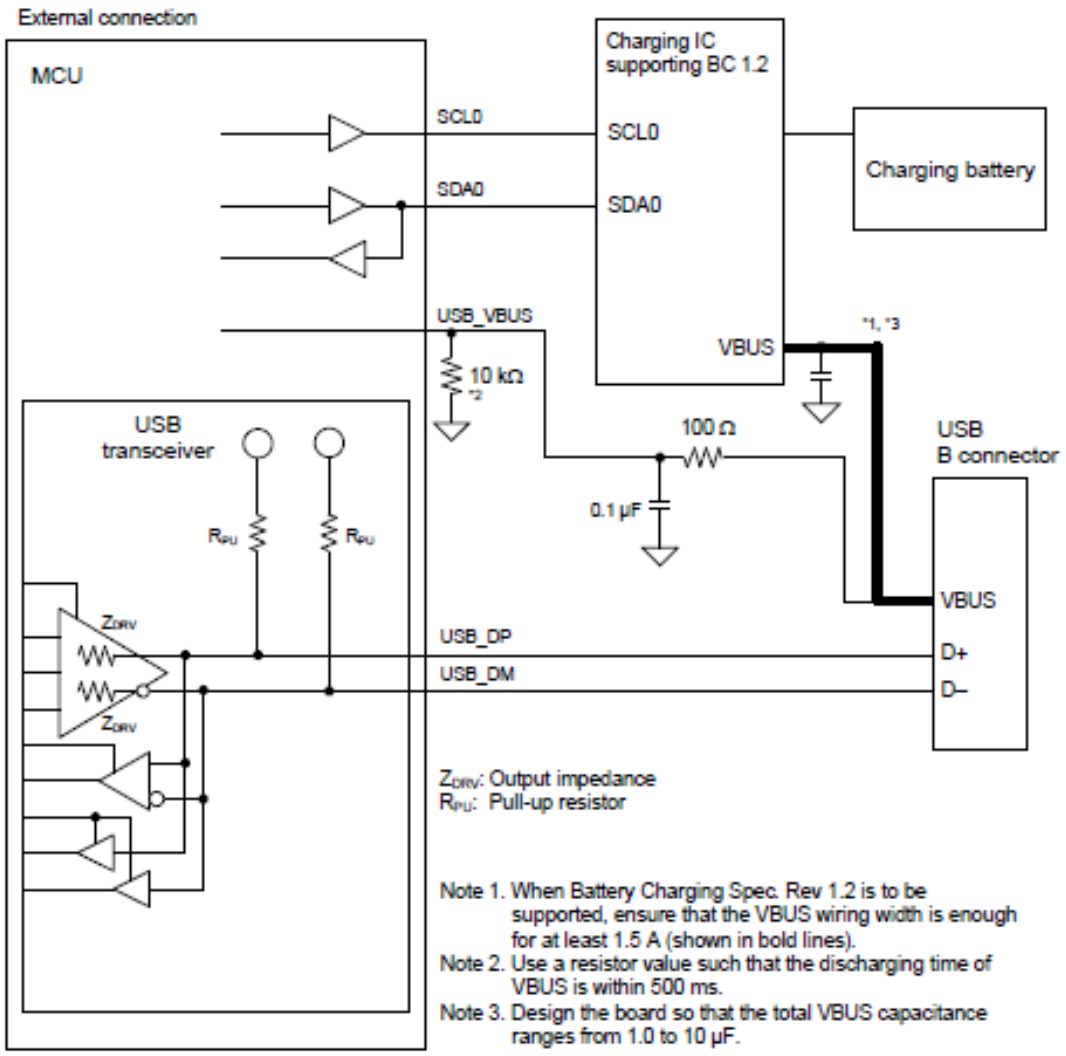


Figure n.9 Example of functional connection with Battery Charging Rev.1.2 supported

[After]

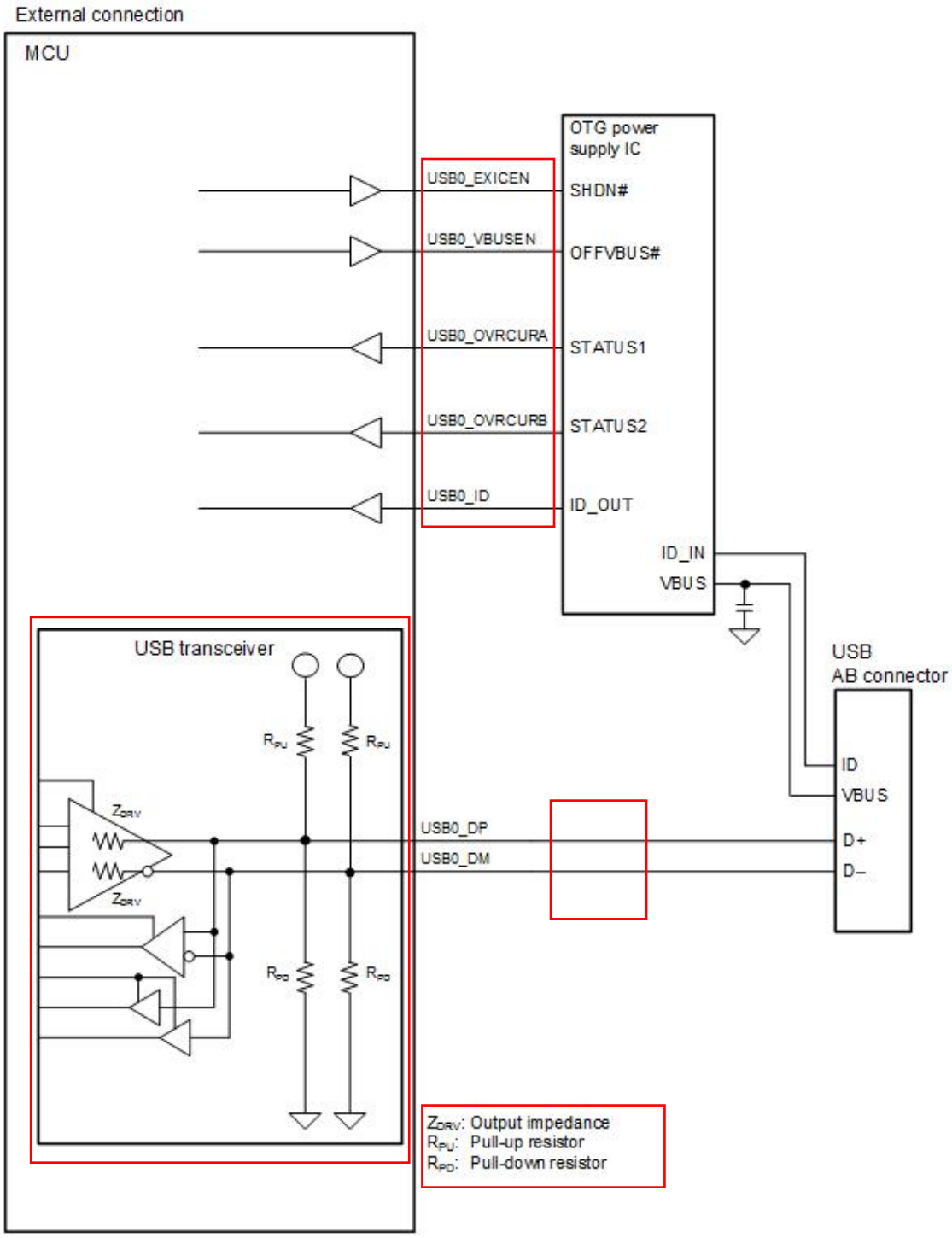


Figure n.5 Example OTG connection in self-powered state

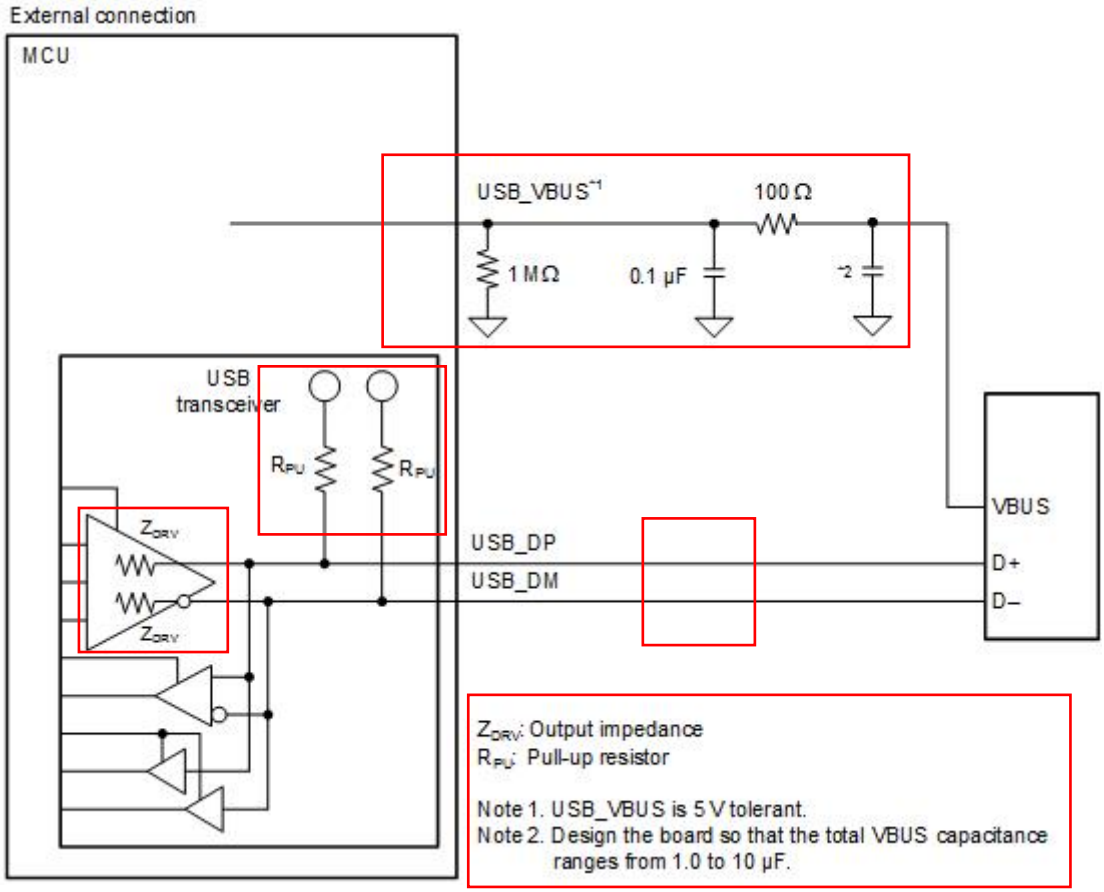


Figure n.6 Example device connection in self-powered state

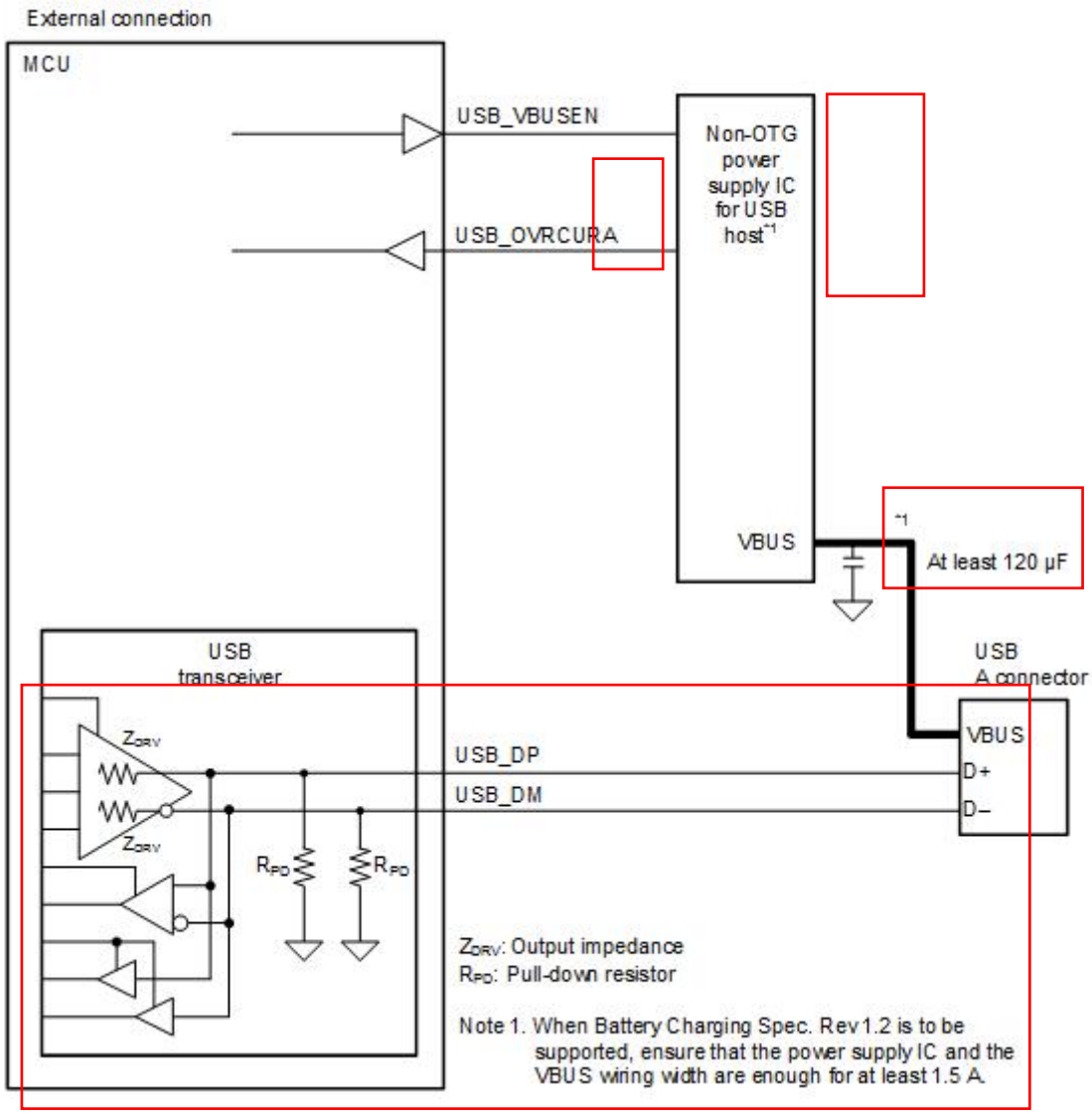


Figure n.7 Example host connection

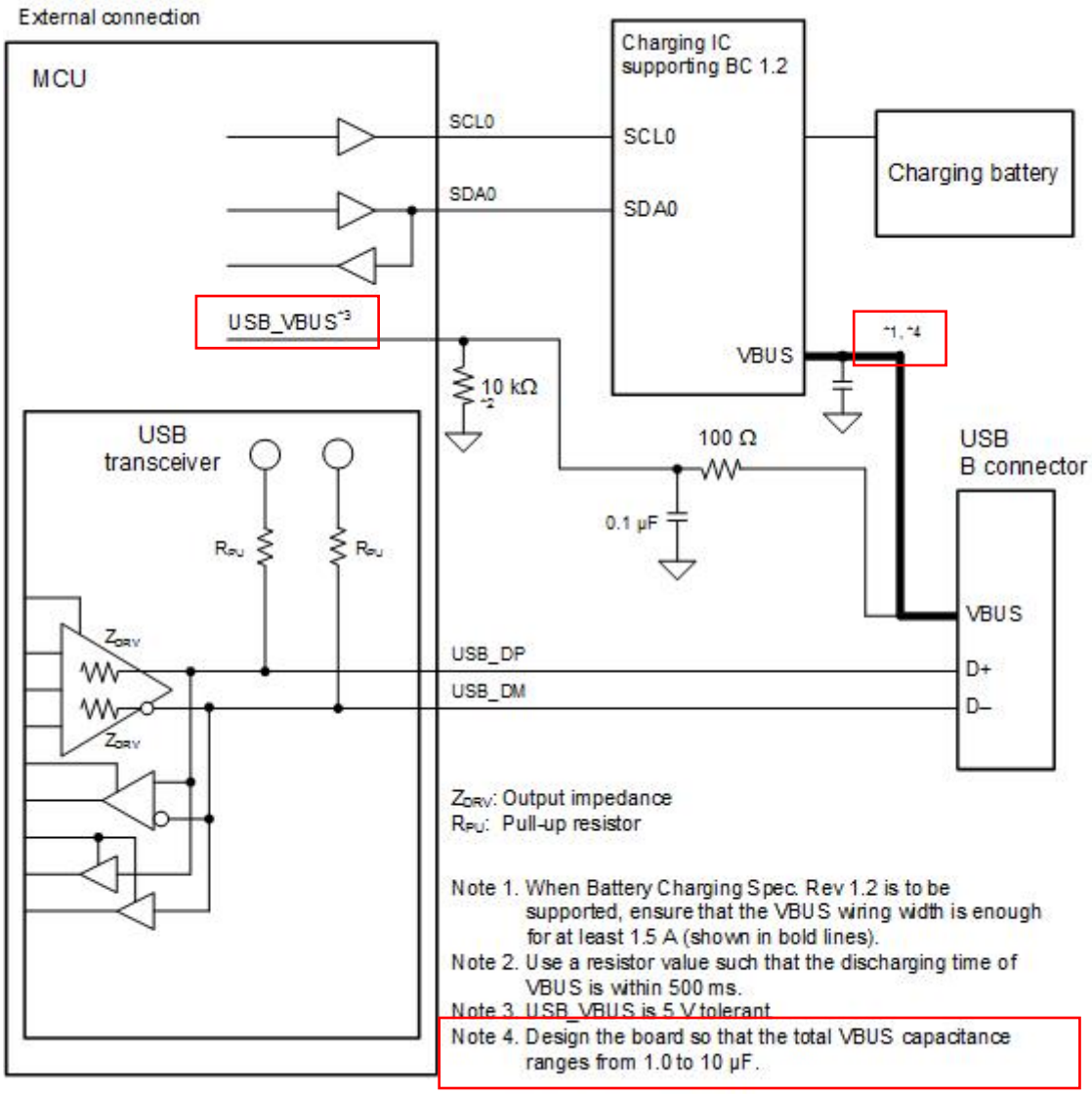


Figure n.10 Example of functional connection with Battery Charging Rev.1.2 supported

10. (S3A7, S124) USB 2.0 Full-Speed Module (USBFS), Figure n.8 Example device connection in bus-powered state

[Before]

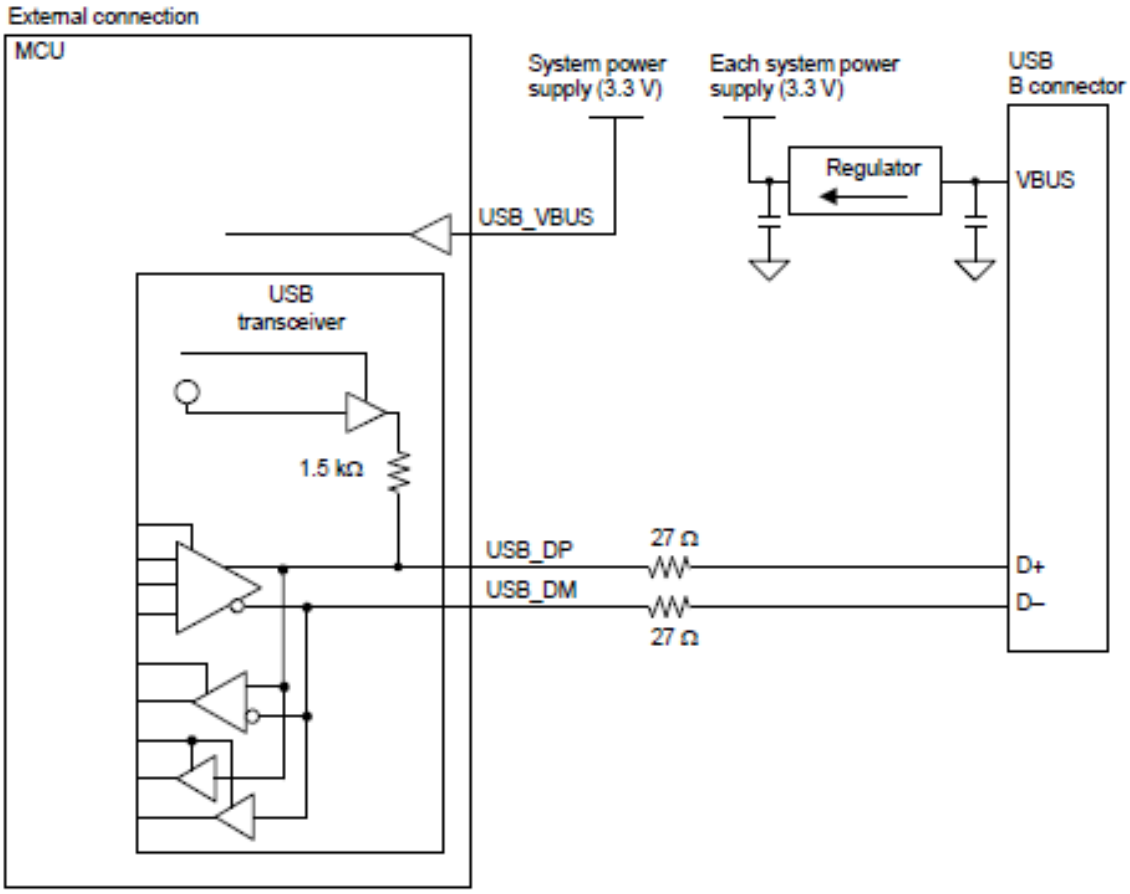


Figure n.8 Example device connection in bus-powered state

[After]

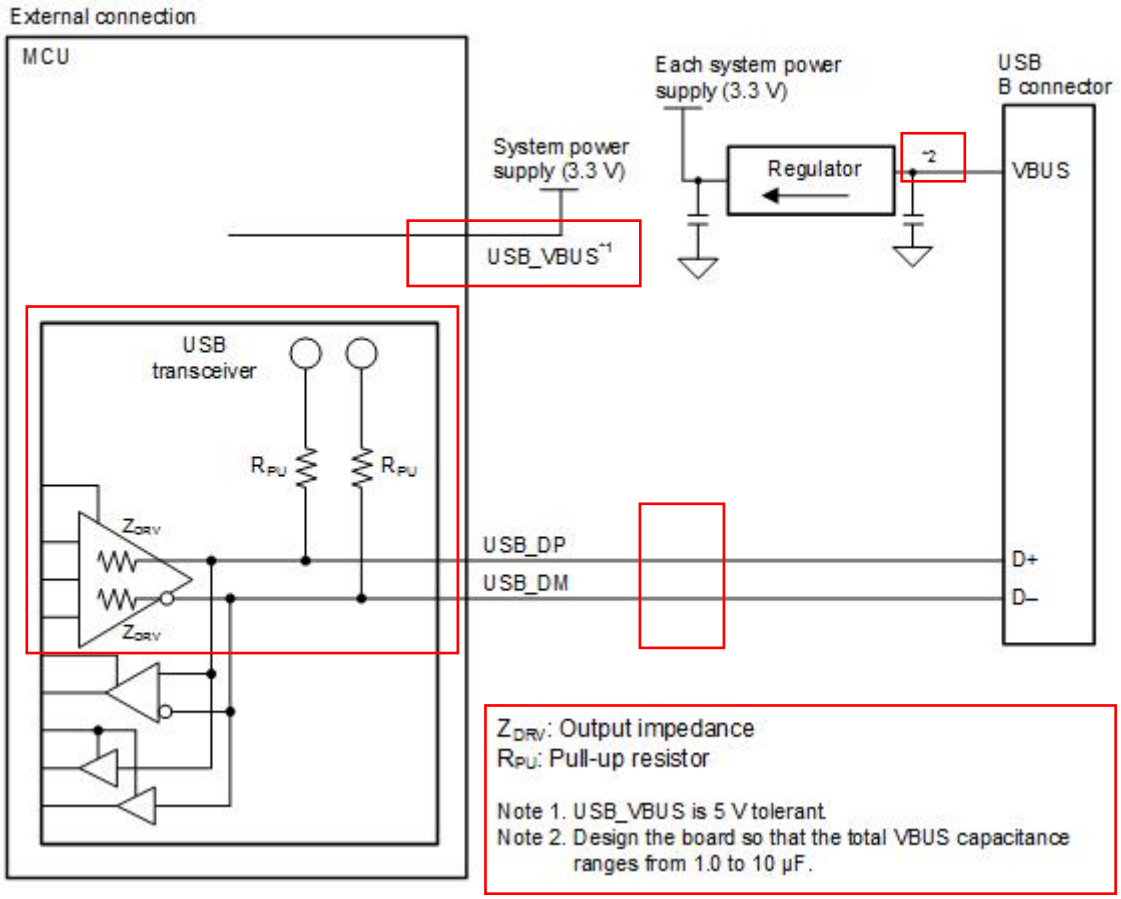


Figure n.8 Example device connection in bus-powered state 1

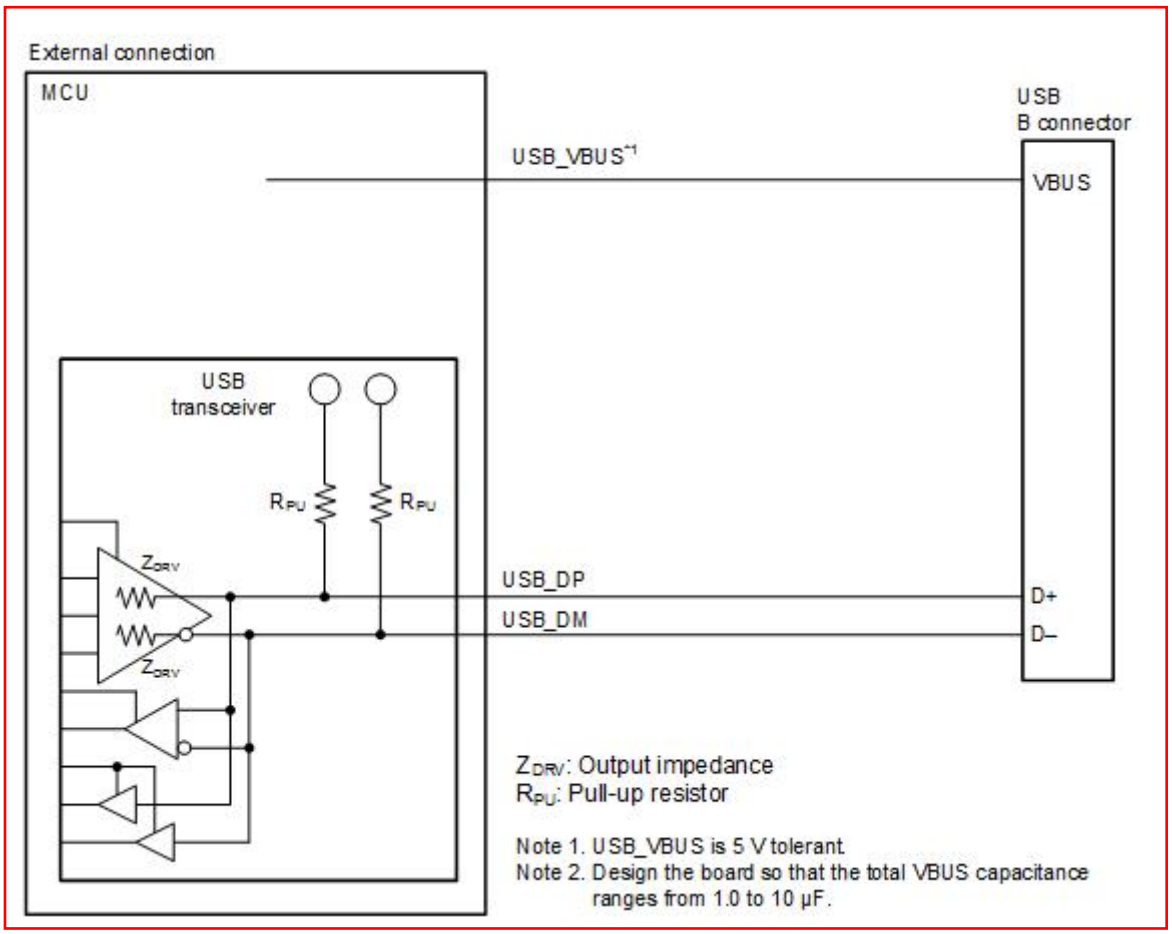


Figure n.9 Example device connection in bus-powered state 2

11. (S7G2, S5D9) Ethernet MAC Controller (ETHERC), n.2.10 Manual PAUSE Frame Register (MPR)

[Before]

Address(es): ETHERC0.MPR 4006 4158h, ETHERC11.MPR 4006 4358h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MP[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[After]

Address(es): ETHERC0.MPR 4006 4158h, ETHERC11.MPR 4006 4358h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MP[15:0]															
Value after reset:	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

12. (S7G2, S5D9) Ethernet MAC Controller (ETHERC), n.2.26 Multicast Address Frame Receive Counter Register (MAFCR)

[Before]

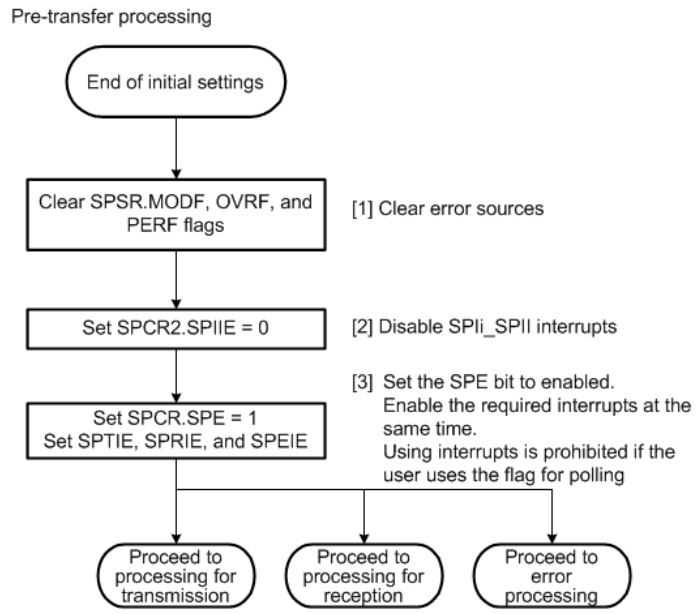
The MAFCR register is a counter that indicates the number of times a frame with the multicast address set was received. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the RFCR register clears the counter value to 0.

[After]

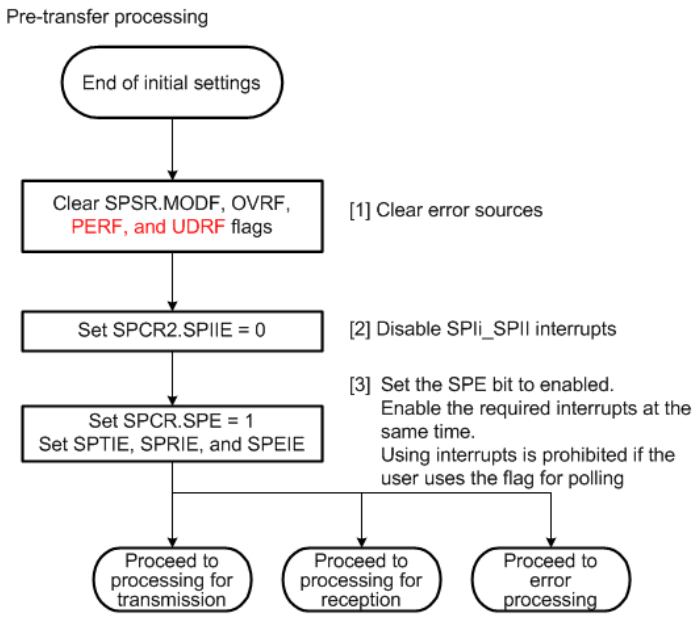
The MAFCR register is a counter that indicates the number of times a frame with the multicast address set was received. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the MAFCR register clears the counter value to 0.

13. (S7G2, S5D9, S3A7, S124) Serial Peripheral Interface (SPI), Figure n.37 Transmission flow in master mode transmission to Figure n.39 Error processing flow for master mode

[Before]



[After]



14. (S7G2, S5D9, S3A7, S124) Serial Peripheral Interface (SPI), Table n.13 SPI interrupt sources

[Before]

Interrupt source	Symbol	Interrupt condition	DMAC or DTC activation
SPI error (mode fault, underrun, overrun, or parity error)	SPIi_SPEI	SPSR.MODF, OVRF, or PERF flag is set to 1 while the SPCR.SPEIE bit is 1	Invalid

[After]

Interrupt source	Symbol	Interrupt condition	DMAC or DTC activation
SPI error (mode fault, underrun, overrun, or parity error)	SPIi_SPEI	SPSR.MODF, OVRF, PERF, or UDRF flag is set to 1 while the SPCR.SPEIE bit is 1	Invalid

15. (S7G2, S5D9) 2D Drawing Engine (DRW), n.2.2 Surface Control Register (CONTROL2)

[Before]

Bit	Symbol	Bit name	Description	R/W
b23, b22	WRITE ALPHA[1:0]	Writeback Alpha Source for Framebuffer	• In non-alpha channel blending mode (USEACB = 0): Sets the alpha source for the framebuffer. b23 b22 0 0: Use alpha from color 2 0 1: Use source alpha (pixel coverage) 1 0: Use 0.0 as alpha 1 1: Use alpha from framebuffer. • In alpha channel blending mode (USEACB = 1): Blends alpha in color 2 instead of framebuffer alpha. 00_B: BC2A = 1: Use alpha from framebuffer as destination (DST_A) else: BC2A = 0: Use alpha in color 2 as destination (DST_A).	W

[After]

Bit	Symbol	Bit name	Description	R/W
b23, b22	WRITE ALPHA[1:0]	Writeback Alpha Source for Framebuffer	• In non-alpha channel blending mode (USEACB = 0): Sets the alpha source for the framebuffer. b23 b22 0 0: Use alpha from color 2 0 1: Use source alpha (pixel coverage) 1 0: Use 0.0 as alpha 1 1: Use alpha from framebuffer. • In alpha channel blending mode (USEACB = 1): Blends alpha in color 2 instead of framebuffer alpha. 00b: BC2A = 1: Use alpha in color 2 as destination (DST_A) else: BC2A = 0: Use alpha from framebuffer as destination (DST_A).	W

16. (S7G2, S5D9) 2D Drawing Engine (DRW), n.2.6 Hardware Version and Feature Set ID Register (HWREVISION)

[Before]

Bit	Symbol	Bit name	Description	R/W
b21	TEXCLUT	Texture CLUT with 16 or 256 Entries Available	Texture CLUT with 16 or 256 entries is available.	R
b22	—	Reserved	This bit is read as 0.	R
b23	RLEUNIT	RLE Unit Available	RLE unit is available.	R
b24	TEX CLUT256	Texture CLUT Available	Texture CLUT is available.	R

[After]

Bit	Symbol	Bit name	Description	R/W
b21	TEXCLUT	Texture CLUT Available	Texture CLUT is available.	R
b22	—	Reserved	This bit is read as 0.	R
b23	RLEUNIT	RLE Unit Available	RLE unit is available.	R
b24	TEX CLUT256	Texture CLUT with 16 or 256 Entries Available	Texture CLUT with 16 or 256 entries is available.	R

17. (S7G2, S5D9) 2D Drawing Engine (DRW), n.3.1.1 Color Formats

[Before]

Supported color formats are:

Framebuffer formats

• 8-bit: a (8)

• 16-bit: RGB (565), aRGB (4444), aRGB (1555)

• 32-bit: aRGB (8888).

[After]

Supported color formats are:

Framebuffer formats

• 8-bit: a (8)

• 16-bit: RGB (565), aRGB (4444)

• 32-bit: aRGB (8888).

18. (S7G2, S5D9) 2D Drawing Engine (DRW), n.6.2.6 Rasterization Optimization, (1) Spanstore

[Before]

In this case, spanstore cannot be activated in the top left corner but can be activated in the bottom left corner. The empty corners in the top right and the bottom left cannot be rasterized because of the spanabort optimization.

[After]

In this case, spanstore cannot be activated in the top left corner but can be activated in the bottom left corner. The empty corners in the top right and the bottom right cannot be rasterized because of the spanabort optimization.

19. (S3A7, S3A6, S3A3, S124, S128) Electrical Characteristics, Table n.2 Recommended operating conditions

(S3A7, S3A3, S124, S128)

[Before]

Note 1. Use AVCC0 and VCC under the following conditions:

AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V

AVCC0 = VCC when VCC < 2.0 V

[After]

Note 1. Use AVCC0 and VCC under the following conditions:

AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.2 V and AVCC0 ≥ 2.2 V

AVCC0 = VCC when VCC < 2.2 V or AVCC0 < 2.2 V

(S3A6)

[Before]

Note 1. Use AVCC0 and VCC under the following conditions:

AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.2 V and AVCC0 ≥ 2.2 V

AVCC0 = VCC when VCC < 2.2 V or AVCC < 2.2 V

[After]

Note 1. Use AVCC0 and VCC under the following conditions:

AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.2 V and AVCC0 ≥ 2.2 V

AVCC0 = VCC when VCC < 2.2 V or AVCC0 < 2.2 V

20. (S3A7) Electrical Characteristics, 51.10 Battery Backup Function Characteristics

[Before]

No description in Electrical Characteristics

[After]

Table n.xx VBATT-I/O characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
VBATWIOn I/O output characteristics (n = 0 to 2)	VCC > $V_{DETBATT}$	VCC = 4.0 to 5.5 V	V_{OH}	VCC – 0.8	–	–	V	I_{OH} = -200µA
			V_{OL}	–	–	0.8		I_{OL} = 200µA
		VCC = 2.7 to 4.0 V	V_{OH}	VCC – 0.5	–	–		I_{OH} = -100µA
			V_{OL}	–	–	0.5		I_{OL} = 100µA
		VCC = $V_{DETBATT}$ to 2.7 V	V_{OH}	VCC – 0.3	–	–		I_{OH} = -50µA
			V_{OL}	–	–	0.3		I_{OL} = 50µA
	VCC < $V_{DETBATT}$	VBATT = 2.7 to 3.6 V	V_{OH}	V_{BATT} – 0.5	–	–		I_{OH} = -100µA
			V_{OL}	–	–	0.5		I_{OL} = 100µA
		VBATT = 1.6 to 2.7 V	V_{OH}	V_{BATT} – 0.3	–	–		I_{OH} = -50µA
			V_{OL}	–	–	0.3		I_{OL} = 50µA

21. (S3A6, S3A3) Electrical Characteristics, Table n.73 ACMPLP characteristics

(S3A6)

[Before]

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	Standard mode		VREF	0	-	VCC–1.4	V	-
	Window mode	CMPREF1	VREFH	1.4	-	VCC	V	-
		CMPREF0	VREFL	0	-	VCC–1.4	V	-

Note: When 8-bit DAC output is used as the reference voltage, the offset voltage increases up to 2.5 x VCC/256.
Note: In window mode, be sure to satisfy the following condition: VREFH - VREFL ≥ 0.2 V.

[After]

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	Standard mode	IVREFn (n = 0, 1)	VREF	0	-	VCC–1.4	V	-
	Window mode	IVREF1	VREFH	1.4	-	VCC	V	-
		IVREF0	VREFL	0	-	VCC–1.4	V	-

Note: When 8-bit DAC output is used as the reference voltage, the offset voltage increases up to 2.5 x VCC/256.
Note: In window mode, be sure to satisfy the following condition: IVREF1 - IVREF0 ≥ 0.2 V.

(S3A3)

[Before]

Item			Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	Standard mode		VREF	0	-	VCC–1.4	V	-
	Window mode	CMPREF1	VREFH	1.4	-	VCC	V	-
		CMPREF0	VREFL	0	-	VCC–1.4	V	-

Note: When 8-bit DAC output is used as the reference voltage, the offset voltage increases up to 2.5 x VCC/256.
Note: In window mode, you must satisfy the following condition: Vref1 - Vref0 ≥ 0.2 V.

[After]

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	Standard mode	IVREFn (n = 0, 1)	VREF	0	-	VCC–1.4	V	-
	Window mode	IVREF1	VREFH	1.4	-	VCC	V	-
		IVREF0	VREFL	0	-	VCC–1.4	V	-

Note: When 8-bit DAC output is used as the reference voltage, the offset voltage increases up to 2.5 x VCC/256.
Note: In window mode, be sure to satisfy the following condition: IVREF1 - IVREF0 ≥ 0.2 V.

22. (S7G2) Electrical Characteristics, Table 59.4 I/O V_{IH}, I_{IL}

[Before]

Item			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	RTCIC0, RTCIC1, RTCIC2 (When V_{BATT} power supply is selected)	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3	V
			V_{IL}	–0.3	-	V_{BATT} × 0.2	
			ΔV_T	V_{BATT} × 0.05	-	-	

[After]

Item					Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	RTCIC0, RTCIC1, RTCIC2	When using the Battery Backup Function	When VBATT power supply is selected	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3	V
					V_{IL}	-	-	V_{BATT} × 0.2	
					ΔV_T	V_{BATT} × 0.05	-	-	
				When VCC power supply is selected	V_{IH}	VCC × 0.8	-	Higher voltage either VCC + 0.3 V or V_{BATT} + 0.3 V	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
			When not using the Battery Backup Function		V_{IH}	VCC × 0.8	-	VCC + 0.3	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	

23. (S7G2) Electrical Characteristics, Table 59.4 I/O V_{IH}, I_{IL}

[Before]

Item			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	5V-tolerant ports*3	V_{IH}	VCC × 0.8	-	VCC + 3.5 (max 5.8)	V
			V_{IL}	–0.3	-	VCC × 0.2	
			ΔV_T	VCC × 0.05	-	-	
	Ports	5V-tolerant ports*5	V_{IH}	VCC × 0.8	-	VCC + 3.5 (max 5.8)	
			V_{IL}	–0.3	-	VCC × 0.2	

Note 1. SCL0_B, SCL1_B, SDA1_B (total 3 pins).
Note 2. SCL0_A, SDA0_A, SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 7 pins).
Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 23 pins).
Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 22pins).
Note 6. All input pins except for the ports already described in the table.

[After]

Item			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	5V-tolerant ports*3*7	V_{IH}	VCC × 0.8	-	VCC + 3.5 (max 5.8)	V
			V_{IL}	–0.3	-	VCC × 0.2	
			ΔV_T	VCC × 0.05	-	-	
	Ports	5V-tolerant ports*5*7	V_{IH}	VCC × 0.8	-	VCC + 3.5 (max 5.8)	
			V_{IL}	–0.3	-	VCC × 0.2	

Note 1. SCL0_B, SCL1_B, SDA1_B (total 3 pins).
Note 2. SCL0_A, SDA0_A, SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 7 pins).
Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 23 pins).
Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 22 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V. Otherwise, a breakdown might occur because the 5 V-tolerant ports are electrically controlled to not violate the breakdown voltage.

24. (S7G2) Appendix I/O Registers, Table 3.2 Access cycles for non-GPT modules

[Before]

Table 3.2 Access cycles for non-GPT modules (1 of 3)

Address		Peripherals	Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
From	To		Read	Write	Read	Write		
4000 0000h	4001 CFFFh	MMPU, SMPU, SPMON, MMF, SRAM, BUS, DMACn, DMA, DTC, ICU, DBG, FCACHE	6				ICLK	Memory Protection Unit, Memory Mirror Function, SRAM, Buses, DMA Controller, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
4001 E000h	4001 E3FFh	SYSTEM	7				ICLK	Operation Modes, Resets, Clock Generation Function, Register Write Protection Function
4001 E400h	4001 E6FFh	SYSTEM	11		6 ~ 9		PCLKB	Low Power Mode, Resets, Low Voltage Detect, Battery Backup Function
4004 0000h	4004 7FFFh	PORTn, PFS, PMISC, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	5		1 ~ 4		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Realtime Clock, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control

Table 3.2 Access cycles for non-GPT modules (2 of 3)

Address		Peripherals	Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
From	To		Read	Write	Read	Write		
4004 8000h	4004 DFEFh	SRCRAM	6	5	2 ~ 5	1 ~ 4	PCLKB	Sampling Rate Converter
4004 DFF0h	4004 DFF7h	SRC	7		3 ~ 6		PCLKB	
4004 DFF8h	4004 DFFFh	SRC	5		1 ~ 4		PCLKB	
4004 E000h	4005 FFFFh	SSIn, CANn, IICn, DOC, ADC12n, TSN, DAC12, AMI	5		1 ~ 4		PCLKB	Serial Sound Interface, Controller Area Network Module, I2C Bus Interface, Data Operation Circuit, 12-Bit A/D Converter, Temperature Sensor, 12-Bit D/A Converter
4006 0000h	4006 0FFFh	USBHS	(5+BWAIT)*2		(1+BWAIT) ~ (4+BWAIT)*2		PCLKA	USB 2.0 High-Speed Module
4006 2000h	4006 2FFFh	SDHIn	5		1 ~ 4		PCLKA	SD/MMC Host Interface
4006 4000h	4006 40FFh	EDMAC0	6		2 ~ 5		PCLKA	Ethernet DMA Controller
4006 4100h	4006 41FFh	ETHERC0	15		11 ~ 14		PCLKA	Ethernet MAC Controller
4006 4200h	4006 42FFh	EDMAC1	6		2 ~ 5		PCLKA	Ethernet DMA Controller
4006 4300h	4006 43FFh	ETHERC1	15		11 ~ 14		PCLKA	Ethernet MAC Controller
4006 4400h	4006 44FFh	PTPEDMAC	6		2 ~ 5		PCLKA	Ethernet DMA Controller
4006 4500h	4006 45FFh	EPTPC_CFG, EPTPC, EPTPCn	(3+wait cycle)*3		(wait cycle-1) ~ (2+wait cycle)		PCLKA	Ethernet PTP Controller
4007 2000h	4007 2FFFh	SPI0, SPI1	5*5		1 ~ 4*5		PCLKA	Serial Peripheral Interface
4007 4000h	4007 4FFFh	CRC	5		1 ~ 4		PCLKA	CRC Calculator
4007 8000h	4007 8FFFh	GPT32EHi, GPT32Ej, GPT32k, GPT_OPS	Refer to Table 3*6				PCLKA	General PWM Timer
4007 B000h	4007 BFFFh	GPT_ODC	4		1 ~ 3		PCLKA	PWM Delay Generation Circuit
4008 0000h	4008 1FFFh	KINT, CTSU	4		1 ~ 3		PCLKB	Key Interrupt Function, Capacitive Touch Sensing Unit
4008 4000h	4008 4FFFh	AGTn	7	5	3 ~ 6	1 ~ 4	PCLKB	Asynchronous General Purpose Timer
4008 5000h	4008 5FFFh	ACMPHSn	4		1 ~ 3		PCLKB	High-Speed Analog Comparator
4009 0000h	4009 03FFh	USBFS	6		2 ~ 5		PCLKB	USB 2.0 Full-Speed Module

Table 3.2 Access cycles for non-GPT modules (3 of 3)

Address		Peripherals	Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
From	To		Read	Write	Read	Write		
4009 0400h	4009 04FFh	USBFS	4		1 ~ 3		PCLKB	USB 2.0 Full-Speed Module
4009 4000h	4009 4FFFh	PDC	5		1 ~ 4		PCLKB	Parallel Data Capture Unit
400E 0000h	400E 4FFFh	GLCDC, DRW	5		1 ~ 4		PCLKA	Graphics LCD Controller
400E 6000h	400E 603Fh	JPEG	15	7	11 ~ 14	3 ~ 6	PCLKA	JPEG Codec
400E 6040h	400E 6FFFh	JPEG	7	6	3 ~ 6	2 ~ 5	PCLKA	JPEG Codec
6400 0000h	6400 000Fh	QSPI	5	15 ~ *7	1 ~ 4	11 ~ *7	PCLKA	Quad Serial Peripheral Interface
6400 0010h	6400 0013h	QSPI	26 ~	7 ~ *7	22 ~ *7	3 ~ *7	PCLKA	Quad Serial Peripheral Interface
6400 0014h	6400 0037h	QSPI	5	15 ~ *7	1 ~ 4	11 ~ *7	PCLKA	Quad Serial Peripheral Interface
6400 0804h	6400 0807h	QSPI	4	4	1 ~ 3	1 ~ 3	PCLKA	Quad Serial Peripheral Interface

[After]

Table 3.2 Access cycles for non-GPT modules (1 of 3)

Address		Peripherals	Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
From	To		Read	Write	Read	Write		
4000 0000h	4001 CFFFh	MMPU, SMPU, SPMON, MMF, SRAM, BUS, DMACn, DMA, DTC, ICU, DBG, FCACHE	6				ICLK	Memory Protection Unit, Memory Mirror Function, SRAM, Buses, DMA Controller, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
4001 E000h	4001 E3FFh	SYSTEM	7				ICLK	Operation Modes, Resets, Clock Generation Function, Register Write Protection Function
4001 E400h	4001 E6FFh	SYSTEM	11		7 ~ 9		PCLKB	Low Power Mode, Resets, Low Voltage Detect, Battery Backup Function
4004 0000h	4004 7FFFh	PORTn, PFS, PMISC, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	5		2 ~ 4		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Realtime Clock, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control

Table 3.2 Access cycles for non-GPT modules (2 of 3)

Address		Peripherals	Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
From	To		Read	Write	Read	Write		
4004 8000h	4004 DFEFh	SRCRAM	6	5	3 ~ 5	2 ~ 4	PCLKB	Sampling Rate Converter
4004 DFF0h	4004 DFF7h	SRC	7		4 ~ 6		PCLKB	
4004 DFF8h	4004 DFFFh	SRC	5		2 ~ 4		PCLKB	
4004 E000h	4005 FFFFh	SSIn, CANn, IICn, DOC, ADC12n, TSN, DAC12, AMI	5		2 ~ 4		PCLKB	Serial Sound Interface, Controller Area Network Module, I²C Bus Interface, Data Operation Circuit, 12-Bit A/D Converter, Temperature Sensor, 12-Bit D/A Converter
4006 0000h	4006 0FFFh	USBHS	(5+BWAIT)*2		(2+BWAIT) ~ (4+BWAIT)*2		PCLKA	USB 2.0 High-Speed Module
4006 2000h	4006 2FFFh	SDHIn	5		2 ~ 4		PCLKA	SD/MMC Host Interface
4006 4000h	4006 40FFh	EDMAC0	6		3 ~ 5		PCLKA	Ethernet DMA Controller
4006 4100h	4006 41FFh	ETHERC0	15		12 ~ 14		PCLKA	Ethernet MAC Controller
4006 4200h	4006 42FFh	EDMAC1	6		3 ~ 5		PCLKA	Ethernet DMA Controller
4006 4300h	4006 43FFh	ETHERC1	15		12 ~ 14		PCLKA	Ethernet MAC Controller
4006 4400h	4006 44FFh	PTPEDMAC	6		3 ~ 5		PCLKA	Ethernet DMA Controller
4006 4500h	4006 45FFh	EPTPC_CFG, EPTPC, EPTPCn	(3+wait cycle)*3		(wait cycle) ~ (2+wait cycle)		PCLKA	Ethernet PTP Controller
4007 0000h	4007 0EFFh	SCI0 to SCI9	5*4		2 ~ 4*4		PCLKA	Serial Communications Interface
4007 0F00h	4007 0FFFh	IRDA	5		2 ~ 4		PCLKA	IrDA Interface
4007 2000h	4007 2FFFh	SPI0, SPI1	5*5		2 ~ 4*5		PCLKA	Serial Peripheral Interface
4007 4000h	4007 4FFFh	CRC	5		2 ~ 4		PCLKA	CRC Calculator
4007 8000h	4007 8FFFh	GPT32EHi, GPT32Ej, GPT32k, GPT_OPS	Refer to Table 3*6				PCLKA	General PWM Timer
4007 B000h	4007 BFFFh	GPT_ODC	4		1 ~ 3		PCLKA	PWM Delay Generation Circuit
4008 0000h	4008 1FFFh	KINT, CTSU	4		1 ~ 3		PCLKB	Key Interrupt Function, Capacitive Touch Sensing Unit
4008 4000h	4008 4FFFh	AGTn	7	5	4 ~ 6	2 ~ 4	PCLKB	Asynchronous General Purpose Timer
4008 5000h	4008 5FFFh	ACMPHSn	4		1 ~ 3		PCLKB	High-Speed Analog Comparator
4009 0000h	4009 03FFh	USBFS	6		3 ~ 5		PCLKB	USB 2.0 Full-Speed Module

Table 3.2 Access cycles for non-GPT modules (3 of 3)

Address		Peripherals	Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
From	To		Read	Write	Read	Write		
4009 0400h	4009 04FFh	USBFS	4		1 ~ 3		PCLKB	USB 2.0 Full-Speed Module
4009 4000h	4009 4FFFh	PDC	5		2 ~ 4		PCLKB	Parallel Data Capture Unit
400E 0000h	400E 4FFFh	GLCDC, DRW	5		2 ~ 4		PCLKA	Graphics LCD Controller
400E 6000h	400E 603Fh	JPEG	15	7	12 ~ 14	4 ~ 6	PCLKA	JPEG Codec
400E 6040h	400E 6FFFh	JPEG	7	6	4 ~ 6	3 ~ 5	PCLKA	JPEG Codec
6400 0000h	6400 000Fh	QSPI	5	15 ~ *7	2 ~ 4	12 ~ *7	PCLKA	Quad Serial Peripheral Interface
6400 0010h	6400 0013h	QSPI	26 ~	7 ~ *7	23 ~ *7	4 ~ *7	PCLKA	Quad Serial Peripheral Interface
6400 0014h	6400 0037h	QSPI	5	15 ~ *7	2 ~ 4	12 ~ *7	PCLKA	Quad Serial Peripheral Interface
6400 0804h	6400 0807h	QSPI	4	4	1 ~ 3	1 ~ 3	PCLKA	Quad Serial Peripheral Interface