Date: Jul. 3, 2017

# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-R8C-A058B/E | Rev. | 2.00 |
|---|---|---|---|---|---|---|
| Title | Caution on using wait mode and stop mode | | Information Category | Technical Notification | | |
| Applicable Product | R8C/54E, R8C/54F, R8C/54G, R8C/54H, R8C/56E, R8C/56F, R8C/56G, R8C/56H | Lot No.<br>- | Reference Document | Latest user's Manual of applicable products | | |

This caution below applies to wait mode and stop mode in the above mentioned Applicable Products.

## 1. Description

The interrupt request flag may not be set to "1", when two or more interrupt requests are generated simultaneously under the condition that there are two or more peripheral functions and their operations in wait mode/stop mode are enabled [Note 1]. In this case, the interrupt request flag isn't set to "1" even though another same interrupt source is generated.

Note 1. The peripheral functions, the interrupt request flag (the IR bit in the corresponding interrupt control register) of which is set to "1" (interrupt requested) in wait mode/stop mode.

## 2. Conditions

This caution shall be applied when all the following conditions are met.

(1) In Wait mode/Stop mode

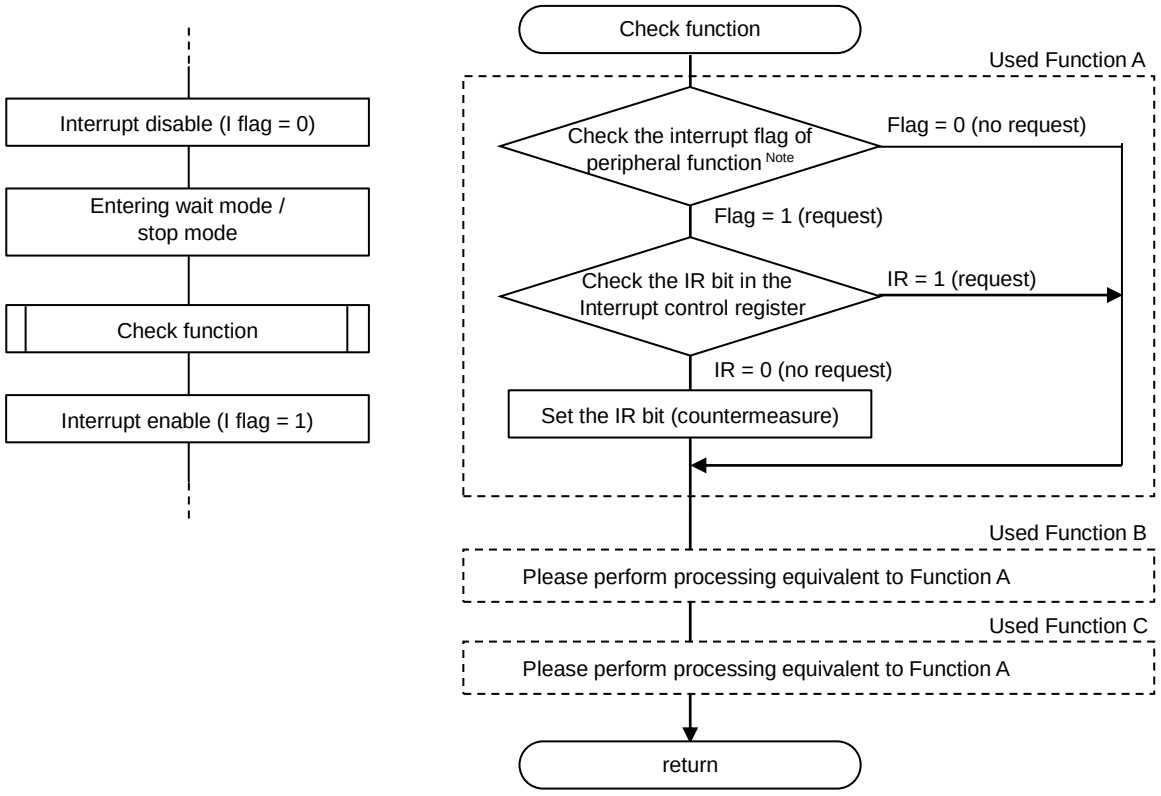
(2) There are two or more peripheral functions and their operations in wait mode/stop mode are enabled.

(3) An interrupt source A, which is used to exit wait mode/stop mode, is generated and then an enabled peripheral function interrupt source B is generated just when the CPU is started by interrupt source A.

## 3. Countermeasure

Execute the following countermeasure in your software.

- Disable the interrupt (setting the I flag in the Flag register to "0") before entering wait mode/stop mode. After exiting wait mode/stop mode, compare the interrupt request flag of the peripheral function, the operation of which is enabled, with the interrupt request bit corresponding to the peripheral function. If the peripheral function interrupt flag is set to "1" and the IR bit in the corresponding interrupt control register is set to "0" (no interrupt requested), set the IR bit in the interrupt control register to "1". And then, enable the interrupts (set the I flag to "1"). In this way, the interrupts which have been generated can be processed properly.




Note. The timer RC, timer RD, timer RE2, timer RF, timer RG, synchronous serial communication unit/ $I^2C$ bus interface, and CAN error interrupts each have multiple interrupt request sources. An interrupt request is generated by the logical OR of those interrupt request sources. Check the interrupt flags that are the bits of enabled interrupt request source status register (status register) by interrupt request source enable register (enable register). Branch to “Flag = 0” when interrupt request source enable register is disabled.

Figure. Flowchart of countermeasure

### 3.1 Caution on software measures

- To enter wait mode, disable the interrupts (set the I flag in the Flag register (FLG) to “0”) and set the CM30 bit in the CM3 register to “1”. Don’t use the WAIT instruction.
- Before entering stop mode, disable the interrupts.
- Use the MOV instruction when setting the IR bit in the interrupt control register to “1” as a measure for this caution (caution on using wait mode and stop mode).
- When an “interrupt-judging function” is called as a measure for this caution (caution on using wait mode and stop mode), the stack area are consumed.

3.2 Description of judgement bit

| Interrupt Source | Interrupt flag of the peripheral functions | Interrupt request bit |
|---|---|---|
| Timer RJ_1 | LINIF bit in the LINIR_1 register Note 2 | IR bit in the TRJIC_1 register |
| INT4 | INT4S bit in the INTSTS register Note 2 | IR bit in the INT4IC register |
| Timer RC_0 | Each bit in the TRCSR_0 register Note 4 | IR bit in the TRCIC_0 register |
| Timer RD0_0 | Each bit in the TRDSR0_0 register Note 4 | IR bit in the TRD0IC_0 register |
| Timer RD1_0 | Each bit in the TRDSR1_0 register Note 4 | IR bit in the TRD1IC_0 register |
| UART2 transmit | U2TIF bit in the U2IR register Note 2 | IR bit in the U2TIC register |
| UART2 receive | U2RIF bit in the U2IR register Note 2 | IR bit in the U2RIC register |
| Key input | KIIS bit in the KIS register Note 2 | IR bit in the KUPIC register |
| Synchronous serial communication unit/ $I^2C$ bus interface (SSU0/ IIC0) | Each bit in the SISR_0 register Note 4 | IR bit in the SSUIC_0/ IICIC_0 register |
| Timer RF/ Compare 0/ Compare 1/Capture Note1 | Each bit in the TRFSR register Note 4 | IR bit in the TRFIC register |
| UART0_0 transmit | U0TIF bit in the U0IR_0 register Note 2 | IR bit in the U0TIC_0 register |
| UART0_0 receive | U0RIF bit in the U0IR_0 register Note 2 | IR bit in the U0RIC_0 register |
| UART0_1 transmit | U0TIF bit in the U0IR_1 register Note 2 | IR bit in the U0TIC_1 register |
| UART0_1 receive | U0RIF bit in the U0IR_1 register Note 2 | IR bit in the U0RIC_1 register |
| INT2 | INT2S bit in the INTSTS register Note 2 | IR bit in the INT2IC register |
| Timer RJ_0 | LINIF bit in the LINIR_0 register Note 2 | IR bit in the TRJIC_0 register |
| Timer RB2_0 | TRBIF bit in the TRBIR_0 register | IR bit in the TRB2IC_0 register |
| INT1 | INT1S bit in the INTSTS register Note 2 | IR bit in the INT1IC register |
| INT3 | INT3S bit in the INTSTS register Note 2 | IR bit in the INT3IC register |
| INT0 | INT0S bit in the INTSTS register Note 2 | IR bit in the INT0IC register |
| UART2 bus collision detection | U2BCNIF bit in the U2IR register Note 2 | IR bit in the U2BCNIC register |
| Timer RG Note 1 | Each bit in the TRGSR register Note 4 | IR bit in the TRGIC register |
| CAN_0 error | WKUP bit in the CANISR_0 register Note 4 | IR bit in the CANERIC_0 register |
| Voltage monitor 1 Note 3 | VW1C2 bit in the VW1C register | IR bit in the VCMP1IC register |
| Voltage monitor 2 Note 3 | VW2C2 bit in the VW2C register | IR bit in the VCMP2IC register |
| Synchronous serial communication unit/ $I^2C$ bus interface (SSU1/ IIC1) | Each bit in the SISR_1 register Note 4 | IR bit in the SSUIC_1/ IICIC_1 register |
| Timer RC_1 Note 1 | Each bit in the TRCSR_1 register Note 4 | IR bit in the TRCIC_1 register |

Note:

1. Provided only in R8C/56E, R8C/56F, R8C/56G and R8C/56H products.
2. Refer to “3.3 Register and flag used in a judgement” for the details on the applicable registers and bits.
3. The interrupt source is enabled only when the maskable interrupt is selected.
4. The bits of status register that the corresponding interrupt enable bits are set to 1.

### 3.3 Register and flag used in a judgement

The red words (registers and flags) are not described in Hardware manual. In the case of not applicable, the setting of these registers and flags is unnecessary.

(1) UART0 Interrupt Flag and Enable Register (U0IR)

Address: 00088h (U0IR_0), 00098h (U0IR_1)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | U0TIF | U0RIF | - | - | U0TIE | U0RIE | - | - |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0-b1 | - | Nothing is assigned. The write value must be 0. The read value is 0. | | - |
| b2 | U0RIE | UART0 receive interrupt enable bit | 0: Receive interrupt disabled<br>1: Receive interrupt enabled | R/W |
| b3 | U0TIE | UART0 transmit interrupt enable bit | 0: Transmit interrupt disabled<br>1: Transmit interrupt enabled | R/W |
| b4-b5 | - | Nothing is assigned. The write value must be 0. The read value is 0. | | - |
| b6 | U0RIF | UART0 receive interrupt request flag | [Conditions for setting to 0]<br>• When the IR bit of these flag becomes 0 from 1.<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• When the interrupt request of these flag occurs. | R/W |
| b7 | U0TIF | UART0 transmit interrupt request flag | | R/W |

(2) Timer RJ/ LIN Interrupt Request Register (LINIR)

Address: 0008Dh (LINIR_0), 0009Dh (LINIR_1)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | - | - | - | - | - | - | TRJIF |
| After Reset | X | X | X | X | X | X | X | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | LINIF | Timer RJ/ LIN interrupt request flag | [Conditions for setting to 0]<br>• When the IR bit of these flag becomes 0 from 1.<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• When the interrupt request of these flag occurs. | R/W |
| b1-b7 | - | Nothing is assigned. The write value must be 0. The read value is 0. | | - |

(3) UART2 Interrupt Status Register (U2IR)

Address: 000D8h (U2IR)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | U2TIF | U2RIF | - | U2BCNIF | - | - | - | - |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0-b3 | - | Reserved | Set to 0. | R/W |
| b4 | U2BCNIF | Bus collision detection interrupt request flag | 0: No interrupt requested Note 1<br>1: Interrupt requested | R/W |
| b5 | - | Reserved | Set to 0. | R/W |
| b6 | U2RIF | Receive interrupt request flag | 0: No interrupt requested Note 1<br>1: Interrupt requested | R/W |
| b7 | U2TIF | Transmit interrupt request flag | | R/W |

Note 1. The flag is set to 0 only when 0 is written after reading 1.
[Conditions for setting to 0]
• When the IR bit of these flag becomes 0 from 1.
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• When the interrupt request of these flag occurs.

(4) INT Interrupt Status Register (INTSTS)

Address: 00235h (INTSTS)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | - | - | INT4S | INT3S | INT2S | INT1S | INT0S |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | INT0S | INT0 interrupt request flag | [Conditions for setting to 0]<br>• When the IR bit of these flag becomes 0 from 1.<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• When the interrupt request of these flag occurs. | R/W |
| b1 | INT1S | INT1 interrupt request flag | | R/W |
| b2 | INT2S | INT2 interrupt request flag | | R/W |
| b3 | INT3S | INT3 interrupt request flag | | R/W |
| b4 | INT4S | INT4 interrupt request flag | | R/W |
| b5-b7 | - | Reserved | Set to 0. | R/W |

(5) Key Input Interrupt Status Register (KIS)

Address: 00237h (KIS)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | KIIS | - | - | - | - | - | - | - |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0-b6 | - | Reserved | Set to 0. | R |
| b7 | KIIS | Key input interrupt request flag | [Conditions for setting to 0]<br>• When the IR bit of these flag becomes 0 from 1.<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• When the interrupt request of these flag occurs. | R/W |

(6) Voltage Monitor 1 Circuit Control Register (VW1C)

Address: 00039h (VW1C)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | VW1C7 | - | VW1F1 | VW1F0 | VW1C3 | VW1C2 | VW1C1 | VW1C0 |
| After Reset | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | VW1C0 | Voltage monitor 1 interrupt enable bit | 0: Disabled<br>1: Enabled | R/W |
| b1 | VW1C1 | Voltage monitor 1 digital filter mode select bit | 0: Digital filter enabled mode (digital filter circuit enabled)<br>1: Digital filter disabled mode (digital filter circuit disabled) | R/W |
| b2 | VW1C2 | Voltage change detection flag | 0: Not detected<br>1: Detected by passing through Vdet1 | R/W |
| b3 | VW1C3 | Voltage detection 1 signal monitor flag | 0: VCC < Vdet1<br>1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled | R |
| b4 | VW1F0 | Sampling clock select bits | 00B: fLOCO divided by 1<br>01B: fLOCO divided by 2<br>10B: fLOCO divided by 4<br>11B: fLOCO divided by 8 | R/W |
| b5 | VW1F1 | | | R/W |
| b6 | - | Reserved | Set to 0. | R/W |
| b7 | VW1C7 | Voltage monitor 1 interrupt generation condition select bit | 0: VCC reaches Vdet1 or above<br>1: VCC reaches Vdet1 or below | R/W |

(7) Voltage Monitor 2 Circuit Control Register (VW2C)

Address: 0003Ah (VW2C)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | VW2C7 | - | VW2F1 | VW2F0 | VW2C3 | VW2C2 | VW2C1 | VW2C0 |
| After Reset | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | VW2C0 | Voltage monitor 2 interrupt enable bit | 0: Disabled<br>1: Enabled | R/W |
| b1 | VW2C1 | Voltage monitor 2 digital filter mode select bit | 0: Digital filter enabled mode (digital filter circuit enabled)<br>1: Digital filter disabled mode (digital filter circuit disabled) | R/W |
| b2 | VW2C2 | Voltage change detection flag | 0: Not detected<br>1: Detected by passing through Vdet2 | R/W |
| b3 | VW2C3 | Voltage detection 2 signal monitor flag | 0: VCC < Vdet2<br>1: VCC ≥ Vdet2 or voltage detection 2 circuit disabled | R |
| b4 | VW2F0 | Sampling clock select bits | 00B: fLOCO divided by 1<br>01B: fLOCO divided by 2<br>10B: fLOCO divided by 4<br>11B: fLOCO divided by 8 | R/W |
| b5 | VW2F1 | | | R/W |
| b6 | - | Reserved | Set to 0. | R/W |
| b7 | VW2C7 | Voltage monitor 2 interrupt generation condition select bit | 0: VCC reaches Vdet2 or above<br>1: VCC reaches Vdet2 or below | R/W |

(8) SI Status Register (SISR)

SSU Function:

Address: 000EAh (SISR_0), 000FAh (SISR_1)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | TDRE | TEND | RDRF | NACKF | STOP | ORER_AL | AAS | CE_ADZ |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | CE_ADZ | Conflict error flag | 0: No conflict error<br>1: Conflict error | R/W |
| b1 | AAS | Reserved | Set to 0. | R/W |
| b2 | ORER_AL | Overrun error flag | 0: No overrun error<br>1: Overrun error | R/W |
| b3 | STOP | Reserved | Set to 0. | R/W |
| b4 | NACKF | Reserved | Set to 0. | R/W |
| b5 | RDRF | Receive data register full flag | 0: No data in the SIRDR register<br>1: Data present in the SIRDR register | R/W |
| b6 | TEND | Transmit end flag | 0: The TDRE bit is 0 when the last bit of transmit data is transmitted<br>1: The TDRE bit is 1 when the last bit of transmit data is transmitted | R/W |
| b7 | TDRE | Transmit data empty flag | 0: Data is not transferred from registers SITDR to SISDR<br>1: Data is transferred from registers SITDR to SISDR | R/W |

I²C bus Function:

Address: 000EAh (SISR_0), 000FAh (SISR_1)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | TDRE | TEND | RDRF | NACKF | STOP | ORER_AL | AAS | CE_ADZ |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | CE_ADZ | General call address recognition flag | This flag is set to 1 when a general call address is detected. | R/W |
| b1 | AAS | Slave address recognition flag | This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SIMR2 register in slave receive mode (slave address detection, general call address detection). | R/W |
| b2 | ORER_AL | Arbitration lost flag/overrun error flag | In I²C bus interface mode, this flag indicates that arbitration is lost in master mode. This flag is set to 1 when:<br>• The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode<br>• The SDA pin is held high at start condition detection in master transmit/receive mode<br><br>In clock synchronous serial mode, this bit indicates that an overrun error has occurred. This flag is set to 1 when:<br>• The last bit of the next data is received while the RDRF bit is set to 1. | R/W |
| b3 | STOP | Stop condition detection flag | This flag is set to 1 when a stop condition is detected after the frame is transferred. | R/W |
| b4 | NACKF | No acknowledge detection flag | This flag is set to 1 when no ACKnowledge is detected<br>from the receive device after transmission. | R/W |
| b5 | RDRF | Receive data register full flag | This flag is set to 1 when receive data is transferred from registers SISDR to SIRDR. | R/W |
| b6 | TEND | Transmit end flag | In I²C bus interface mode, this flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is 1.<br>In clock synchronous mode, this flag is set to 1 when the last bit of the transmit frame is transmitted. | R/W |
| b7 | TDRE | Transmit data empty flag | This flag is set to 1 when:<br>• Data is transferred from registers SITDR to SISDR and the SITDR register becomes empty.<br>• The TRS bit in the SICR1 register is set to 1 (transmit mode)<br>• A start condition is generated (including retransmission)<br>• Slave receive mode is changed to slave transmit mode | R/W |

(9) Timer RB2 Interrupt Request Register (TRBIR)

Address: 00137h (TRBIR_0)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | TRBIE | TRBIF | - | - | - | - | - | - |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0-b5 | - | Nothing is assigned. The write value must be 0. The read value is 0. | | - |
| b6 | TRBIF | Timer RB2 interrupt request flag | 0: No interrupt requested<br>1: Interrupt requested | R/W |
| b7 | TRBIE | Timer RB2 interrupt enable bit | 0: Interrupt disabled<br>1: Interrupt enabled | R/W |

(10) Timer RC Status Register (TRCSR)

Address: 00145h (TRCSR_0), 00165h (TRCSR_1)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | OVF | - | - | - | IMFD | IMFC | IMFB | IMFA |
| After Reset | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | IMFA | Input capture/ compare match A flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>• Set to 0 by the DTC acknowledge when the DTC is activated by an IMFi interrupt.<br>[Condition for setting to 1]<br>• Input Capture Function<br>When the value of the TRCCNT register is transferred to the TRCGRA register at the input edge of the TRCIOi pin.<br>• Output Compare Function/ PWM Mode/ PWM2 Mode<br>When the values of registers TRCCNT and TRCGRi match.<br>(i = A to D) | R/W |
| b1 | IMFB | Input capture/ compare match B flag | | R/W |
| b2 | IMFC | Input capture/ compare match C flag | | R/W |
| b3 | IMFD | Input capture/ compare match D flag | | R/W |
| b4-b6 | - | Nothing is assigned. The write value must be 1. The read value is 1. | | - |
| b7 | OVF | Timer overflow flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• When the TRCCNT register overflows from FFFFh to 0000h. | R/W |

(11) Timer RD Status Register 0 (TRDSR0)

Address: 00193h (TRDSR0_0)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | - | - | OVF | IMFD | IMFC | IMFB | IMFA |
| After Reset | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | IMFA | Input capture/ compare match A flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• Input Capture Function<br>When the value of the TRD0 is transferred to the TRDGRi0 register at the input edge of the TRDIOi0 pin.<br>• Functions other than Input Capture Function<br>When the values of registers TRD0 and TRDGRi0 match.<br>(i = A to D) | R/W |
| b1 | IMFB | Input capture/ compare match B flag | | R/W |
| b2 | IMFC | Input capture/ compare match C flag | | R/W |
| b3 | IMFD | Input capture/ compare match D flag | | R/W |
| b4 | OVF | Overflow flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• When the TRD0 overflows from FFFFh to 0000h. | R/W |
| b5-b7 | - | Nothing is assigned. The write value must be 1. The read value is 1. | | - |

(12) Timer RD Status Register 1 (TRDSR1)

Address: 001A3h (TRDSR1_0)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | - | UDF | OVF | IMFD | IMFC | IMFB | IMFA |
| After Reset | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | IMFA | Input capture/ compare match A flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• Input Capture Function<br>When the value of the TRD1 is transferred to the TRDGRi1 register at the input edge of the TRDIOi1 pin.<br>• Functions other than Input Capture Function<br>When the values of registers TRD1 and TRDGRi1 match.<br>(i = A to D) | R/W |
| b1 | IMFB | Input capture/ compare match B flag | | R/W |
| b2 | IMFC | Input capture/ compare match C flag | | R/W |
| b3 | IMFD | Input capture/ compare match D flag | | R/W |
| b4 | OVF | Overflow flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• When the TRD0 overflows from FFFFh to 0000h. | R/W |
| b5 | UDF | Underflow flag | In complementary PWM mode<br>[Source for setting to 0]<br>Write 0 after reading.<br>[Source for setting to 1]<br>When TRD1 underflows.<br>Enabled only in complementary PWM mode. | R/W |
| b6-b7 | - | Nothing is assigned. The write value must be 1. The read value is 1. | | - |

(13) Timer RF Status Register (TRFSR)

Address: 001B4h (TRFSR)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | - | - | - | OVF | ICF | CMP1F | CMP0F |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | CMP0F | Compare 0 match flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1] | R/W |
| b1 | CMP1F | Compare 1 match flag | • Output compare mode<br>When the value of registers TRF and TRFMi match. (i = 0, 1) | R/W |
| b2 | ICF | Input capture flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• Input capture mode<br>When the input edge of the TRFI pin is detected. | R/W |
| b3 | OVF | Overflow flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• All mode<br>When the TRF register overflows. | R/W |
| b4-b7 | - | Nothing is assigned. The write value must be 0. The read value is 0. | | - |

(14) Timer RG Status Register (TRGSR)

Address: 001F4h (TRGSR)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | - | - | DIRF | OVF | UDF | IMFB | IMFA |
| After Reset | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | IMFA | Input-capture/ compare-match flag A | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• Input Capture Function<br>Input edge of TRGIOi pin.<br>• Output Compare Function, PWM mode<br>When the values of registers TRG and TRGGRi match.<br>(i = A, B) | R/W |
| b1 | IMFB | Input-capture/ compare-match flag B | | R/W |
| b2 | UDF | Underflow flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• When the TRG register underflows. | R/W |
| b3 | OVF | Overflow flag | [Conditions for setting to 0]<br>• When 0 is written to this bit after reading it as 1.<br>[Condition for setting to 1]<br>• When the TRG register overflows. | R/W |
| b4 | DIRF | Count direction flag | 0: TRG register is decremented<br>1: TRG register is incremented | R |
| b5-b7 | - | Nothing is assigned. The write value must be 1. The read value is 1. | | - |

(15) CAN Interrupt Status Register (CANISR)

Address: 06F7Eh (CANISR_0)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | WKUP | ERR | TFIFO | TE | RFIFO | RE | - | - |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0-b1 | - | Nothing is assigned. The write value must be 0. The read value is 0. | | - |
| b2 | RE | Reception complete interrupt flag | 0: Interrupt requested<br>1: Interrupt requested | R |
| b3 | RFIFO | Receive FIFO interrupt flag Note | | R/W |
| b4 | TE | Transmission complete interrupt flag | | R |
| b5 | TFIFO | Transmit FIFO interrupt flag Note | | R/W |
| b6 | ERR | Bus error, warning, error passive, bus-off start, bus-off recovery, overrun, overload, and bus lock interrupt flag Note | | R/W |
| b7 | WKUP | Wake-up interrupt flag Note | | R/W |

Note. This flag is set to 0 only when 0 is written after reading 1.

(16) Interrupt Control Register

Address: 00041H (FMRDYIC), 00042H (TRJIC_1), 00046H (INT4IC), 00047H (TRCIC_0), 00048H (TRD0IC_0), 00049H (TRD1IC_0), 0004AH (TRE2IC), 0004BH (U2TIC), 0004CH (U2RIC), 0004DH (KUPIC), 0004EH (ADIC), 0004FH (SSUIC_0/ IICIC_0), 00050H (TRFIC), 00051H (U0TIC_0), 00052H (U0RIC_0), 00053H (U0TIC_1), 00054H (U0RIC_1), 00055H (INT2IC), 00056H (TRJIC_0), 00058H (TRB2IC_0), 00059H (INT1IC), 0005AH (INT3IC), 0005DH (INT0IC), 0005EH (U2BCNIC), 0006BH (TRGIC), 0006CH (CANRXIC_0), 0006DH (CANTXIC_0), 0006EH (CANERIC_0), 00072H (VCMP1IC), 00073H (VCMP2IC), 00079H (SSUIC_1/ IICIC_1), 0007FH (TRCIC_1)

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | - | - | - | IR | ILVL2 | ILVL1 | ILVL0 |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | ILVL0 | Interrupt priority level select bits | 000B: Level 0 (interrupt disabled)<br>001B-111B: Level 1 to Level 7 | R/W |
| b1 | ILVL1 | | | R/W |
| b2 | ILVL2 | | | R/W |
| b3 | IR | Interrupt request bit | 0: No interrupt requested<br>1: Interrupt requested | R/W Note |
| b4-b7 | - | Nothing is assigned. The write value must be 0. The read value is 0. | | - |

Note. Only 0 can be written to the IR bit. (Do not write 1 to this bit.) However, a case to use as this measure is excluded. In this case, use the MOV instruction when setting the IR bit in the interrupt control register to “1” as a measure for “caution on using wait mode and stop mode”.

## 3.4 Example of software measures (using wait mode)

Examples of the software measures when using wait mode are shown below.

Example)

Interrupts to exit wait mode: Timer RB2 interrupt (ILVL=1), CAN wakeup interrupt (ILVL=6)

The peripheral functions the operations of which are enabled in wait mode: INT1 interrupt (ILVL=0)

| Entering wait mode | | Descriptions |
|---|---|---|
| BCLR | 1, FMR0; | CPU rewrite mode disabled |
| BSET | 0, PRCR; | Writing to CM3 register enabled (Protection disabled) |
| FCLR | I; | Interrupt disabled |
| BSET | 0, CM3; | Enter wait mode |
| NOP; | | Insert at least four NOP instructions |
| NOP; | | |
| NOP; | | |
| NOP; | | |
| BCLR | 0, PRCR; | Writing to CM3 register disabled (Protection enabled) |
| JSR | CHECK_ICU; | The check function is called |
| FSET | I; | Interrupt enabled |
| NOP; | | NOP instruction |

| Check function | | Descriptions |
|---|---|---|
| CHECK_ICU: | | |
| BTST | 6, TRBIR_0; | Judge the TRBIF bit |
| JNC | CHK_ICU001; | Branches to the label when TRBIF bit is 0 |
| BTST | 3, TRB2IC_0; | Judge the IR bit |
| JC | CHK_ICU001; | Branches to the label when IR bit is 1 |
| MOV.B | #009H, TRB2IC_0; | Set the IR bit (Countermeasure) |
| CHK_ICU001: | | |
| TST.B | #080H, CANISR_0; | Judge the WKUP bit |
| JEQ | CHK_ICU002; | Branches to the label when WKUP bit is 0 |
| BTST | 3, CANERIC_0; | Judge the IR bit |
| JC | CHK_ICU002; | Branches to the label when IR bit is 1 |
| MOV.B | #00EH, CANERIC_0; | Set the IR bit (Countermeasure) |
| CHK_ICU002: | | |
| BTST | 1, INTSTS; | Judge the INT1S bit |
| JNC | CHK_ICU003; | Branches to the label when INT1S bit is 0 |
| BTST | 3, INT1IC; | Judge the IR bit |
| JC | CHK_ICU003; | Branches to the label when IR bit is 1 |
| MOV.B | #008H, INT1IC; | Set the IR bit (Countermeasure) |
| CHK_ICU003: | | |
| RTS; | | Return to subroutine |

## 3.5 Example of software measures (using stop mode)

Examples of the software measures when using stop mode are shown below.

Example)

Interrupts to exit wait mode: CAN wakeup interrupt (ILVL=7), INT0 interrupt (ILVL=5)

| Entering stop mode | | Descriptions |
|---|---|---|
| BCLR | 1, FMR0; | CPU rewrite mode disabled |
| BSET | 0, PRCR; | Writing to CM1 register enabled (Protection disabled) |
| FCLR | I; | Interrupt disabled |
| BSET | 0, CM1; | Enter stop mode |
| JMP.B | LABEL_001; | Branches to the label |
| LABEL_001: | | |
| NOP; | | Insert at least four NOP instructions |
| NOP; | | |
| NOP; | | |
| NOP; | | |
| BCLR | 0, PRCR; | Writing to CM1 register disabled (Protection enabled) |
| JSR | CHECK_ICU; | The check function is called |
| FSET | I; | Interrupt enabled |
| NOP; | | NOP instruction |

| Check function | | Descriptions |
|---|---|---|
| CHECK_ICU: | | |
| TST.B | #080H, CANISR_0; | Judge the WKUP bit |
| JEQ | CHK_ICU001; | Branches to the label when WKUP bit is 0 |
| BTST | 3, CANERIC_0; | Judge the IR bit |
| JC | CHK_ICU001; | Branches to the label when IR bit is 1 |
| MOV.B | #00FH, CANERIC_0; | Set the IR bit (Countermeasure) |
| CHK_ICU001: | | |
| BTST | 0, INTSTS; | Judge the INT0S bit |
| JNC | CHK_ICU002; | Branches to the label when INT0S bit is 0 |
| BTST | 3, INT0IC; | Judge the IR bit |
| JC | CHK_ICU002; | Branches to the label when IR bit is 1 |
| MOV.B | #00DH, INT0IC; | Set the IR bit (Countermeasure) |
| CHK_ICU002: | | |
| RTS; | | Return to subroutine |