Renesas added a restriction at switching a clock source due to non-response from some interruptions which are RTC periodic interrupt, RTC periodic event output, internal asynchronous (AGT) interrupt and the external pin interrupt.

1. Restriction

When switching a clock source by changing SCKSCR.CKSEL[2:0] which is shown in Figure 1, clock output from the selector stops for 4 cycles of the switched clock as shown in Figure 2. Please follow the conditions below due to avoid not to accept the interrupt requests.

1) When using RTC periodical interrupt, RTC periodical event output or internal asynchronous interrupt, the clock source must be switched at a point in time when the interrupt or the event is not issued.

2) When using external interrupt, the pulse width must be added 4 clock cycles of switched source.
Figure1 Block diagram of clock source selector

- **SCKSCR.CKSEL[2:0]**
- **Source A**
- **Source B**
- **System clock** (SCKDIVCR.ICK[2:0]=000b)
- **Clock source A**
- **Clock source B**
- **Selected clock**
- **PCLKB** (SCKDIVCR.PCKB[2:0]=001b)

**Figure2 Timing of clock source switching**

- ta (maximum): 2 system clock cycles and 3 clock cycles of source A
- tb (maximum): 3.5 clock cycles of source B
- Source A: Clock source before switch
- Source B: Clock source after switch