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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-78K-A009A/E	Rev.	1.00
Title	Restriction regarding watchdog timer		Information Category	Technical Notification		
Applicable Product	78K Family (See Attachment sheet 1)	Lot No. _	Reference Document	Latest user's Manual of applicable products		

This notification has the same content as TN-78K-A008B/E.

The restriction below applies to watchdog timer in the above mentioned Applicable Products.

1. Restriction1 watchdog timer window function

Wrong WDT-RESET may assert when WDT counter is cleared (writing ACh to WDTE register) at just 50% of count-overflow-value and when window open period of watchdog timer is set to 75%.

1.1 Conditions

If following all conditions is established, customer's software is applicable to the restriction.

(1) "Operation of watchdog timer" is "enabled" (WDTON in User option byte = "1")

(2) "Operation of watchdog timer in the HALT or STOP mode" is "enabled" (WDSTBYON in User option byte = "1")

(3) "Setting of window open period of watchdog timer" is "75%" (WINDOW1, WINDOW0 in User option byte = "10b")

(4) During watchdog timer operates, counter is cleared at just 50% of count-overflow-value.

1.2 Countermeasure

Please apply any of the following measures.

Countermeasure1: Set "window open period" to "50%" or "100%".

Countermeasure2: If "window open period" is set to "75%", please perform Counter-clear with the period other than 50% counter value.

2. Restriction2 watchdog timer window function

WDT-RESET may not occur when “25%” is specified as “window open period” and when WDT counter is cleared at just 50% of count-overflow-value.

2.1 Conditions

If following all conditions is established, customer’s software is applicable to the restriction.

(1) “Operation of watchdog timer” is “enabled” (WDTON in User option byte = “1”)

(2) “Operation of watchdog timer in the HALT or STOP mode” is “enabled” (WDSTBYON in User option byte = “1”) Note

(3) “Setting of window open period of watchdog timer” is “25%” (WINDOW1, WINDOW0 in User option byte = “00b”)

(4) During watchdog timer operates, counter is cleared at just 50% of count-overflow-value.

Note. 78K0 Family does not have this function.

2.2 Countermeasure

Set “window open period” to “50%” or “75%” or “100%”.

Note

- Each bit (WDTON, WDSTBYON, WINDOW1, and WINDOW0) is allocated in user option byte. Regarding user option byte area (address), please refer to the hardware manual of the product you are using. 78K0 Family does not have WDSTBYON bit.

[Applicable products]

Attachment Sheet 1

		Restriction 1	Restriction 2
78K0 Family			
78K0/Ix2	UPD78F074x, UPD78F075x	-	✓
78K0/Kx2	UPD78F050x, UPD78F051x, UPD78F052x, UPD78F053x, UPD78F054x	-	✓
78K0/Kx2-A	UPD78F059x	-	✓
78K0/Kx2-C	UPD78F076x	-	✓
78K0/Kx2-L	UPD78F055x, UPD78F056x, UPD78F057x, UPD78F058x	-	✓
78K0/Lx2	UPD78F036x, UPD78F037x, UPD78F038x, UPD78F039x	-	✓
78K0/Lx3	UPD78F040x, UPD78F041x, UPD78F042x, UPD78F043x, UPD78F044x, UPD78F045x, UPD78F046x, UPD78F047x, UPD78F048x, UPD78F049x	-	✓
78K0/Lx3-M	UPD78F805x	-	✓
UPD78F8025	UPD78F802x	-	✓
78K0R Family			
78K0R/Hx3	UPD78F103x, UPD78F104x, UPD78F105x	✓	✓
78K0R/Ix3	UPD78F120x, UPD78F121x, UPD78F122x, UPD78F123x	✓	✓
78K0R/Kx3	UPD78F114x, UPD78F115x, UPD78F116x, UPD78F117x, UPD78F118x	✓	✓
78K0R/Kx3-A	UPD78F101x	✓	-
78K0R/Kx3-C	UPD78F184x	✓	✓
78K0R/Kx3-L	UPD78F100x, UPD78F101x, UPD78F102x, UPD78F103x	✓	-
78K0R/Kx3-L(USB)	UPD78F102x	✓	-
78K0R/Lx3	UPD78F150x, UPD78F151x	✓	-
78K0R/Lx3-M	UPD78F8070	✓	-
UPD78F8043	UPD78F804x	✓	-
UPD78F8058	UPD78F805x	✓	✓
UPD78F8069	UPD78F806x	✓	✓

✓ Applicable

- Not applicable