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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0094A/E	Rev.	1.00
Title	Restriction regarding reading data Flash memory		Information Category	Technical Notification		
Applicable Product	RL78/G11, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/G1D, RL78/G1F, RL78/G1H, RL78/L12, RL78/L13, RL78/L1A, RL78/L1C, RL78/I1A, RL78/I1B, RL78/I1C, RL78/I1D, RL78/I1D	Lot No. –	Reference Document	Latest user's Manual of applicable products		

The restriction below applies to above-mentioned Applicable Products.

1. Description

Applicable Usage

There are restriction when following all conditions are exist.

(1) Reading data flash memory during sub-system clock selected as CPU/peripheral hardware clock (CLS note =1).

(2) Switch over CPU/peripheral hardware clock to main system clock after (1), Reading data flash memory during main system clock selected as CPU/peripheral hardware clock frequency (CLS =0).

(3) Selecting HS or LV mode. Or Selecting LS or LP mode and CPU/peripheral hardware clock frequency is more than 1MHz.

Note: bit 7 of System clock control register (CKC)

Restriction

Read out data flash memory during sub-system clock selected as CPU/peripheral hardware clock frequency (CLS=1) then read out the data flash memory during main system clock selected (CLS=0), read out result may be wrongly changed.

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2. Countermeasure

Please apply one of the following procedures.

Countermeasure 1:

In case of switch over the CPU/peripheral hardware clock from sub-system clock to main system clock, please read data flash after executing the following procedures (1) to (3).

(1) Confirming complete switched to main system clock (CLS=0).

(2) Reading some data flash memory once. Don't use this value.

(3) Waiting until the following time pass.

HS (High-speed main) mode: 5 μs

LS (Low-speed main) mode: 1 μs

LV (Low-voltage main) mode:10 μs

LP (Low-power main) mode: 1 μs

Countermeasure 2:

Please do not read data flash memory during sub-system clock selected as CPU/peripheral hardware clock. If read access to the data flash memory is necessary during sub-system clock is selected for CPU/peripheral hardware clock, please store data flash memory value to RAM before switching sub-system clock, then read out RAM value

3. Improvement plan

This matter is restriction of products.

We will describe this restriction in next revision user's manual of applicable products.

4. Part numbers of applicable products

Table 1 shows product group and part numbers of applicable products.

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Product group	Parts number
RL78/G11	R5F105xxx
RL78/G13	R5F100xxx, R5F101xxx
RL78/G14	R5F104xxx
RL78/G1A	R5F10Exxx
RL78/G1C	R5F10Jxxx, R5F10Kxxx
RL78/G1D	R5F11Axxx
RL78/G1F	R5F11Bxxx
RL78/G1G	R5F11Exxx
RL78/G1H	R5F11Fxxx
RL78/L12	R5F10Rxxx
RL78/L13	R5F10Wxxx
RL78/L1A	R5F11Mxxx
RL78/L1C	R5F110xxx, R5F111xxx
RL78/I1A	R5F107xxx
RL78/I1C	R5F10Nxxx
RL78/I1D	R5F117xxx
RL78/H1D	R5F11Nxxx, R5F11Pxxx, R5F11Rxxx