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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A918A/E	Rev.	1.00
Title	Restriction of input capture function at TPU cascaded operation		Information Category	Technical Notification		
Applicable Product	SH72A2 Group, SH72A0 Group	Lot No. ALL	Reference Document	SH72A2 Group, SH72A0 Group User's Manual: Hardware Rev. 1.00 R01UH0164EJ0100		

Regarding 16-bit timer pulse unit (TPU) implemented in the product shown above, it is found that there is a restriction of input capture function at cascaded operation. Please take the restriction into account at the time of use.

1. Restriction

When 16-bit timer counter 2 and 3 (TP2CNT and TP3CNT) are connected in cascade and operate as 32-bit counter, the value of 32-bit counter can be captured by input capture signal of timer counter 2 and 3 (TP02C and TP03C or TP02D and TP03D) simultaneously.

However, even 2 input capture signals are input simultaneously, there is a possibility that the capture timing of the upper counter and the lower counter can be deviated due to the delay time difference into LSI.
When capturing overflow timing of the lower counter, like from 0000_FFFF to 0001_0000, the captured value should be either 0000_FFFF or 0001_0000, but due to the deviation of the capture timing, 0000_0000, 0001_0000 etc. can be captured.

2. Example of workaround

When these timers are operated as 32-bit input capture counter, the deviation of the captured value can be occurred when the captured values of the lower counter are 0000, 0001 or 0002. In this case, please disable the values, discard the captured value etc.