To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL NEWS No.M16C-114-0310

Replace Sheets of Renesas Technical News No. M16C-106-0309
M16C/62P Group Precautions when Applying “H” to CNVSS Pin

Classification	Concerned Products
Corrections and supplementary explanation of document √ Notes Knowhow Others	M16C/62P Group

RENESAS TECHNICAL NEWS “No. M16C-106-0309” has clerical errors on Figure 1 and 2.
RENESAS TECHNICAL NEWS “M16C/62P Precautions when applying “H” to CNVSS pin” should be replaced with the attached one “No. M16C-106-0309”.

Revised contents

1. “Note 2. when the $\overline{\text{RESET}}$ pin is “L” in boot mode (apply “H” to the CNVSS pin and P5_0 ($\overline{\text{CE}}$), and “L” to the P5_5 ($\overline{\text{EPM}}$)), an internal pull-up is enabled for P6_7” is added on Figure 1 and 2.
   Figure A shows the revised parts.

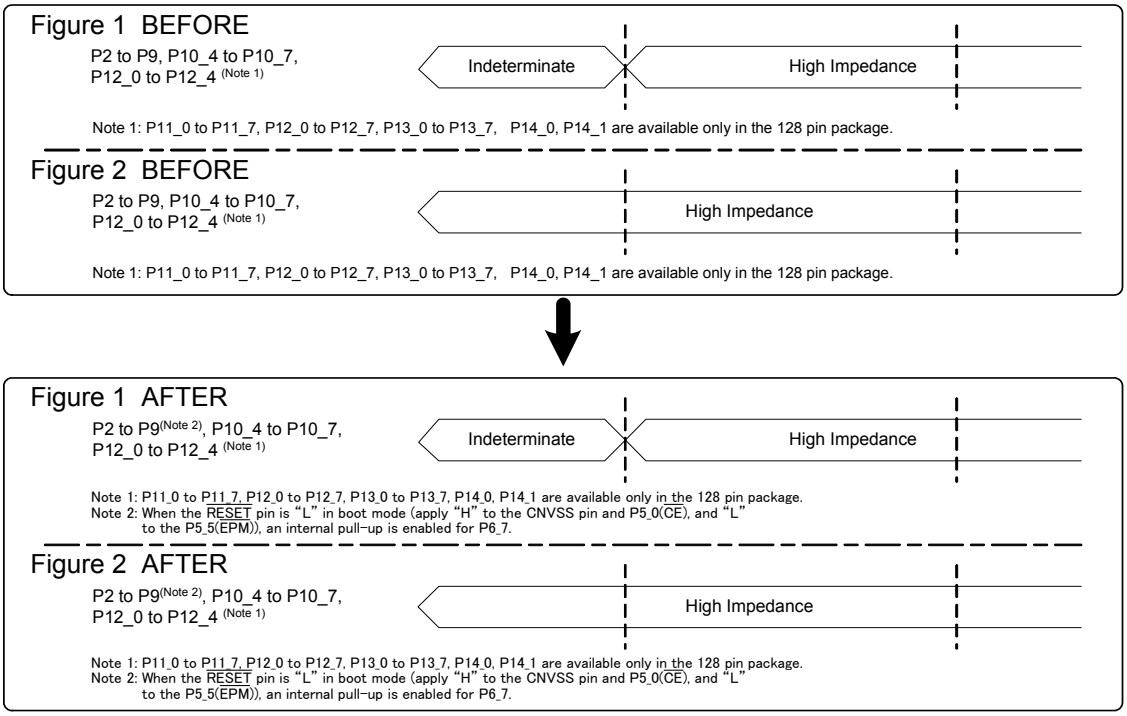


Figure A. Before and after revised parts

2. The “Pull-up enabled “H”” timing and the “Indeterminate” timing have clerical error on Figure 2.

   Figure B shows the revised part.

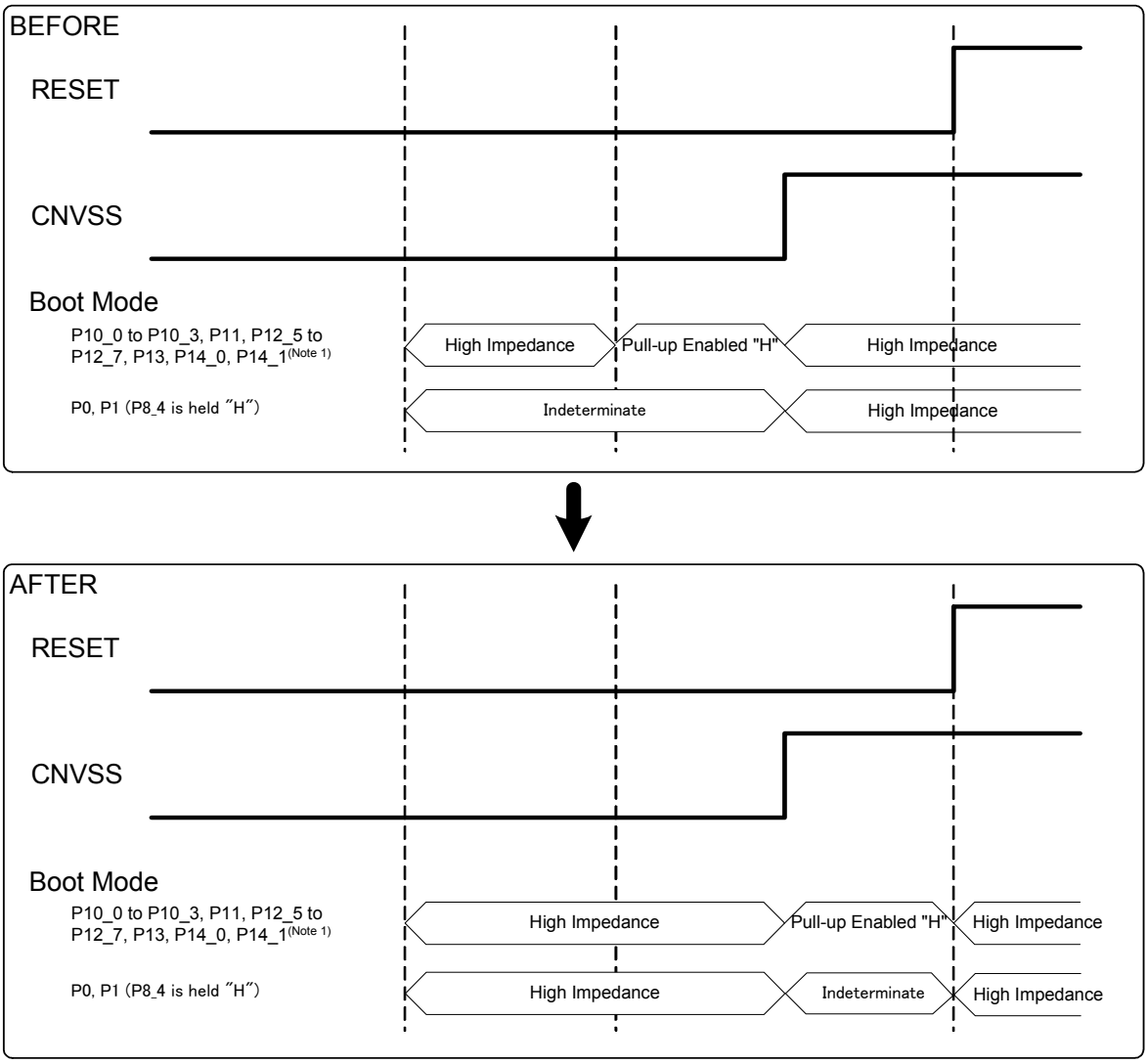


Figure B. Before and after revised parts

RENESAS TECHNICAL NEWS

No.M16C-114-0310

M16C/62P Group
Precautions when Applying “H” to CNVSS Pin

Classification	**Concerned Products**
Corrections and supplementary explanation of document √ Notes Knowhow Others	M16C/62P Group

1. Precautionary Note

1. 1 Precautions in microprocessor mode or boot mode

I/O ports will be indeterminate until internal power supply is stable, such as when the power is turned on, if “H” is applied to the CNVSS pin and “L” to the $\overline{\text{RESET}}$ pin while internal power supply is unstable.

1. 2 Precaution 1 in boot mode

When the $\overline{\text{RESET}}$ pin is “L” in boot mode (apply “H” to the CNVSS pin and P5_0 ($\overline{\text{CE}}$), and “L” to the P5_5 ($\overline{\text{EPM}}$)), internal pull-up is enabled for P10_0 to P10_3, P11_0 to P11_7, P12_5 to P12_7, P13_0 to P13_7, P14_0 and P14_1 (Note 1) and so become “H” level.

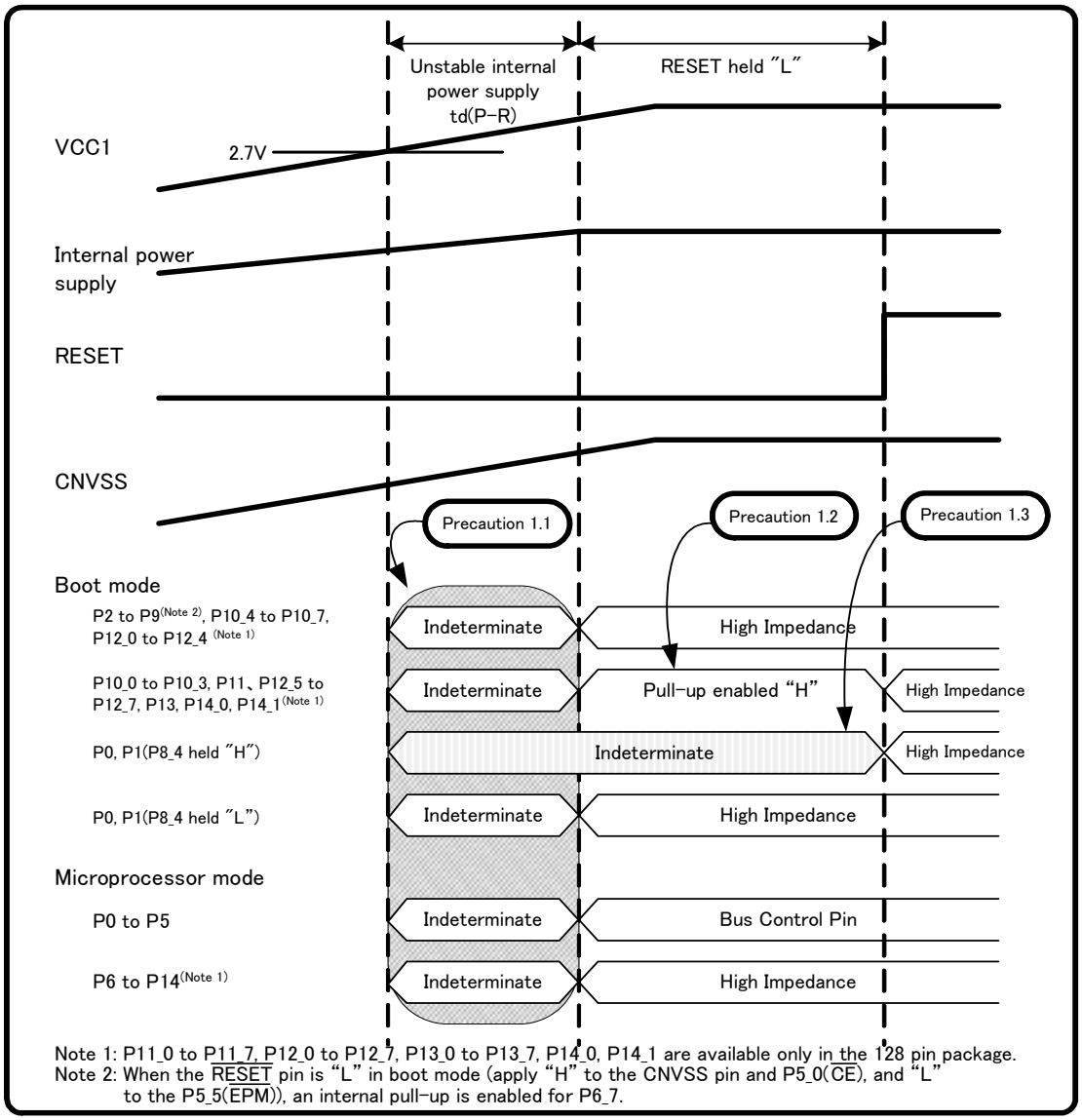
Note 1: P11_0 to P11_7, P12_5 to P12_7, P13_0 to P13_7, P14_0 and P14_1 are available in the 128 pin package only.

1. 3 Precaution 2 in boot mode

P0_0 to P0_7 and P1_0 to P1_7 may become indeterminate when P8_4 is “H” and the $\overline{\text{RESET}}$ pin is “L” in boot mode (apply “H” to the CNVSS pin and P5_0 ($\overline{\text{CE}}$) , and “L” to P5_5 ($\overline{\text{EPM}}$)).

P0_0 to P0_7 and P1_0 to P1_7 are in a high impedance state when the $\overline{\text{RESET}}$ pin and P8_4 are “L”.

Figure 1 shows pin state when turning power on in boot mode and microprocessor mode.



Note 1: P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 are available only in the 128 pin package.
Note 2: When the $\overline{\text{RESET}}$ pin is "L" in boot mode (apply "H" to the CNVSS pin and P5_0($\overline{\text{CE}}$), and "L" to the P5_5($\overline{\text{EPM}}$)), an internal pull-up is enabled for P6_7.

Figure 1. Pin State when Power is Turned On in Boot Mode and Microprocessor Mode

2. Countermeasure

2. 1 Countermeasure for “Precautions in microprocessor mode or boot mode”

Follow the procedures listed below when applying “H” to the CNVSS pin.

1. Apply “L” to the $\overline{\text{RESET}}$ pin and the CNVSS pin
2. Wait more than 2ms (min.) after power applied to the VCC1 pin exceeds over 2.7V (wait time for internal power supply stabilization)
3. Apply “H” to the CNVSS pin
4. Apply “H” to the $\overline{\text{RESET}}$ pin (reset cancellation)

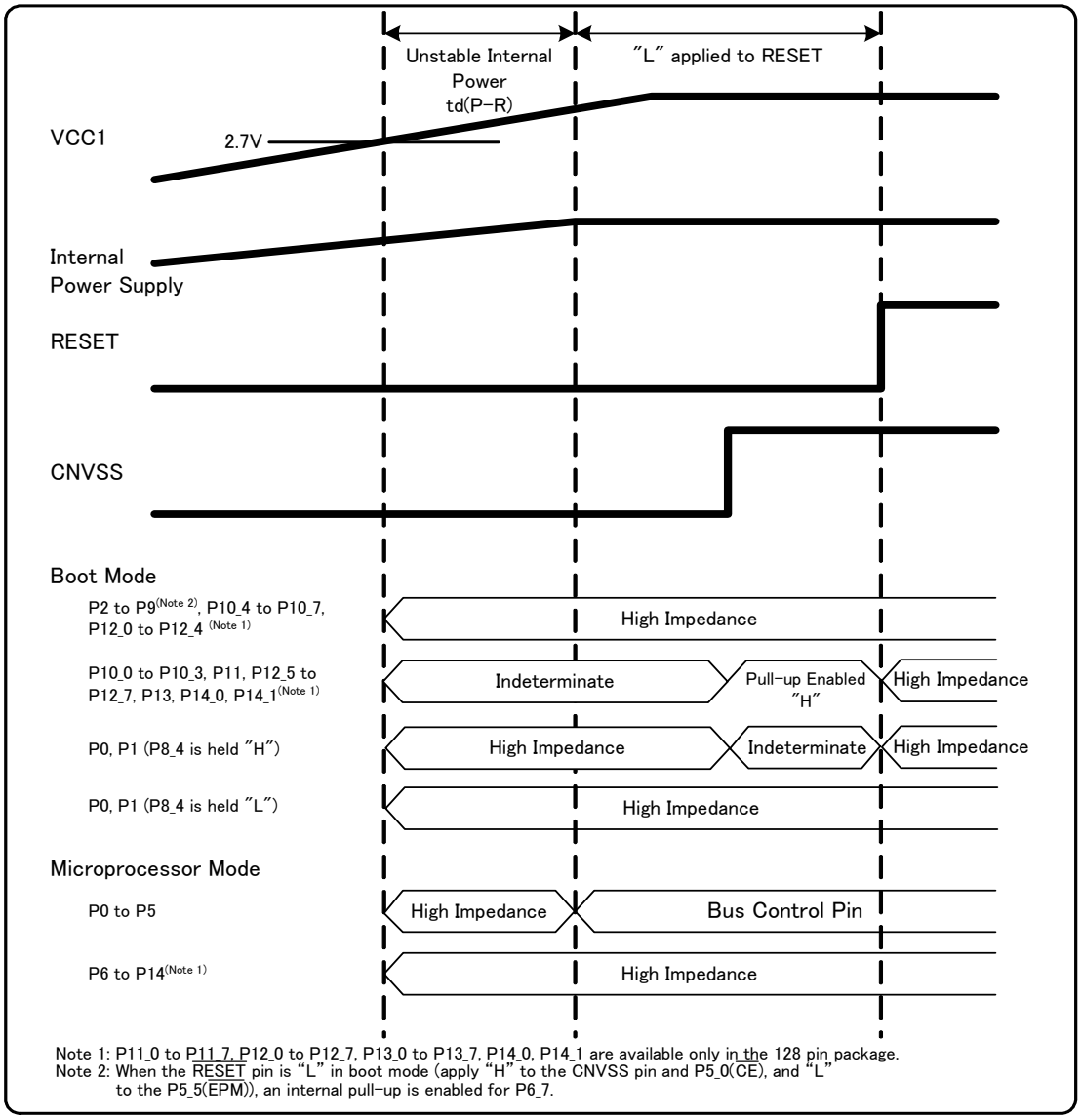


Figure 2. Pin State when Countermeasure is Followed and Power is Turned On

2. 2 Countermeasure for “Precaution 1 in boot mode”

Take measures, such as connecting an external pull-down resistor or using pins other than P10_0 to P10_3, P11_0 to P11_7, P12_5 to P12_7, P13_0 to P13_7, P14_0 and P14_1 if necessary.

2.3 Countermeasure for “Precaution 2 in boot mode”

Apply “L” to P8_4 if necessary.

3. Affected Products

3. 1 Products affected by “Precautions in microprocessor mode or boot mode”

This precaution applies to the following products. Products not listed are not affected.

M16C/62P

Affected Products	
Flash Memory version	M30627FHPGP, M30626FHPFP, M30626FHPGP, M30625FGPGP, M30624FGPFP, M30624FGPGP, M30620FCPFP, M30620FCPGP, M30622F8PFP, M30622F8PGP
Mask ROM version	M30626MHP-XXXFP, M30626MHP-XXXGP, M30627MHP-XXXGP, M30624MHP-XXXFP, M30624MHP-XXXGP, M30625MHP-XXXGP M30622MHP-XXXFP, M30622MHP-XXXGP, M30623MHP-XXXGP, M30626MWP-XXXFP, M30626MWP-XXXGP, M30627MWP-XXXGP M30624MWP-XXXFP, M30624MWP-XXXGP, M30625MWP-XXXGP, M30624MGP-XXXFP, M30624MGP-XXXGP, M30625MGP-XXXGP

3. 2 Products affected by “Precaution 1 in boot mode”

This precaution applies to the following products. Products not listed are not affected.

M16C/62P

Affected Products	
Flash Memory version	M30627FHPGP, M30626FHPFP, M30626FHPGP, M30625FGPGP, M30624FGPFP, M30624FGPGP, M30620FCPFP, M30620FCPGP, M30622F8PFP, M30622F8PGP

3. 3 Products affected by “Precaution 2 while in boot mode”

This precaution applies to the following products.

M16C/62P

Affected Products	
Flash Memory version	All products