## **RENESAS TECHNICAL UPDATE**

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan Renesas Electronics Corporation

Product Category	MPU/MCU	Document No.	TN-RA*-A0053A/E	Rev.	1.00	
Title	RA6T2 Group Electric Specification	Information Category	Technical Notification			
		Lot No.				
Applicable Product	RA6T2 Group	All	Reference Document	RA6T2 Group User's Manual : Hardware Rev.1.10		

The description of ADC Characteristics is modified.

Colored characters indicate an updated part.

- Red character: remove
- Blue character: add

Table46.35 A/D conversion characteristics

Parameter					Тур	Max	Unit	Test conditions
Resolution					-	12	bit	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN005) (AN006 to AN011)	Conversion time <sup>*1</sup> (operation at ADCLK = 50 MHz)	Permissible signal source impedance Max. = 50Ω	normal conversion	0.70	-	-	μs	<ul> <li>Sampling time of channel-dedicated sample-and-hold circuits: 20 ADCLK</li> <li>Hold mode switching time of channel</li> </ul>
			When using averaging mode(4-time	2.80	-	-	μs	<ul> <li>Hold mode switching time of channel- dedicated sample-and-hold circuits: 2 ADCLK</li> </ul>
			conversion)					<ul> <li>Sampling time : 8 ADCLK</li> </ul>
			,					Successive approximation time : 5     ADCLK
	Offset error			-	±0.5	±1.0	LSB	
	Full-scale error			-	<del>±1.0</del> ±1.5	±1.5	LSB	
	Absolute	normal conversion		-	±5.0	±7.0	LSB	
	accuracy	When using averaging mode (4-time conversion)		-	±4.0	±5.0	LSB	
	Total unadjusted error (TUE)				±3.0	±3.4	LSB	Excludes quantization error (±0.5LSB).
	DNL pseudo-differential nonlinearity error			-	-1 to +1.5	-1 to +2.5	LSB	
	INL integral nonlinearity error			-	±2.0	±3.0	LSB	
High-speed channels (AN000 to AN005) (AN006 to AN011) ((AN018 to AN019) <sup>*2</sup> )	Conversion time <sup>*1</sup> (operation at ADCLK = 50 MHz)	Permissible signal source impedance Max. = 50Ω	normal conversion	0.16	-	-	μs	Sampling time : 3 ADCLK     Successive approximation time : 5     ADCLK
			When using averaging mode(4-time conversion)	0.64	-	-	μs	ADOLK
	Offset error			-	±1.0	±3.0	LSB	
	Full-scale error			-	±1.5	±2.5	LSB	
		ersion	-	±5.5	±7.0	LSB		
		When using averaging mode (4-time conversion)		-	±4.5	±5.5	LSB	
	Total unadjusted error (TUE)				±3.5	±4.0	LSB	Excludes quantization error (±0.5LSB).
	DNL pseudo-differential nonlinearity error			-	-1 to +1.5	-1 to +2.5	LSB	



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Parameter				Min	Тур	Max	Unit	Test conditions
	INL integral nonlinearity error			-	±2.0	±3.0	LSB	
High-precision channels (AN012 to AN017)	Conversion time <sup>*1</sup> (operation at ADCLK = 50 MHz)	Permissible signal source impedance Max. = 50Ω	normal conversion	0.28	-	-	μs	Sampling time : 9 ADCLK     Successive approximation time : 5
			When using averaging mode(4-time conversion)	1.12	-	-	μs	ADCLK
	Offset error			-	±1.0	±1.5	LSB	
	Full-scale error			-	±1.0	±2.5	LSB	
	Absolute	normal conversion		-	±4.0	±7.0	LSB	
	accuracy	When using averaging mode (4-time conversion)		-	±3.0	±5.5	LSB	
	Total unadjusted error (TUE)				±3.4	±4.4	LSB	Excludes quantization error (±0.5LSB).
	DNL pseudo-differential nonlinearity error			-	-1 to +1.5	-1 to +2.5	LSB	
	INL integral nonlinearity error			-	±2.0	±3.0	LSB	
Normal-precision channels	time <sup>*1</sup> (operation at ADCLK = 50	Permissible signal source impedance Max. = 50Ω	normal conversion	0.50	-	-	μs	Sampling time : 20 ADCLK     Successive approximation time : 5
(AN020 to AN028)			When using averaging mode(4-time conversion)	2.00	-	-	μs	ADCLK
	Offset error			-	±1.0	±2.5	LSB	
	Full-scale error			-	±1.5	±2.5	LSB	
	accuracy W	normal conversion		-	±5.5	±8.0	LSB	
		When using averaging mode (4-time conversion)		-	±5.5	±7.0	LSB	
	Total unadjusted error (TUE)				±4.2	±5.3	LSB	Excludes quantization error (±0.5LSB).
	DNL pseudo-differential nonlinearity error			-	-1 to +1.5	-1 to +2.5	LSB	
	INL integral nonlinearity error			-	±2.0	±4.0	LSB	

Note 1. Channel-dedicated sample-and-hold circuits in use; The conversion time is the sum of the sampling time of channel-dedicated sample-and-hold circuits, the hold mode switching time, the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions. Channel-dedicated sample-and-hold circuits not in use; The conversion time is the sum of the sampling time and the successive

approximation time. Each of the above state is indicated for the test conditions.

Note 2. These channels cannot be used with Channel-dedicated sample-and-hold circuits .

