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# RENESAS TECHNICAL UPDATE

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|---|---|---|---|---|---|---|
| Title | RA6T2 Group<br>Changes of Low Power mode specification for ADC | | Information Category | Technical Notification | | |
| Applicable Product | RA6T2 Group | Lot No.<br>All | Reference Document | RA6T2 Group User's Manual : Hardware Rev.1.20 | | |

The specification of Low Power mode for ADC has been modified for the following items

1) Table 10.2
   Operating conditions of each low power mode (2 of 2)
2) Table 10.3
   Interrupt Source for canceling Snooze, Software Standby, and Deep Software Standby modes
3) Section 10.2.11
   SNZEDCR0 : Snooze End Control Register 0
4) Section 10.8.3
   Returning from Snooze Mode to Software Standby mode
   Table 10.8
   Available snooze end requests (triggers to return to Software Standby mode)
   Table 10.9
   Snooze end conditions
5) Section 10.10.12
   Conditions of A/D Conversion Start in Snooze Mode
   Section 10.10.13
   ELC Events in Snooze Mode
6) Table 12.4
   Event table (7 of 9)
7) Table 17.3
   Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (5 of 6)

[Modified]

Table 10.2 Operating conditions of each low power mode (2 of 2)

| Item | Sleep mode | Software Standby mode | Snooze mode | Deep Software Standby mode |
|---|---|---|---|---|
| DMA Controller (DMAC) | Selectable | Stop (Retained) | Operation prohibited | Stop (Undefined) |
| Data Transfer Controller (DTC) | Selectable | Stop (Retained) | Selectable | Stop (Undefined) |
| Watchdog Timer (WDT) | Selectable*1 | Stop (Retained) | Stop (Retained) | Stop (Undefined) |
| Independent Watchdog Timer (IWDT) | Selectable*1 | Selectable*1 | Selectable*1 | Stop (Undefined) |
| Asynchronous General Purpose Timer (AGTn (n = 0, 1)) | Selectable | Selectable*12 | Selectable*12 | Stop (Undefined) |
| 12-Bit A/D Converter (ADC) | Selectable | Stop (Retained) | Operation prohibited | Stop (Undefined) |
| Programmable Gain Amplifiers (PGAs) | Selectable*13 | Stop (Retained) | Selectable*13 | Stop (Undefined) |
| 12-Bit D/A Converter (DAC12) | Selectable | Stop (Retained) | Selectable | Stop (Undefined) |
| Data Operation Circuit (DOC) | Selectable | Stop (Retained) | Selectable | Stop (Undefined) |
| Serial Communications Interface (SCI0) | Selectable | Stop (Retained) | Selectable (RXD0 falling edge is available, to enter snooze mode) (only in asynchronous mode).*5 | Stop (Undefined) |
| Serial Communications Interface (SCIn (n = 1 to 4, 9)) | Selectable | Stop (Retained) | Operation prohibited | Stop (Undefined) |
| I2C Bus Interface (IIC0) | Selectable | Selectable*3 | Selectable*3 Only wakeup interrupt is available. | Stop (Undefined) |
| I2C Bus Interface (IIC1) | Selectable | Stop (Retained) | Operation prohibited | Stop (Undefined) |
| Event Link Controller (ELC) | Selectable | Stop (Retained) | Selectable*6 | Stop (Undefined) |
| High-Speed Analog Comparator (ACMPHSn, n = 0 to 3) | Selectable | Stop (Retained) | Selectable VCOUT function only.*9 | Stop (Undefined) |
| IRQn (n = 0 to 15) pin interrupt | Selectable | Selectable | Selectable | Stop (Undefined) |
| NMI, IRQn-DS (n = 0 to 15) pin interrupt | Selectable | Selectable | Selectable | Selectable |
| Key Interrupt Function (KINT) | Selectable | Selectable | Selectable | Stop (Undefined) |
| Low voltage detection (LVD) | Selectable | Selectable | Selectable | Selectable*10 |
| Power-on reset circuit | Operating | Operating | Operating | Operating*11 |
| Other peripheral modules | Selectable | Stop (Retained) | Operation prohibited | Stop (Undefined) |
| I/O Ports | Operating | Retained | Operating | Retained |

Note: Selectable means that operating or not operating can be selected by the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.
Stop (Undefined) means that the contents of the internal registers are undefined and power to the internal circuit is cut off.
All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode. In order to avoid increase in power consumption in Snooze mode, module-stop bit of modules which are unnecessary in Snooze mode must be set to 1 before entering Software Standby mode.

Note 1. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in Option Function Select Register 0 (OFS0) in WDT auto start mode.Power consumption can be reduced in Normal and Sleep modes by selecting an appropriate operating power control mode according to the operating frequency.
Note 2. Stopped when the clock output source select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO).
Note 3. IIC0 wakeup interrupt is available.
Note 4. When using SCI0 in Snooze mode, MOSCCR.MOSTP and PLLCR.PLLSTP and PLL2CR.PLL2STP bits must be 1.
Note 5. Serial communication modes of SCI0 is only in asynchronous mode.
Note 6. Event lists the restrictions described in section 10.10.13. ELC Events in Snooze Mode.
Note 7. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the oscillator status is the same as before entering Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the oscillator stops when the MCU enters Deep Software Standby mode.
Note 8. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, data in the Standby SRAM is retained in Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, data in the Standby SRAM is undefined in Deep Software Standby mode.
Note 9. Only VCOUT function is permitted. The VCOUT pin operates when ACMPHS uses no digital filter. For details on digital filter, see section 39, High-Speed Analog Comparator (ACMPHS).
Note 10. When using LVD in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] bits must be 00b or 01b before entering Deep Software Standby mode.
Note 11. When the MCU enters Deep Software Standby mode with the DPSBYCR.DEEPCUT[1:0] bits set to 11b, the LVD circuit stops and the low-power function of the power-on reset circuit is enabled.
Note 12. AGT0 operation is possible when 100b (AGTLCLK) is selected by the AGT0.AGTMR1.TCK[2:0] bits. AGT1 operation is possible when 100b (AGTLCLK) or 101 (Underflow event signal from AGT0) is selected by the AGT1.AGTMR1.TCK[2:0] bits.
Note 13. When using the Programmable Gain Amplifiers, MSTPD16 must be set to 0. For details, see section 36.3.13. Programmable Gain Amplifier.

No.13 was removed, and No.14 was updated and moved up to No. 13.

Table 10.3 Interrupt Source for canceling Snooze, Software Standby and Deep Software Standby Modes

| Interrupt source | Name | Software Standby mode | Snooze mode | Deep Software Standby mode |
|---|---|---|---|---|
| NMI | | Yes | Yes | Yes |
| Port | PORT_IRQn (n = 0 to 15) | Yes | Yes | Yes*3 |
| LVD | LVD_LVD1 | Yes | Yes | Yes |
| | LVD_LVD2 | Yes | Yes | Yes |
| IWDT | IWDT_NMIUNDF | Yes | Yes | No |
| KINT | KEY_INTKR | Yes | Yes | No |
| AGT1 | AGT1_AGTI | Yes | Yes*2 | No |
| | AGT1_AGTCMAI | Yes | Yes | No |
| | AGT1_AGTCMBI | Yes | Yes | No |
| IIC0 | IIC0_WU | Yes | Yes | No |
| ~~ADC~~ | ~~ADC_CCMPM0~~ | ~~No~~ | ~~Yes with SELSR0*1 *2~~ | ~~No~~ |
| | ~~ADC_CCMPM1~~ | ~~No~~ | ~~Yes with SELSR0*1 *2~~ | ~~No~~ |
| SCI0 | SCI0_AM | No | Yes with SELSR0*1 | No |
| DTC | DTC_COMPLETE | No | Yes with SELSR0*1 *2 | No |
| DOC | DOC_DOPCI | No | Yes with SELSR0 *1 | No |

Note 1. To use the interrupt request as a trigger for exiting the Snooze mode, the request must be selected in SELSR0 . See section 12, Interrupt Controller Unit (ICU) for the setting of SELSR0. When a trigger selected in SELSR0 occurs after executing WFI instruction and during the transition from Normal mode to Software Standby mode, the request might or might not be accepted, depending on the timing of the occurrence.
Note 2. The event which is enabled by the SNZEDCR0 must not be used.
Note 3. IRQn-DS pin interrupt is available. IRQn pin interrupt is not available.

10.2.11 SNZEDCR0 : Snooze End Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x094

| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SCI0UMTED | - | - | - | - | DTCNZRED | DTCZRED | AGTUNFED |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Function | R/W |
|---|---|---|---|
| 0 | AGTUNFED | AGT1 Underflow Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |
| 1 | DTCZRED | Last DTC Transmission Completion Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |
| 2 | DTCNZRED | Not Last DTC Transmission Completion Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |
| 3 | - | This bit is read as 0. The write value should be 0. | R/W |
| 4 | - | This bit is read as 0. The write value should be 0. | R/W |
| 5 | - | This bit is read as 0. The write value should be 0. | R/W |
| 6 | - | This bit is read as 0. The write value should be 0. | R/W |
| 7 | SCI0UMTED | SCI0 Address Mismatch Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZEDCR0 register controls the condition of switching from Snooze mode to Software Standby mode. In order to use a trigger shown in Table 10.8 as a condition to switch from Snooze mode to Software Standby mode, the corresponding bitin the SNZEDCR0 register must be set to 1.

The event that is used to return from snooze mode to normal mode as shown in Table 10.3 must not be enabled in the SNZEDCR0 register.

**AGTUNFED bit (AGT1 Underflow Snooze End Enable)**
The AGTUNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AGT1 underflow. For details on the trigger conditions, see section 23, Low Power Asynchronous General Purpose Timer (AGTW).

**DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)**
The DTCZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of the last DTC transmission, that is, when CRA or CRB registers in the DTC is 0. For details on the trigger conditions, see section 16, Data Transfer Controller (DTC).

**DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)**
The DTCNZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of each DTC transmission, that is, when CRA or CRB registers in the DTC is not 0. For details on the trigger conditions, see section 16, Data Transfer Controller (DTC).

~~**AD0MATED bit (ADC Compare Match 0 Snooze End Enable)**~~
~~The AD0MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC event when a conversion result matches the expected data. For details on the trigger conditions, see section 36, 12-Bit A/D Converter (ADC).~~

~~**AD1MATED bit (ADC Compare Match 1 Snooze End Enable)**~~
~~The AD1MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC event when a conversion result matches the expected data. For details on the trigger conditions, see section 36, 12-Bit A/D Converter (ADC).~~

**SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)**
The SCI0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an SCI0 event when an address received in Software Standby mode does not match the expected data. For details on the trigger conditions, see section 26, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 operates in asynchronous mode.

### 10.8.3 Returning from Snooze Mode to Software Standby Mode

Table 10.8 shows the snooze end request that can be used as triggers to return to Software Standby mode. The snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are ignored. When multiple requests are selected, each of the requests invokes transition to Software Standby mode from Snooze mode.

Table 10.9 shows the snooze end conditions that consist of the snooze end requests and the conditions of the peripheral modules. The SCI0 ~~, ADC,~~ and DTC modules can keep the MCU in Snooze mode until they complete the operation. However, an AGTn (n = 1) underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of SCI0 operation.

Figure 10.7 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to which snooze end requests are set in the SNZEDCR0 register. A snooze request is cleared automatically after returning to Software Standby mode.

Table 10.8 Available snooze end requests (triggers to return to Software Standby mode)

| **Peripheral Module** | **Snooze end request** | **Enable/Disable Control** | |
|---|---|---|---|
| | | **Register** | **Bit** |
| AGT1 | AGT1 underflow (AGT1_AGTI) | SNZEDCR0 | AGTUNFED |
| DTC | Last DTC transmission completion (DTC_COMPLETE) | SNZEDCR0 | DTCZRED |
| DTC | Not Last DTC Transmission Completion (DTC_TRANSFER) | SNZEDCR0 | DTCNZRED |
| ~~ADC~~ | ~~Composite compare match 0 (ADC_CCMPM0)~~ | ~~SNZEDCR0~~ | ~~AD0MATED~~ |
| ~~ADC~~ | ~~Composite compare match 1 (ADC_CCMPM1)~~ | ~~SNZEDCR0~~ | ~~AD1MATED~~ |
| SCI0 | SCI0 address mismatch (SCI0_DCUF) | SNZEDCR0 | SCI0UMTED |

Table 10.9 Snooze end conditions

| **Operating module when a snooze end request occurs** | **Snooze end request** | |
|---|---|---|
| | **AGT1 underflow** | **Other than AGT1 underflow** |
| DTC<br>~~ADC~~ | The MCU transitions to the Software Standby mode after DTC ~~and ADC~~ complete operation. | The MCU transitions to the Software Standby mode after DTC, ~~ADC,~~ and SCI0 complete the operation. |
| SCI0 | The MCU transitions to the Software Standby mode immediately after the snooze end request is generated. | |
| Other than specified | The MCU transitions to the Software Standby mode immediately after a snooze end request is generated. | |

Note: If the DTC is used to activate the ~~ADC, or~~ SCI, the MCU transitions to Software Standby mode immediately after a snooze end request is generated.

~~10.10.12 Conditions of A/D Conversion Start in Snooze Mode~~
~~ADC can only be triggered by the ELC in Snooze mode. Do not use software trigger or ADTRGn (n = 0, 1) pin.~~

10.10.13 ELC Events in Snooze Mode
This section lists available ELC events in Snooze mode. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ~~ADC Composite compare match 0 (ADC_CCMPM0)~~
- ~~ADC Composite compare match 1 (ADC_CCMPM1)~~
- Data operation circuit interrupt (DOC_DOPCI).

Table 12.4 Event table (7 of 9)

| Event number | Interrupt request source | Name | IELSRn | | DELSRn | Canceling Snooze | Canceling Software Standby | Canceling Deep Software Standby |
|---|---|---|---|---|---|---|---|---|
| | | | Connect to NVIC | Invoke DTC | Invoke DMAC | | | |
| 0x157 | ADC | ADC_LIMCLPI | ✓ | — | — | — | — | — |
| 0x158 | | ADC_FIFOOVF | ✓ | — | — | — | — | — |
| 0x159 | | ADC_ADI0 | ✓ | ✓ | ✓ | — | — | — |
| 0x15A | | ADC_ADI1 | ✓ | ✓ | ✓ | — | — | — |
| 0x15B | | ADC_ADI2 | ✓ | ✓ | ✓ | — | — | — |
| 0x15C | | ADC_CMPI0 | ✓ | — | — | — | — | — |
| 0x15D | | ADC_CMPI1 | ✓ | — | — | — | — | — |
| 0x15E | | ADC_CCMPM0 | ✓ | ✓ | ✓ | — | — | — |
| 0x160 | | ADC_ERR0 | ✓ | — | — | — | — | — |
| 0x161 | | ADC_RESOVF0 | ✓ | — | — | — | — | — |
| 0x163 | | ADC_CALEND0 | ✓ | — | — | — | — | — |
| 0x164 | | ADC_FIFOREQ0 | ✓ | ✓ | ✓ | — | — | — |
| 0x165 | | ADC_FIFOREQ1 | ✓ | ✓ | ✓ | — | — | — |
| 0x166 | | ADC_FIFOREQ2 | ✓ | ✓ | ✓ | — | — | — |
| 0x167 | | ADC_ADI3 | ✓ | ✓ | ✓ | — | — | — |
| 0x168 | | ADC_ADI4 | ✓ | ✓ | ✓ | — | — | — |
| 0x169 | | ADC_ADI5678 | ✓ | ✓ | ✓ | — | — | — |
| 0x16A | | ADC_CMPI2 | ✓ | — | — | — | — | — |
| 0x16B | | ADC_CMPI3 | ✓ | — | — | — | — | — |
| 0x16C | | ADC_CCMPM1 | ✓ | ✓ | ✓ | — | — | — |
| 0x16E | | ADC_ERR1 | ✓ | — | — | — | — | — |
| 0x16F | | ADC_RESOVF1 | ✓ | — | — | — | — | — |
| 0x171 | | ADC_CALEND1 | ✓ | — | — | — | — | — |
| 0x172 | | ADC_FIFOREQ3 | ✓ | ✓ | ✓ | — | — | — |
| 0x173 | | ADC_FIFOREQ4 | ✓ | ✓ | ✓ | — | — | — |
| 0x174 | | ADC_FIFOREQ5678 | ✓ | ✓ | ✓ | — | — | — |
| 0x18D | SCI0 | SCI0_RXI | ✓ | ✓ | ✓ | — | — | — |
| 0x18E | | SCI0_TXI | ✓ | ✓ | ✓ | — | — | — |
| 0x18F | | SCI0_TEI | ✓ | — | — | — | — | — |
| 0x190 | | SCI0_ERI | ✓ | — | — | — | — | — |
| 0x191 | | SCI0_AED | ✓ | — | — | — | — | — |
| 0x192 | | SCI0_BFD | ✓ | — | — | — | — | — |
| 0x193 | | SCI0_AM | ✓ | — | — | ✓*1 | — | — |
| 0x195 | SCI1 | SCI1_RXI | ✓ | ✓ | ✓ | — | — | — |
| 0x196 | | SCI1_TXI | ✓ | ✓ | ✓ | — | — | — |
| 0x197 | | SCI1_TEI | ✓ | — | — | — | — | — |
| 0x198 | | SCI1_ERI | ✓ | — | — | — | — | — |
| 0x199 | | SCI1_AED | ✓ | — | — | — | — | — |
| 0x19A | | SCI1_BFD | ✓ | — | — | — | — | — |
| 0x19B | | SCI1_AM | ✓ | — | — | — | — | — |

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (5 of 6)

| Event number | Interrupt request source | Name | Description |
|---|---|---|---|
| 0x140 | IIC0 | IIC0_RX | Rx Data buffer full |
| 0x141 | | IIC0_TX | Tx Data buffer empty |
| 0x142 | | IIC0_TEND | Transmit end |
| 0x145 | | IIC0_COM | Communication event |
| 0x146 | IIC1 | IIC1_RX | Rx Data buffer full |
| 0x147 | | IIC1_TX | Tx Data buffer empty |
| 0x148 | | IIC1_TEND | Transmit end |
| 0x14A | | IIC1_COM | Communication event |
| 0x159 | ADC | ADC_ADI0 | A/D scan end for scan group 0 |
| 0x15A | | ADC_ADI1 | A/D scan end for scan group 1 |
| 0x15B | | ADC_ADI2 | A/D scan end for scan group 2 |
| 0x15E | | ADC_CCMPM0 | Composite compare match 0 |
| 0x167 | | ADC_ADI3 | A/D scan end for scan group 3 |
| 0x168 | | ADC_ADI4 | A/D scan end for scan group 4 |
| 0x169 | | ADC_ADI5678 | A/D scan end for scan group 5 to 8 |
| 0x16C | | ADC_CCMPM1 | Composite compare match 1 |
| 0x18D | SCI0 | SCI0_RXI*4 | Receive data full |
| 0x18E | | SCI0_TXI*4 | Transmit data empty |
| 0x18F | | SCI0_TEI*4 | Transmit end |
| 0x190 | | SCI0_ERI | Receive error |
| 0x191 | | SCI0_AED | Effective edge detection |
| 0x193 | | SCI0_AM | Address match event |
| 0x195 | SCI1 | SCI1_RXI*4 | Received data full |
| 0x196 | | SCI1_TXI*4 | Transmit data empty |
| 0x197 | | SCI1_TEI*4 | Transmit end |
| 0x198 | | SCI1_ERI | Receive error |
| 0x199 | | SCI1_AED | Effective edge detection |
| 0x19B | | SCI1_AM | Address match event |
| 0x19C | SCI2 | SCI2_RXI*4 | Received data full |
| 0x19D | | SCI2_TXI*4 | Transmit data empty |
| 0x19E | | SCI2_TEI*4 | Transmit end |
| 0x19F | | SCI2_ERI | Receive error |
| 0x1A0 | | SCI2_AED | Effective edge detection |
| 0x1A2 | | SCI2_AM | Address match event |
| 0x1A3 | SCI3 | SCI3_RXI*4 | Received data full |
| 0x1A4 | | SCI3_TXI*4 | Transmit data empty |
| 0x1A5 | | SCI3_TEI*4 | Transmit end |
| 0x1A6 | | SCI3_ERI | Receive error |
| 0x1A7 | | SCI3_AED | Effective edge detection |
| 0x1A9 | | SCI3_AM | Address match event |

[Original]

Table 10.2 Operating conditions of each low power mode (2 of 2)

| Item | Sleep mode | Software Standby mode | Snooze mode | Deep Software Standby mode |
|---|---|---|---|---|
| DMA Controller (DMAC) | Selectable | Stop (Retained) | Operation prohibited | Stop (Undefined) |
| Data Transfer Controller (DTC) | Selectable | Stop (Retained) | Selectable | Stop (Undefined) |
| Watchdog Timer (WDT) | Selectable*1 | Stop (Retained) | Stop (Retained) | Stop (Undefined) |
| Independent Watchdog Timer (IWDT) | Selectable*1 | Selectable*1 | Selectable*1 | Stop (Undefined) |
| Asynchronous General Purpose Timer (AGTn (n = 0, 1)) | Selectable | Selectable*12 | Selectable*12 | Stop (Undefined) |
| 12-Bit A/D Converter (ADC) | Selectable | Stop (Retained) | Selectable*13 | Stop (Undefined) |
| Programmable Gain Amplifiers (PGAs) | Selectable*14 | Stop (Retained) | Selectable*14 | Stop (Undefined) |
| 12-Bit D/A Converter (DAC12) | Selectable | Stop (Retained) | Selectable | Stop (Undefined) |
| Data Operation Circuit (DOC) | Selectable | Stop (Retained) | Selectable | Stop (Undefined) |
| Serial Communications Interface (SCI0) | Selectable | Stop (Retained) | Selectable (RXD0 falling edge is available, to enter snooze mode) (only in asynchronous mode).*5 | Stop (Undefined) |
| Serial Communications Interface (SCIn (n = 1 to 4, 9)) | Selectable | Stop (Retained) | Operation prohibited | Stop (Undefined) |
| I2C Bus Interface (IIC0) | Selectable | Selectable*3 | Selectable*3 Only wakeup interrupt is available. | Stop (Undefined) |
| I2C Bus Interface (IIC1) | Selectable | Stop (Retained) | Operation prohibited | Stop (Undefined) |
| Event Link Controller (ELC) | Selectable | Stop (Retained) | Selectable*6 | Stop (Undefined) |
| High-Speed Analog Comparator (ACMPHSn, n = 0 to 3) | Selectable | Stop (Retained) | Selectable VCOUT function only.*9 | Stop (Undefined) |
| IRQn (n = 0 to 15) pin interrupt | Selectable | Selectable | Selectable | Stop (Undefined) |
| NMI, IRQn-DS (n = 0 to 15) pin interrupt | Selectable | Selectable | Selectable | Selectable |
| Key Interrupt Function (KINT) | Selectable | Selectable | Selectable | Stop (Undefined) |
| Low voltage detection (LVD) | Selectable | Selectable | Selectable | Selectable*10 |
| Power-on reset circuit | Operating | Operating | Operating | Operating*11 |
| Other peripheral modules | Selectable | Stop (Retained) | Operation prohibited | Stop (Undefined) |
| I/O Ports | Operating | Retained | Operating | Retained |

Note: Selectable means that operating or not operating can be selected by the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.
Stop (Undefined) means that the contents of the internal registers are undefined and power to the internal circuit is cut off.
All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode. In order to avoid increase in power consumption in Snooze mode, module-stop bit of modules which are unnecessary in Snooze mode must be set to 1 before entering Software Standby mode.

Note 1. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in Option Function Select Register 0 (OFS0) in WDT auto start mode.Power consumption can be reduced in Normal and Sleep modes by selecting an appropriate operating power control mode according to the operating frequency.
Note 2. Stopped when the clock output source select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO).
Note 3. IIC0 wakeup interrupt is available.
Note 4. When using SCI0 in Snooze mode, MOSCCR.MOSTP and PLLCR.PLLSTP and PLL2CR.PLL2STP bits must be 1.
Note 5. Serial communication modes of SCI0 is only in asynchronous mode.
Note 6. Event lists the restrictions described in section 10.10.13. ELC Events in Snooze Mode.
Note 7. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the oscillator status is the same as before entering Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the oscillator stops when the MCU enters Deep Software Standby mode.
Note 8. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, data in the Standby SRAM is retained in Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, data in the Standby SRAM is undefined in Deep Software Standby mode.
Note 9. Only VCOUT function is permitted. The VCOUT pin operates when ACMPHS uses no digital filter. For details on digital filter, see section 39, High-Speed Analog Comparator (ACMPHS).
Note 10. When using LVD in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] bits must be 00b or 01b before entering Deep Software Standby mode.
Note 11. When the MCU enters Deep Software Standby mode with the DPSBYCR.DEEPCUT[1:0] bits set to 11b, the LVD circuit stops and the low-power function of the power-on reset circuit is enabled.
Note 12. AGT0 operation is possible when 100b (AGTLCLK) is selected by the AGT0.AGTMR1.TCK[2:0] bits. AGT1 operation is possible when 100b (AGTLCLK) or 101 (Underflow event signal from AGT0) is selected by the AGT1.AGTMR1.TCK[2:0] bits.
Note 13. When using the 12-bit A/D Converter in Snooze mode, the ADCMPENR.CMPENn bits must be 1. (The precautions for using the 12-Bit A/D Converter in snooze mode are determined after evaluation.)
Note 14. When using the Programmable Gain Amplifiers, MSTPD16 must be set to 0. For details, see section 36.3.13. Programmable Gain Amplifier. (The precautions for using the PGAs are determined after evaluation.)

Table 10.3 Interrupt Source for canceling Snooze, Software Standby and Deep Software Standby Modes

| Interrupt source | Name | Software Standby mode | Snooze mode | Deep Software Standby mode |
|---|---|---|---|---|
| NMI | | Yes | Yes | Yes |
| Port | PORT_IRQn (n = 0 to 15) | Yes | Yes | Yes*3 |
| LVD | LVD_LVD1 | Yes | Yes | Yes |
| | LVD_LVD2 | Yes | Yes | Yes |
| IWDT | IWDT_NMIUNDF | Yes | Yes | No |
| KINT | KEY_INTKR | Yes | Yes | No |
| AGT1 | AGT1_AGTI | Yes | Yes*2 | No |
| | AGT1_AGTCMAI | Yes | Yes | No |
| | AGT1_AGTCMBI | Yes | Yes | No |
| IIC0 | IIC0_WU | Yes | Yes | No |
| ADC | ADC_CCMPM0 | No | Yes with SELSR0*1 *2 | No |
| | ADC_CCMPM1 | No | Yes with SELSR0*1 *2 | No |
| SCI0 | SCI0_AM | No | Yes with SELSR0*1 | No |
| DTC | DTC_COMPLETE | No | Yes with SELSR0*1 *2 | No |
| DOC | DOC_DOPCI | No | Yes with SELSR0 *1 | No |

Note 1. To use the interrupt request as a trigger for exiting the Snooze mode, the request must be selected in SELSR0 . See section 12, Interrupt Controller Unit (ICU) for the setting of SELSR0. When a trigger selected in SELSR0 occurs after executing WFI instruction and during the transition from Normal mode to Software Standby mode, the request might or might not be accepted, depending on the timing of the occurrence.
Note 2. The event which is enabled by the SNZEDCR0 must not be used.
Note 3. IRQn-DS pin interrupt is available. IRQn pin interrupt is not available.

10.2.11 SNZEDCR0 : Snooze End Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x094

| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SCI0UMTED | - | AD1MATED | - | AD0MATED | DTCNZRED | DTCZRED | AGTUNFED |
| Value after reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Function | R/W |
|---|---|---|---|
| 0 | AGTUNFED | AGT1 Underflow Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |
| 1 | DTCZRED | Last DTC Transmission Completion Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |
| 2 | DTCNZRED | Not Last DTC Transmission Completion Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |
| 3 | AD0MATED | ADC Compare Match 0 Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |
| 4 | - | This bit is read as 0. The write value should be 0. | R/W |
| 5 | AD1MATED | ADC Compare Match 1 Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |
| 6 | - | This bit is read as 0. The write value should be 0. | R/W |
| 7 | SCI0UMTED | SCI0 Address Mismatch Snooze End Enable<br>0: Disable the snooze end request<br>1: Enable the snooze end request | R/W |

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZEDCR0 register controls the condition of switching from Snooze mode to Software Standby mode. In order to use a trigger shown in Table 10.8 as a condition to switch from Snooze mode to Software Standby mode, the corresponding bitin the SNZEDCR0 register must be set to 1.

The event that is used to return from snooze mode to normal mode as shown in Table 10.3 must not be enabled in the SNZEDCR0 register.

**AGTUNFED bit (AGT1 Underflow Snooze End Enable)**
The AGTUNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AGT1 underflow. For details on the trigger conditions, see section 23, Low Power Asynchronous General Purpose Timer (AGTW).

**DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)**
The DTCZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of the last DTC transmission, that is, when CRA or CRB registers in the DTC is 0. For details on the trigger conditions, see section 16, Data Transfer Controller (DTC).

**DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)**
The DTCNZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of each DTC transmission, that is, when CRA or CRB registers in the DTC is not 0. For details on the trigger conditions, see section 16, Data Transfer Controller (DTC).

**AD0MATED bit (ADC Compare Match 0 Snooze End Enable)**
The AD0MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC event when a conversion result matches the expected data. For details on the trigger conditions, see section 36, 12-Bit A/D Converter (ADC).

**AD1MATED bit (ADC Compare Match 1 Snooze End Enable)**
The AD1MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC event when a conversion result matches the expected data. For details on the trigger conditions, see section 36, 12-Bit A/D Converter (ADC).

**SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)**
The SCI0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an SCI0 event when an address received in Software Standby mode does not match the expected data. For details on the trigger conditions, see section 26, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 operates in asynchronous mode.

### 10.8.3 Returning from Snooze Mode to Software Standby Mode

Table 10.8 shows the snooze end request that can be used as triggers to return to Software Standby mode. The snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are ignored. When multiple requests are selected, each of the requests invokes transition to Software Standby mode from Snooze mode.
Table 10.9 shows the snooze end conditions that consist of the snooze end requests and the conditions of the peripheral modules. The SCI0, ADC, and DTC modules can keep the MCU in Snooze mode until they complete the operation. However, an AGTn (n = 1) underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of SCI0 operation.
Figure 10.7 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to which snooze end requests are set in the SNZEDCR0 register. A snooze request is cleared automatically after returning to Software Standby mode.

Table 10.8 Available snooze end requests (triggers to return to Software Standby mode)

| Peripheral Module | Snooze end request | Enable/Disable Control | |
|---|---|---|---|
| | | Register | Bit |
| AGT1 | AGT1 underflow (AGT1_AGTI) | SNZEDCR0 | AGTUNFED |
| DTC | Last DTC transmission completion (DTC_COMPLETE) | SNZEDCR0 | DTCZRED |
| DTC | Not Last DTC Transmission Completion (DTC_TRANSFER) | SNZEDCR0 | DTCNZRED |
| ADC | Composite compare match 0 (ADC_CCMPM0) | SNZEDCR0 | AD0MATED |
| ADC | Composite compare match 1 (ADC_CCMPM1) | SNZEDCR0 | AD1MATED |
| SCI0 | SCI0 address mismatch (SCI0_DCUF) | SNZEDCR0 | SCI0UMTED |

Table 10.9 Snooze end conditions

| Operating module when a snooze end request occurs | Snooze end request | |
|---|---|---|
| | AGT1 underflow | Other than AGT1 underflow |
| DTC<br>ADC | The MCU transitions to the Software Standby mode after DTC and ADC complete operation. | The MCU transitions to the Software Standby mode after DTC, ADC, and SCI0 complete the operation. |
| SCI0 | The MCU transitions to the Software Standby mode immediately after the snooze end request is generated. | |
| Other than specified | The MCU transitions to the Software Standby mode immediately after a snooze end request is generated. | |

Note: If the DTC is used to activate the ADC, or SCI, the MCU transitions to Software Standby mode immediately after a snooze end request is generated.

10.10.12 Conditions of A/D Conversion Start in Snooze Mode
ADC can only be triggered by the ELC in Snooze mode. Do not use software trigger or ADTRGn (n = 0, 1) pin.

10.10.13 ELC Events in Snooze Mode
This section lists available ELC events in Snooze mode. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC Composite compare match 0 (ADC_CCMPM0)
- ADC Composite compare match 1 (ADC_CCMPM1)
- Data operation circuit interrupt (DOC_DOPCI).

Table 12.4 Event table (7 of 9)

| Event number | Interrupt request source | Name | IELSRn | | DELSRn | Canceling Snooze | Canceling Software Standby | Canceling Deep Software Standby |
|---|---|---|---|---|---|---|---|---|
| | | | Connect to NVIC | Invoke DTC | Invoke DMAC | | | |
| 0x157 | ADC | ADC_LIMCLPI | ✓ | — | — | — | — | — |
| 0x158 | | ADC_FIFOOVF | ✓ | — | — | — | — | — |
| 0x159 | | ADC_ADI0 | ✓ | ✓ | ✓ | — | — | — |
| 0x15A | | ADC_ADI1 | ✓ | ✓ | ✓ | — | — | — |
| 0x15B | | ADC_ADI2 | ✓ | ✓ | ✓ | — | — | — |
| 0x15C | | ADC_CMPI0 | ✓ | — | — | — | — | — |
| 0x15D | | ADC_CMPI1 | ✓ | — | — | — | — | — |
| 0x15E | | ADC_CCMPM0 | ✓ | ✓ | ✓ | ✓*1 | — | — |
| 0x160 | | ADC_ERR0 | ✓ | — | — | — | — | — |
| 0x161 | | ADC_RESOVF0 | ✓ | — | — | — | — | — |
| 0x163 | | ADC_CALEND0 | ✓ | — | — | — | — | — |
| 0x164 | | ADC_FIFOREQ0 | ✓ | ✓ | ✓ | — | — | — |
| 0x165 | | ADC_FIFOREQ1 | ✓ | ✓ | ✓ | — | — | — |
| 0x166 | | ADC_FIFOREQ2 | ✓ | ✓ | ✓ | — | — | — |
| 0x167 | | ADC_ADI3 | ✓ | ✓ | ✓ | — | — | — |
| 0x168 | | ADC_ADI4 | ✓ | ✓ | ✓ | — | — | — |
| 0x169 | | ADC_ADI5678 | ✓ | ✓ | ✓ | — | — | — |
| 0x16A | | ADC_CMPI2 | ✓ | — | — | — | — | — |
| 0x16B | | ADC_CMPI3 | ✓ | — | — | — | — | — |
| 0x16C | | ADC_CCMPM1 | ✓ | ✓ | ✓ | ✓*1 | — | — |
| 0x16E | | ADC_ERR1 | ✓ | — | — | — | — | — |
| 0x16F | | ADC_RESOVF1 | ✓ | — | — | — | — | — |
| 0x171 | | ADC_CALEND1 | ✓ | — | — | — | — | — |
| 0x172 | | ADC_FIFOREQ3 | ✓ | ✓ | ✓ | — | — | — |
| 0x173 | | ADC_FIFOREQ4 | ✓ | ✓ | ✓ | — | — | — |
| 0x174 | | ADC_FIFOREQ5678 | ✓ | ✓ | ✓ | — | — | — |
| 0x18D | SCI0 | SCI0_RXI | ✓ | ✓ | ✓ | — | — | — |
| 0x18E | | SCI0_TXI | ✓ | ✓ | ✓ | — | — | — |
| 0x18F | | SCI0_TEI | ✓ | — | — | — | — | — |
| 0x190 | | SCI0_ERI | ✓ | — | — | — | — | — |
| 0x191 | | SCI0_AED | ✓ | — | — | — | — | — |
| 0x192 | | SCI0_BFD | ✓ | — | — | — | — | — |
| 0x193 | | SCI0_AM | ✓ | — | — | ✓*1 | — | — |
| 0x195 | SCI1 | SCI1_RXI | ✓ | ✓ | ✓ | — | — | — |
| 0x196 | | SCI1_TXI | ✓ | ✓ | ✓ | — | — | — |
| 0x197 | | SCI1_TEI | ✓ | — | — | — | — | — |
| 0x198 | | SCI1_ERI | ✓ | — | — | — | — | — |
| 0x199 | | SCI1_AED | ✓ | — | — | — | — | — |
| 0x19A | | SCI1_BFD | ✓ | — | — | — | — | — |
| 0x19B | | SCI1_AM | ✓ | — | — | — | — | — |

Table 17.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (5 of 6)

| Event number | Interrupt request source | Name | Description |
|---|---|---|---|
| 0x140 | IIC0 | IIC0_RX | Rx Data buffer full |
| 0x141 | | IIC0_TX | Tx Data buffer empty |
| 0x142 | | IIC0_TEND | Transmit end |
| 0x145 | | IIC0_COM | Communication event |
| 0x146 | IIC1 | IIC1_RX | Rx Data buffer full |
| 0x147 | | IIC1_TX | Tx Data buffer empty |
| 0x148 | | IIC1_TEND | Transmit end |
| 0x14A | | IIC1_COM | Communication event |
| 0x159 | ADC | ADC_ADI0 | A/D scan end for scan group 0 |
| 0x15A | | ADC_ADI1 | A/D scan end for scan group 1 |
| 0x15B | | ADC_ADI2 | A/D scan end for scan group 2 |
| 0x15E | | ADC_CCMPM0*2 | Composite compare match 0 |
| 0x167 | | ADC_ADI3 | A/D scan end for scan group 3 |
| 0x168 | | ADC_ADI4 | A/D scan end for scan group 4 |
| 0x169 | | ADC_ADI5678 | A/D scan end for scan group 5 to 8 |
| 0x16C | | ADC_CCMPM1*2 | Composite compare match 1 |
| 0x18D | SCI0 | SCI0_RXI*4 | Receive data full |
| 0x18E | | SCI0_TXI*4 | Transmit data empty |
| 0x18F | | SCI0_TEI*4 | Transmit end |
| 0x190 | | SCI0_ERI | Receive error |
| 0x191 | | SCI0_AED | Effective edge detection |
| 0x193 | | SCI0_AM | Address match event |
| 0x195 | SCI1 | SCI1_RXI*4 | Received data full |
| 0x196 | | SCI1_TXI*4 | Transmit data empty |
| 0x197 | | SCI1_TEI*4 | Transmit end |
| 0x198 | | SCI1_ERI | Receive error |
| 0x199 | | SCI1_AED | Effective edge detection |
| 0x19B | | SCI1_AM | Address match event |
| 0x19C | SCI2 | SCI2_RXI*4 | Received data full |
| 0x19D | | SCI2_TXI*4 | Transmit data empty |
| 0x19E | | SCI2_TEI*4 | Transmit end |
| 0x19F | | SCI2_ERI | Receive error |
| 0x1A0 | | SCI2_AED | Effective edge detection |
| 0x1A2 | | SCI2_AM | Address match event |
| 0x1A3 | SCI3 | SCI3_RXI*4 | Received data full |
| 0x1A4 | | SCI3_TXI*4 | Transmit data empty |
| 0x1A5 | | SCI3_TEI*4 | Transmit end |
| 0x1A6 | | SCI3_ERI | Receive error |
| 0x1A7 | | SCI3_AED | Effective edge detection |
| 0x1A9 | | SCI3_AM | Address match event |