The descriptions of CSnCR.EXENB bit is corrected.

15. Buses
15.3 Register Descriptions
15.3.1 CSn Control Register (CSnCR) (n = 0 to 7)

[Before]

EXENB bit (Operation Enable)
The EXENB bit enables operation of the associated CS area. On MCU reset, operation is enabled (EXENB = 1) only for area 0. Operation in other areas is disabled (EXENB = 0). Attempts to access disabled areas have no effect.

When the CSC and SDRAMC are in use at the same time, BCLK and SDCLK must operate at the same frequency.

[After]

EXENB bit (Operation Enable)
The EXENB bit enables operation of the associated CS area. On MCU reset, operation is enabled (EXENB = 1) only for area 0. Operation in other areas is disabled (EXENB = 0). Attempts to access disabled areas have no effect.

When the CSC and SDRAMC are in use at the same time, BCLK and SDCLK must operate at the same frequency.

When using the CS0 to CS3 pin function and the EBCLK pin function, set the SDCKOCR.SDCKOEN bit to 0 to stop the output of the SDRAM clock (SDCLK).