Date: Jun. 12, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0082A/E	Rev.	1.00
Title	RA6E2 Group, RA4E2 Group, correction of specifications for ID code protection.		Information Category	Technical Notification		
Applicable Product	RA6E2 Group RA4E2 Group	Lot No. All	Reference Document	RA6E2 Group User's Manual Hardware Rev.1.10 RA4E2 Group User's Manual Hardware Rev.1.10		

The description of operations on connection with the programmer or on-chip debugger of specifications for ID code protection in the Option-Setting Memory, Flash Memory, and Security Features chapters are corrected.

1. Correction of Option-Setting Memory chapter

[before]

Table Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI/USB/SWD boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (all bytes are 0xFF)	Protection disabled	Connection to programmer or on-chip debugger is permitted. The connection to the programmer does not check the ID code, the ID code always matches, and the connection to the programmer is permitted. The on-chip debugger needs to send 0xFF, …, 0xFF (All bytes = 0xFF) on connection.
	Bit [127] = 1 and bit [126] = 1, and at least one of the 16 bytes is not 0xFF.	Protection enabled	Matching ID code = authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code = transition to the ID code protection wait state. When the ID code sent from the programmer or the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased except permanently block protection area and setting of PBPS register. However, forced erasure is not executed when the FSPR bit is 0.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code = authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code = transition to the ID code protection wait state. Renesas cannot access the test mode.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, the connection to the programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

[after]

Table Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI/USB/SWD boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (all bytes are 0xFF)	Protection disabled	Connection to programmer or on-chip debugger is permitted. The connection to the programmer does not check the ID code, the ID code always matches, and the connection to the programmer is permitted. The on-chip debugger needs to send 0xFF, …, 0xFF (All bytes = 0xFF) on connection.
	Bit [127] = 1 and bit [126] = 1, and at least one of the 16 bytes is not 0xFF.	Protection enabled	Matching ID code = authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code = transition to the ID code protection wait state. When the ID code sent from the programmer or the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased ~~except permanently block protection area and setting of PBPS register~~. However, forced erasure is not executed when the FSPR bit is 0 or there is a block with permanent block protection.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code = authentication is complete and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code = transition to the ID code protection wait state. Renesas cannot access the test mode.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, the connection to the programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

2. Correction of Flash Memory chapter

[before]

Table Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI/USB/SWD boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (All bytes = 0xFF)	Protection disabled	Connection to programmer or on-chip debugger is permitted. The connection to the programmer does not check the ID code, the ID code always matches, and the connection to the programmer is permitted. The on-chip debugger needs to send 0xFF, …, 0xFF (All bytes = 0xFF) on connection.
	Bit [127] = 1, Bit [126] = 1, and at least one of the 16 bytes is not 0xFF	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is “ALeRASE” in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the content of the user flash area is erased except permanently block protection area and setting of PBPS register. However, forced erasure is not executed when the SAS.FSPR[*1] bit is 0.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. Renesas cannot access the test mode.
	Bit [127] = 0	Protection enabled	ID code validation is not performed, the ID code is always mismatching, and connection to the programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

[after]

Table Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI/USB/SWD boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (All bytes = 0xFF)	Protection disabled	Connection to programmer or on-chip debugger is permitted. The connection to the programmer does not check the ID code, the ID code always matches, and the connection to the programmer is permitted. The on-chip debugger needs to send 0xFF, …, 0xFF (All bytes = 0xFF) on connection.
	Bit [127] = 1, Bit [126] = 1, and at least one of the 16 bytes is not 0xFF	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is “ALeRASE” in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the content of the user flash area is erased ~~except permanently block protection area and setting of PBPS register~~. However, forced erasure is not executed when the SAS.FSPR[*1] bit is 0 or there is a block with permanent block protection.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. Renesas cannot access the test mode.
	Bit [127] = 0	Protection enabled	ID code validation is not performed, the ID code is always mismatching, and connection to the programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

3. Correction of Security Features chapter

[before]

Table Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI/USB/SWD boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (All bytes = 0xFF)	Protection disabled	Connection to programmer or on-chip debugger is permitted. The connection to the programmer does not check the ID code, the ID code always matches, and the connection to the programmer is permitted. The on-chip debugger needs to send 0xFF, …, 0xFF (All bytes = 0xFF) or needs to send nothing on connection.
	Bit [127] = 1, Bit [126] = 1, and at least one of the 16 bytes is not 0xFF	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is “ALeRASE” in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased. However, forced erasure is not executed when the SAS.FSPR*1 bit is 0.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. Renesas cannot access the test mode.
	Bit [127] = 0	Protection enabled	ID code validation is not performed, the ID code is always mismatching, and connection to the programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

[after]

Table Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI/USB/SWD boot mode) On-chip debug mode (SWD boot mode)	0xFF, …, 0xFF (All bytes = 0xFF)	Protection disabled	Connection to programmer or on-chip debugger is permitted. The connection to the programmer does not check the ID code, the ID code always matches, and the connection to the programmer is permitted. The on-chip debugger needs to send 0xFF, …, 0xFF (All bytes = 0xFF) or needs to send nothing on connection.
	Bit [127] = 1, Bit [126] = 1, and at least one of the 16 bytes is not 0xFF	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is “ALeRASE” in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased. However, forced erasure is not executed when the SAS.FSPR*1 bit is 0 or there is a block with permanent block protection.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or the on-chip debugger is permitted. Mismatching ID code: Additional transition to the ID code protection waiting state. Renesas cannot access the test mode.
	Bit [127] = 0	Protection enabled	ID code validation is not performed, the ID code is always mismatching, and connection to the programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.