Date: Oct. 7, 2021

# RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

| Product Category | MPU/MCU | | Document No. | TN-RA*-A0039A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | RA6E1 Group, correction of Pin list and IO ports | | Information Category | Technical Notification | | |
| Applicable Product | RA6E1 Group | Lot No.<br>All | Reference Document | RA6E1 Group User's Manual Hardware Rev.1.00 | | |

The descriptions of Pin list and IO ports are corrected.

[before] page 66

**1. Overview**

**1.7 Pin Lists**

**Table 1.15 Pin list (1 of 3)**

| LQFP100 | LQFP64 | QFN48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI/SSIE/SDHI/MMC/ EHTERC(RMII) | GPT/AGT/RTC | ADC12/DAC12 |
|---|---|---|---|---|---|---|---|---|
| 7 | — | — | — | P406 | | SSIRXD0_A/RMII0_TXD1_B | GTIOC1B/AGTO5 | — |
| 16 | — | — | CACREF | P708 | IRQ11 | RXD1/SSLB3_B | — | — |
| 32 | 23 | — | CLKOUT | P205 | IRQ1-DS | TXD4/CTS9_RTS9/SCL1_B/SSLA0_A/USB_OVRCURA-DS/ SD0DAT3_A/ET0_WOL | GTIOC4A/AGTO1 | — |

[after]

**Table 1.15 Pin list (1 of 3)**

| LQFP100 | LQFP64 | QFN48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI/SSIE/SDHI/MMC/ EHTERC(RMII) | GPT/AGT/RTC | ADC12/DAC12 |
|---|---|---|---|---|---|---|---|---|
| 7 | — | — | — | P406 | | SSLA3_C/SSIRXD0_A/RMII0_TXD1_B | GTIOC1B/AGTO5 | — |
| 16 | — | — | CACREF | P708 | IRQ11 | RXD1/SSLB3_B/AUDIO_CLK | — | — |
| 32 | 23 | — | CLKOUT | P205 | IRQ1-DS | TXD4/CTS9_RTS9/SCL1_B/SSLA0_A/USB_OVRCURA-DS/ SSILRCK0/SD0DAT3_A/ET0_WOL | GTIOC4A/AGTO1 | — |

[before] page 67

**Table 1.15 Pin list (2 of 3)**

| LQFP100 | LQFP64 | QFN48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI/SSIE/SDHI/MMC/ EHTERC(RMII) | GPT/AGT/RTC | ADC12/DAC12 |
|---|---|---|---|---|---|---|---|---|
| 75 | 48 | 36 | — | P100 | IRQ2 | RXD0/SCK1/MISOB_A/QSPCLK/OM_SCLK | GTETRGA/GTIOC5B/AGTIO0 | — |
| 76 | 49 | 37 | CACREF | P500 | — | CTS5/USB_VBUSEN/QSPCLK | AGTOA0 | — |

[after]

**Table 1.15 Pin list (2 of 3)**

| LQFP100 | LQFP64 | QFN48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI/SSIE/SDHI/MMC/ EHTERC(RMII) | GPT/AGT/RTC | ADC12/DAC12 |
|---|---|---|---|---|---|---|---|---|
| 75 | 48 | 36 | — | P100 | IRQ2 | RXD0/SCK1/MISOB_A/QSPCLK~~/OM_SCLK~~ | GTETRGA/GTIOC5B/AGTIO0 | — |
| 76 | 49 | 37 | CACREF | P500 | — | ~~CTS5~~USB_VBUSEN/QSPCLK | AGTOA0 | — |

[before] page 464

## 19. I/O Ports

### 19.6 Peripheral Select Settings for Each Product

**Table 19.6 Register settings for input/output pin function (PORT1) (1 of 2)**

| PSEL[4:0] settings | Function | pin | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P100 | P101 | P102 | P103 | P104 | P105 | P106 | P107 | P108 | P109 | P110 | P111 | P112 | P113 | P114 | P115 |
| 00000b (value after reset) | Hi-Z/ JTAG/SW D | Hi-Z | | | | | | | | TMS/ SWDIO | TDO/S WO | TDI | Hi-Z | | | | |
| 00001b | AGT | AGTIO 0 | AGTEE 0 | AGTO0 | AGTIO 2 | AGTEE 2 | AGTO2 | AGTOB 0 | AGTOA 0 | AGTOA 3 | AGTOB 3 | AGTEE 3 | AGTOA 5 | AGTOB 5 | AGTEE 5 | AGTIO 5 | — |
| 00010b | GPT*2 | GTETR GA | GTETR GB | GTOW LO | GTOW UP | GTETR GB | GTETR GA | — | — | GTOUL O | GTOVU P | GTOVL O | — | — | — | — | — |
| 00011b | GPT*2 | GTIOC 5B | GTIOC 5A | — | — | GTIOC 1B | GTIOC 1A | — | — | GTIOC 0B | GTIOC 1A | GTIOC 1B | — | — | — | — | GTIOC 4A |
| 00100b | SCI | RXD0/ MISO0/ SCL0 | TXD0/ MOSI0/ SDA0 | SCK0 | CTS0_ RTS0/ SS0 | RXD8/ MISO8/ SCL8 | TXD8/ MOSI8/ SDA8 | SCK8 | CTS8_ RTS8/ SS8 | — | — | CTS2_ RTS2/ SS2 | SCK2 | TXD2/ MOSI2/ SDA2/ TXDX2/ SIOX2 | RXD2/ MISO2/ SCL2/ RXDX2 | — | — |
| 00101b | SCI | SCK1 | CTS1_ RTS1/ SS1 | — | — | — | — | — | — | CTS9_ RTS9/ SS9 | TXD9/ MOSI9/ SDA9 | RXD9/ MISO9/ SCL9 | SCK9 | SCK1 | — | CTS9 | — |
| 00110b | SPI*1 | MISOB _A | MOSIB _A | RSPCK B_A | SSLB0 _A | SSLB1 _A | SSLB2 _A | SSLB3 _A | — | SSLA0 _B | MOSIA _B | MISOA _B | RSPCK A_B | SSLA0 _B | — | — | — |
| 01001b | CLKOUT/ RTC | — | — | — | — | — | — | — | — | — | CLKOU T | — | — | — | — | — | — |
| 01010b | CAC/ ADC12 | — | — | ADTRG 0 | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 10000b | CAN | — | — | CRX0 | CTX0 | — | — | — | — | — | CTX1 | CRX1 | — | — | — | — | — |

[after]

**Table 19.6 Register settings for input/output pin function (PORT1) (1 of 2)**

| PSEL[4:0] settings | Function | pin | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P100 | P101 | P102 | P103 | P104 | P105 | P106 | P107 | P108 | P109 | P110 | P111 | P112 | P113 | P114 | P115 |
| 00000b (value after reset) | Hi-Z/ JTAG/SWD | Hi-Z | | | | | | | | TMS/ SWDIO | TDO/SWO | TDI | Hi-Z | | | | |
| 00001b | AGT | AGTIO0 | AGTEE0 | AGTO0 | AGTIO2 | AGTEE2 | AGTO2 | AGTOB0 | AGTOA0 | AGTOA3 | AGTOB3 | AGTEE3 | AGTOA5 | AGTOB5 | AGTEE5 | AGTIO5 | — |
| 00010b | GPT*2 | GTETRGA | GTETRGB | — | — | GTETRGB | GTETRGA | — | — | — | — | — | — | — | — | — | — |
| 00011b | GPT*2 | GTIOC5B | GTIOC5A | GTIOC2B | GTIOC2A | GTIOC1B | GTIOC1A | — | — | — | GTIOC1A | GTIOC1B | — | — | GTIOC2A | GTIOC2B | GTIOC4A |
| 00100b | SCI | RXD0/ MISO0/ SCL0 | TXD0/ MOSI0/ SDA0 | SCK0 | CTS0_ RTS0/ SS0 | — | — | — | — | — | — | CTS2_ RTS2/ SS2 | SCK2 | TXD2/ MOSI2/ SDA2/ TXDX2/ SIOX2 | RXD2/ MISO2/ SCL2/ RXDX2 | — | — |
| 00101b | SCI | SCK1 | CTS1_ RTS1/ SS1 | — | — | — | — | — | — | CTS9_ RTS9/ SS9 | TXD9/ MOSI9/ SDA9 | RXD9/ MISO9/ SCL9 | SCK9 | SCK1 | — | CTS9 | — |
| 00110b | SPI*1 | MISOB_A | MOSIB_A | RSPCKB_A | SSLB0_A | SSLB1_A | SSLB2_A | SSLB3_A | — | SSLA0_B | MOSIA_B | MISOA_B | RSPCKA_B | SSLA0_B | — | — | — |
| 01001b | CLKOUT/ RTC | — | — | — | — | — | — | — | — | — | CLKOUT | — | — | — | — | — | — |
| 01010b | CAC/ ADC12 | — | — | ADTRG0 | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 10000b | CAN | — | — | CRX0 | CTX0 | — | — | — | — | — | — | — | — | — | — | — | — |

[before] page 465

**Table 19.7 Register settings for input/output pin function (PORT2)**

| PSEL[4:0] settings | Function | Pin | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P200*4 | P201 | P205 | P206 | P207 | P208 | P209 | P210 | P211 | P212 | P213 | P214 |
| 00000b (value after reset) | Hi-Z/ JTAG/SWD | Hi-Z | | | | | | | | | | | |
| 00001b | AGT | — | — | AGTO1 | — | — | — | AGTEE5 | AGTOB5 | AGTOA5 | AGTEE1 | AGTEE2 | AGTO5 |
| 00010b | GPT*2 | — | — | GTIV | GTIU | — | GTOVLO | GTOVUP | GTIW | GTIV | GTETRGD | GTETRGC | GTIU |
| 00011b | GPT*2 | — | — | GTIOC4A | — | — | — | — | — | — | GTIOC0B | GTIOC0A | — |
| 00100b | SCI | — | — | TXD4/ MOSI4/ SDA4 | RXD4/ MISO4/ SCL4 | TXD4/ MOSI4/ SDA4 | — | — | — | — | — | — | — |
| 00101b | SCI | — | — | CTS9_RTS9/ SS9 | CTS9 | — | — | — | — | — | RXD1/ MISO1/ SCL1/ RXDX1 | TXD1/ MOSI1/ SDA1/ TXDX1/ SIOX1 | — |
| 00110b | SPI*1 | — | — | SSLA0_A | SSLA1_A | SSLA2_A | — | — | — | — | — | — | — |
| 00111b | IIC*1 | — | — | SCL1_B | SDA1_B | — | — | — | — | — | — | — | — |
| 01001b | CLKOUT/ RTC | — | — | CLKOUT | — | — | — | — | — | — | — | — | — |
| 01010b | CAC/ADC12 | — | — | — | — | — | — | — | — | — | — | ADTRG1 | — |

[after]

**Table 19.7 Register settings for input/output pin function (PORT2)**

| PSEL[4:0] settings | Function | Pin | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P200*4 | P201 | P205 | P206 | P207 | P208 | P209 | P210 | P211 | P212 | P213 | P214 |
| 00000b (value after reset) | Hi-Z/ JTAG/SWD | Hi-Z | | | | | | | | | | | |
| 00001b | AGT | — | — | AGTO1 | — | — | — | AGTEE5 | AGTOB5 | AGTOA5 | AGTEE1 | AGTEE2 | AGTO5 |
| 00010b | GPT*2 | — | — | — | — | — | — | — | — | — | — | — | — |
| 00011b | GPT*2 | — | — | GTIOC4A | — | — | — | — | — | — | — | — | — |
| 00100b | SCI | — | — | TXD4/ MOSI4/ SDA4 | RXD4/ MISO4/ SCL4 | TXD4/ MOSI4/ SDA4 | — | — | — | — | — | — | — |
| 00101b | SCI | — | — | CTS9_RTS9/ SS9 | CTS9 | — | — | — | — | — | RXD1/ MISO1/ SCL1/ ~~RXDX1~~ | TXD1/ MOSI1/ SDA1/ ~~TXDX1~~ ~~SIOX1~~ | — |
| 00110b | SPI*1 | — | — | SSLA0_A | SSLA1_A | SSLA2_A | — | — | — | — | — | — | — |
| 00111b | IIC*1 | — | — | SCL1_B | SDA1_B | — | — | — | — | — | — | — | — |
| 01001b | CLKOUT/ RTC | — | — | CLKOUT | — | — | — | — | — | — | — | — | — |
| 01010b | CAC/ADC12 | — | — | — | — | — | — | — | — | — | — | — | — |

[before] page 466

**Table 19.8 Register settings for input/output pin function (PORT3)**

| PSEL[4:0] settings | Function | Pin | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | P300 | P301 | P302 | P303 | P304 | P305 | P306 | P307 |
| 00000b (value after reset) | Hi-Z/JTAG/SWD | TCK/SWCLK | Hi-Z | | | | | | |
| 00001b | AGT | — | AGTIO0 | — | — | AGTEE2 | AGTOB2 | AGTOA2 | AGTEE4 |
| 00010b | GPT*2 | GTOUUP | GTOULO | GTOUUP | — | GTOWLO | GTOWUP | GTOULO | GTOUUP |
| 00011b | GPT*2 | GTIOC0A | GTIOC4B | GTIOC4A | GTIOC7B | GTIOC7A | — | — | — |
| 00100b | SCI | — | RXD2/MISO2/SCL2/ RXDX2 | TXD2/MOSI2/ SDA2/TXDX2/ SIOX2 | — | RXD6/MISO6/ SCL6 | TXD6/MOSI6/ SDA6 | SCK6 | CTS6_RTS6/ SS6 |

[after]

**Table 19.8 Register settings for input/output pin function (PORT3)**

| PSEL[4:0] settings | Function | Pin | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | P300 | P301 | P302 | P303 | P304 | P305 | P306 | P307 |
| 00000b (value after reset) | Hi-Z/JTAG/SWD | TCK/SWCLK | Hi-Z | | | | | | |
| 00001b | AGT | — | AGTIO0 | — | — | AGTEE2 | AGTOB2 | AGTOA2 | AGTEE4 |
| 00010b | GPT*2 | — | — | — | — | — | — | — | — |
| 00011b | GPT*2 | — | GTIOC4B | GTIOC4A | GTIOC7B | GTIOC7A | — | — | — |
| 00100b | SCI | — | RXD2/MISO2/SCL2/ RXDX2 | TXD2/MOSI2/ SDA2/TXDX2/ SIOX2 | — | — | — | — | — |

[before] page 466

**Table 19.9 Register settings for input/output pin function (PORT4) (1 of 2)**

| PSEL[4:0] settings | Function | pin | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P400 | P401 | P402 | P403 | P404 | P405 | P406 | P407 | P408 | P409 | P410 | P411 | P412 | P413 | P414 | P415 |
| 00000b (value after reset) | Hi-Z/ JTAG/SWD | Hi-Z | | | | | | | | | | | | | | | |
| 00001b | AGT | AGTIO1 | — | — | — | — | — | AGTO5 | AGTIO0 | AGTOB2 | AGTOA2 | AGTOB1 | AGTOA1 | AGTEE1 | AGTEE3 | AGTIO5 | AGTIO4 |
| 00010b | GPT*3 | — | GTETRGA | — | — | — | — | — | — | GTOWLO | GTOWUP | GTOVLO | GTOVUP | GTOULO | GTOUUP | — | — |
| 00011b | GPT*3 | GTIOC6A | GTIOC6B | — | — | — | GTIOC1A | GTIOC1B | GTIOC6A | GTIOC6B | — | — | — | — | — | GTIOC0B | GTIOC0A |
| 00100b | SCI | SCK4 | CTS4_ RTS4/ SS4 | CTS4 | — | — | — | — | CTS4_ RTS4/ SS4 | CTS4 | — | RXD0/ MISO0/ SCL0 | TXD0/ MOSI0/ SDA0 | SCK0 | CTS0_ RTS0/ SS0 | CTS0 | — |
| 00101b | SCI | SCK7 | TXD7/ MOSI7/ SDA7 | RXD7/ MISO7/ SCL7 | CTS7_ RTS7/ SS7 | CTS7 | — | — | — | RXD3/ MISO3/ SCL3 | TXD3/ MOSI3/ SDA3 | SCK3 | CTS3_ RTS3/ SS3 | CTS3 | — | — | — |
| 00110b | SPI*2 | — | — | — | — | — | — | SSLA3_C | SSLA3_A | — | — | MISOB_B | MOSIB_B | RSPCKB_B | SSLB0_B | SSLB1_B | SSLB2_B |
| 00111b | IIC*2 | SCL0_A | SDA0_A | — | — | — | — | — | SDA0_B | SCL0_B | — | — | — | — | — | — | — |
| 01001b | CLKOUT/ RTC | — | — | — | — | — | — | — | RTCOUT | — | — | — | — | — | — | — | — |
| 01010b | CAC/ ADC12 | ADTRG1 | — | CACREF | — | — | — | — | ADTRG0 | — | — | — | — | — | — | — | — |
| 10000b | CAN | — | CTX0 | CRX0 | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 10010b | SSIE*2 | AUDIO_CLK | — | AUDIO_CLK | SSIBCK0_A | SSILRCK0/SSIFS0_A | SSITXD0_A | SSIRXD0_A | — | — | — | — | — | — | — | — | — |
| 10011b | USBFS | — | — | — | — | — | — | — | USB_VBUS | USB_ID | USB_EXICEN | — | — | — | — | — | USB_VBUSEN |

[after]

**Table 19.9 Register settings for input/output pin function (PORT4) (1 of 2)**

| PSEL[4:0] settings | Function | pin | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P400 | P401 | P402 | P403 | P404 | P405 | P406 | P407 | P408 | P409 | P410 | P411 | P412 | P413 | P414 | P415 |
| 00000b (value after reset) | Hi-Z/ JTAG/SWD | Hi-Z | | | | | | | | | | | | | | | |
| 00001b | AGT | AGTIO1 | — | — | — | — | — | AGTO5 | AGTIO0 | AGTOB2 | AGTOA2 | AGTOB1 | AGTOA1 | AGTEE1 | AGTEE3 | AGTIO5 | AGTIO4 |
| 00010b | GPT*3 | — | GTETRGA | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 00011b | GPT*3 | GTIOC6A | GTIOC6B | — | — | — | GTIOC1A | GTIOC1B | GTIOC6A | GTIOC6B | — | — | — | — | — | — | — |
| 00100b | SCI | SCK4 | CTS4_ RTS4/ SS4 | CTS4 | — | — | — | — | CTS4_ RTS4/ SS4 | CTS4 | — | RXD0/ MISO0/ SCL0 | TXD0/ MOSI0/ SDA0 | SCK0 | CTS0_ RTS0/ SS0 | CTS0 | — |
| 00101b | SCI | — | — | — | — | — | — | — | — | RXD3/ MISO3/ SCL3 | TXD3/ MOSI3/ SDA3 | SCK3 | CTS3_ RTS3/ SS3 | CTS3 | — | — | — |
| 00110b | SPI*2 | — | — | — | — | — | — | SSLA3_C | SSLA3_A | — | — | MISOB_B | MOSIB_B | RSPCKB_B | SSLB0_B | SSLB1_B | SSLB2_B |
| 00111b | IIC*2 | SCL0_A | SDA0_A | — | — | — | — | — | SDA0_B | SCL0_B | — | — | — | — | — | — | — |
| 01001b | CLKOUT/ RTC | — | — | — | — | — | — | — | RTCOUT | — | — | — | — | — | — | — | — |
| 01010b | CAC/ ADC12 | — | — | CACREF | — | — | — | — | ADTRG0 | — | — | — | — | — | — | — | — |
| 10000b | CAN | — | CTX0 | CRX0 | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 10010b | SSIE*2 | AUDIO_CLK | — | AUDIO_CLK | SSIBCK0_A | SSILRCK0/SSIFS0_A | SSITXD0_A | SSIRXD0_A | — | — | — | — | — | — | — | — | — |
| 10011b | USBFS | — | — | — | — | — | — | — | USB_VBUS | USB_ID | USB_EXICEN | — | — | — | — | — | USB_VBUSEN |

[before] page 467

**Table 19.10 Register settings for input/output pin function (PORT5)**

| PSEL[4:0] settings | Function | pin | | | | | |
|---|---|---|---|---|---|---|---|
| | | P500 | P501 | P502 | P503 | P504 | P505 |
| 00000b (value after reset) | Hi-Z/JTAG/SWD | Hi-Z | | | | | |
| 00001b | AGT | AGTOA0 | AGTOB0 | AGTOA2 | AGTOB2 | AGTOA3 | AGTOB3 |
| 00010b | GPT*1 | GTIU | GTIV | GTIW | GTETRGC | GTETRGD | — |
| 00011b | GPT*1 | — | — | — | — | — | — |
| 00100b | SCI | — | — | CTS6 | CTS6_RTS6/ SS6 | SCK6 | RXD6/MISO6/ SCL6 |
| 00101b | SCI | CTS5 | TXD5/MISO5/ SDA5 | RXD5/MISO5/ SCL5 | SCK5 | CTS5_RTS5/S S5 | — |
| 00111b | IIC | — | — | — | — | — | — |
| 01010b | CAC/ADC12 | CACREF | — | — | — | — | — |
| 10000b | CAN | — | — | — | — | — | — |
| 10001b | QSPI | QSPCLK | QSSL | QIO0 | QIO1 | QIO2 | QIO3 |
| 10011b | USBFS | USB_VBUSEN | USB_OVRCURA | USB_OVRCURB | USB_EXICEN | USB_ID | — |
| ASEL bit | | AN116 | AN117 | AN118 | AN119 | AN120 | AN121 |
| ISEL bit | | — | IRQ11 | IRQ12 | — | — | IRQ14 |
| DSCR[1:0] bits | Drive capacity control | L/M/H | L/M/H | L/M/H | L/M/H | L/M/H | L/M/H |
| NCODR bit | N-ch open-drain | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| PCR bit | Pull-up | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 100 pins product | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 64 pins product | | ✓ | — | — | — | — | — |
| 48 pins product | | ✓ | — | — | — | — | — |

[after]

**Table 19.10 Register settings for input/output pin function (PORT5)**

| PSEL[4:0] settings | Function | pin | | | | | |
|---|---|---|---|---|---|---|---|
| | | P500 | P501 | P502 | P503 | P504 | P505 |
| 00000b (value after reset) | Hi-Z/JTAG/SWD | Hi-Z | | | | | |
| 00001b | AGT | AGTOA0 | AGTOB0 | AGTOA2 | AGTOB2 | AGTOA3 | AGTOB3 |
| 00010b | GPT*1 | — | — | — | GTETRGC | GTETRGD | — |
| 00011b | GPT*1 | — | — | — | — | — | — |
| 00100b | SCI | — | — | — | — | — | — |
| 00101b | SCI | — | — | — | — | — | — |
| 00111b | IIC | — | — | — | — | — | — |
| 01010b | CAC/ADC12 | CACREF | — | — | — | — | — |
| 10000b | CAN | — | — | — | — | — | — |
| 10001b | QSPI | QSPCLK | QSSL | QIO0 | QIO1 | QIO2 | QIO3 |
| 10011b | USBFS | USB_VBUSEN | USB_OVRCURA | USB_OVRCURB | USB_EXICEN | USB_ID | — |
| ASEL bit | | — | — | — | — | — | — |
| ISEL bit | | — | IRQ11 | IRQ12 | — | — | IRQ14 |
| DSCR[1:0] bits | Drive capacity control | L/M/H | L/M/H | L/M/H | L/M/H | L/M/H | L/M/H |
| NCODR bit | N-ch open-drain | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| PCR bit | Pull-up | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 100 pins product | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 64 pins product | | ✓ | — | — | — | — | — |
| 48 pins product | | ✓ | — | — | — | — | — |

[before] page 468

**Table 19.11 Register settings for input/output pin function (PORT6)**

| PSEL[4:0] settings | Function | Pin | | | | | |
|---|---|---|---|---|---|---|---|
| | | P600 | P601 | P602 | P608 | P609 | P610 |
| 00000b (value after reset) | Hi-Z/JTAG/SWD | Hi-Z | | | | | |
| 00001b | AGT | AGTIO3 | AGTEE3 | AGTO3 | — | AGTO5 | AGTO4 |
| 00011b | GPT | GTIOC6B | GTIOC6A | GTIOC7B | GTIOC4B | GTIOC5A | GTIOC5B |
| 00100b | SCI | — | — | — | — | — | — |
| 00101b | SCI | SCK9 | RXD9/MISO9/SCL9 | TXD9/MOSI9/SDA9 | — | — | CTS7 |
| 01001b | CLKOUT/RTC | CLKOUT | — | — | — | — | — |
| 01010b | CAC/ADC12 | CACREF | — | — | — | — | — |
| 10000b | CAN | — | — | — | — | CTX1 | CRX1 |

[After]

**Table 19.11 Register settings for input/output pin function (PORT6)**

| PSEL[4:0] settings | Function | Pin | | | | | |
|---|---|---|---|---|---|---|---|
| | | P600 | P601 | P602 | P608 | P609 | P610 |
| 00000b (value after reset) | Hi-Z/JTAG/SWD | Hi-Z | | | | | |
| 00001b | AGT | AGTIO3 | AGTEE3 | AGTO3 | — | AGTO5 | AGTO4 |
| 00011b | GPT | GTIOC6B | GTIOC6A | GTIOC7B | GTIOC4B | GTIOC5A | GTIOC5B |
| 00100b | SCI | — | — | — | — | — | — |
| 00101b | SCI | SCK9 | RXD9/MISO9/SCL9 | TXD9/MOSI9/SDA9 | — | — | — |
| 01001b | CLKOUT/RTC | CLKOUT | — | — | — | — | — |
| 01010b | CAC/ADC12 | CACREF | — | — | — | — | — |
| 10000b | CAN | — | — | — | — | — | — |

[before] page 468

**Table 19.12 Register settings for input/output pin function (PORT7)**

| PSEL[4:0] settings | Function | Pin |
|---|---|---|
| | | P708 |
| 00000b (value after reset) | Hi-Z/JTAG/SWD | Hi-Z |
| 00001b | AGT | — |
| 00011b | GPT*1 | — |
| 00101b | SCI | RXD1/MISO1/SCL1/RXDX1/SCL1 |

[after]

**Table 19.12 Register settings for input/output pin function (PORT7)**

| PSEL[4:0] settings | Function | Pin |
|---|---|---|
| | | P708 |
| 00000b (value after reset) | Hi-Z/JTAG/SWD | Hi-Z |
| 00001b | AGT | — |
| 00011b | GPT*1 | — |
| 00101b | SCI | ~~RXD1/~~MISO1/SCL1/RXDX1/SCL1 |