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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0040A/E	Rev.	1.00
Title	RA6E1 Group, correction of General PWM Timer (GPT)		Information Category	Technical Notification		
Applicable Product	RA6E1 Group	Lot No. All	Reference Document	RA6E1 Group User's Manual Hardware Rev.1.00		

The descriptions of General PWM Timer (GPT) are corrected.

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1. Overview

1.1 Function Outline

Table 1.7 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 2 channels and a 16-bit timer with GPT16 × 4 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 21, General PWM Timer (GPT).

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18. Event Link Controller (ELC)

18.2.3 ELSRn : Event Link Setting Register n (n = 0 to 9, 12, 14 to 17)

Table 18.3 Association between event signal names set in ELSRn .ELS[8:0] bits and signal numbers (4 of 5)

Event number	Interrupt request source	Name	Description
0x0FF	GPT7	GPT7_CCMPA	Compare match A
0x100		GPT7_CCMPB	Compare match B
0x101		GPT7_CMPC	Compare match C
0x102		GPT7_CMPD	Compare match D
0x103		GPT7_CMPE	Compare match E
0x104		GPT7_CMPF	Compare match F
0x105		GPT7_OVF	Overflow
0x106		GPT7_UDF	Underflow
0x150	GPT	GPT_UVWEDGE	UVW edge event

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20. Port Output Enable for GPT (POEG)

20.3 Output-Disable Control Operation

If any of the following conditions is satisfied, the GTIOCxA, GTIOCxB, and the 3-phase PWM output for BLDC motor control pins can be set to output-disable:

- Input level or edge detection of the GTETRGn pins

  When POEGGn.PIDE is 1, the POEGGn.PIDF flag is set to 1.

- Output-disable request from the GPT

  When POEGGn.IOCE is 1, the POEGGn.IOCF flag is set to 1 if the disable request is enabled by GTINTAD. The GTINTAD.GRPABH and GTINTAD.GRPABL settings apply to the group selected by the GPT register GTINTAD.GRP[1:0] or OPSCR.GRP[1:0].

- Oscillation stop detection for the clock generation circuit

  While POEGGn.OSTPE is 1, the halt status of the main clock oscillator is detected and the POEGGn. OSTPF flag is set to 1.

● SSF bit setting

When POEGGn.SSF is set to 1, the PWM output is disabled.

The output-disable state is controlled in the GPT module. The output-disable of the GTIOCxA and GTIOCxB pins is set in the GTINTAD.GRP[1:0], GTIOR.OADF[1:0], and GTIOR.OBDF[1:0] bits in GPTx. The output-disable of the 3-phase PWM output for BLDC motor control pins is set in the OPSCR.GRP[1:0] bits and OPSCR.GODF bit in GPT_OPS.

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● Output-disable request from the GPT

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21. General PWM Timer (GPT)

21.1 Overview

The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 2 channels and a 16-bit timer with GPT16 × 4 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.

Table 21.1 lists the GPT specifications, Table 21.2 shows the GPT functions, and Figure 21.1 shows a block diagram.

Table 21.1 GPT specifications

Parameter	Description
Functions	• 32 bits × 2 channels (GPT32n (n = 1, 2)) • 16 bits × 4 channels (GPT16m (m = 4 to 7)) • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow • Generation of dead times in PWM operation • Synchronous starting, stopping and clearing counters for arbitrary channels • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 8 ELC events • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to the status of two input pins • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 4 external triggers • Output pin disable function by detected short-circuits between output pins • PWM waveform for controlling brushless DC motors can be generated • Compare match A to F event, overflow/underflow event, and input UVW edge event can be output to the ELC • Enables the noise filter for input capture and input UVW • Period count function • Logical operation between the channel output • Bus clock: PCLKA, Core clock: PCLKD • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64)

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Table 21.2 GPT functions (2 of 2)

Parameter	Description
DMAC/DTC activation	All the interrupt sources
Brushless DC motor control function	Available
Interrupt sources	9 sources • GTCCRA comare match/input capture(GPTn_CCMPA) • GTCCRB comare match/input capture(GPTn_CCMPB) • GTCCRC comare match(GPTn_CMPC) • GTCCRD comare match(GPTn_CMPD)

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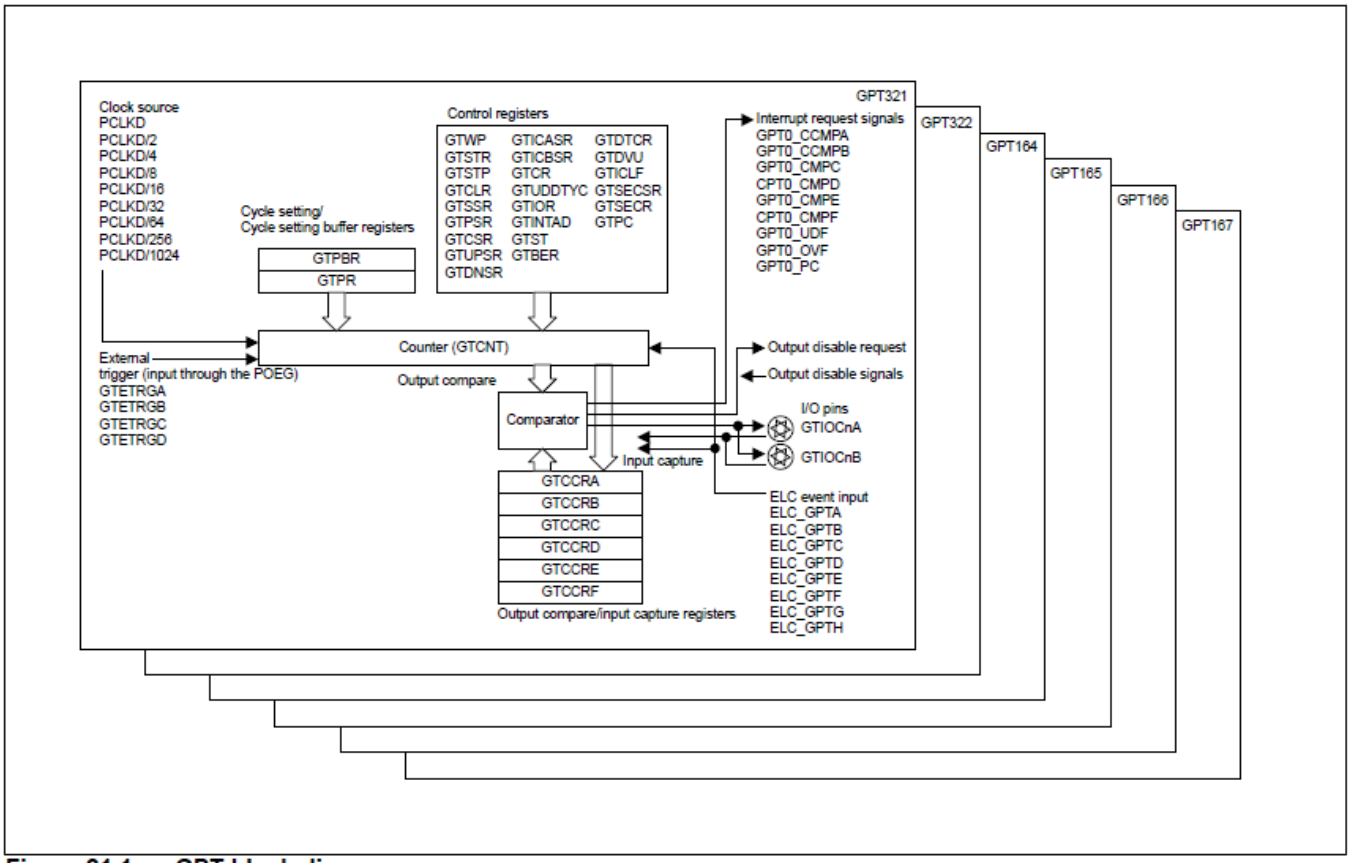

Figure 21.1 GPT block diagram

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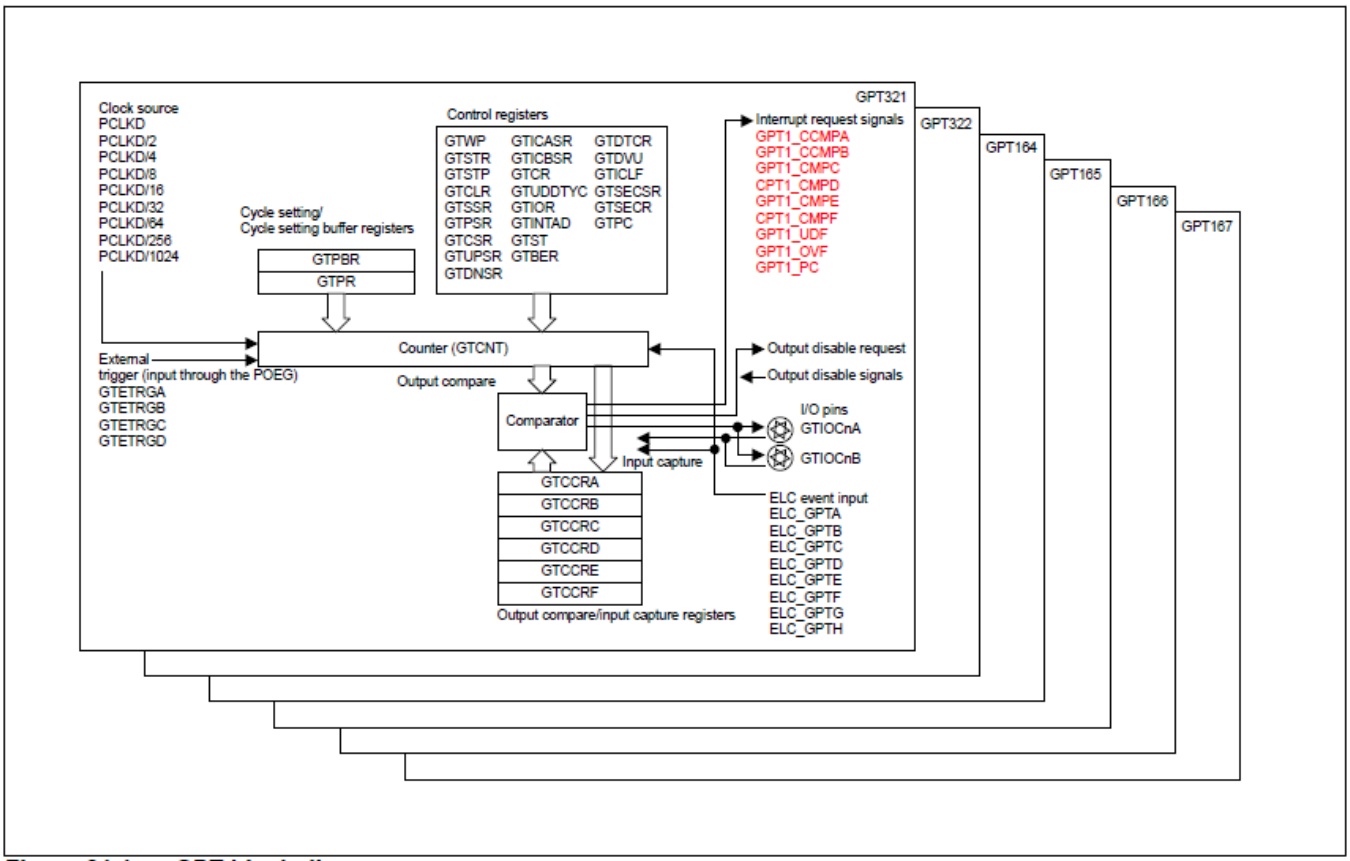

Figure 21.1 GPT block diagram

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21.2.27 GTSECR : General PWM Timer Operation Enable Bit Simultaneous Control Register

The GTSECR register simultaneously updates the value for operation enable bits of a channel set by the GTSECSR register. Writing 1 to a bit in the GTSECR register in any channel and updating it updates an operation enable bit for all channels, related to the position of the bit written with 1 by the all GTSECSR registers.

The GTSECR register of channel which security attribution is configured as secure can not be written by non-secure access. For example, if GPT0 is configured as secure and other GPTs are configured as non-secure, the GPT0.GTSECR register cannot be written by non-secure access to GPT1.GTSECR register even if the simulataneous control of GPT0 is enabled, and the simultaneous control status of GPT0 is not changed.

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The GTSECR register of channel which security attribution is configured as secure can not be written by non-secure access. For example, if GPTn is configured as secure and other GPTs are configured as non-secure, the GPTn.GTSECR register cannot be written by non-secure access to GPT$_{n+1}$.GTSECR register even if the simultaneous control of GPTn is enabled, and the simultaneous control status of GPTn is not changed.