

# RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU	Document No.	TN-RA*-A0037A/E	Rev.	1.00
Title	RA4E1 Group, correction of IO ports	Information Category	Technical Notification		
Applicable Product	RA4E1 Group	Lot No.	Reference Document	RA4E1 Group User's Manual Hardware Rev.1.00	
		All			

The tables of IO ports are corrected.

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## 19. I/O Ports

### 19.6 Peripheral Select Settings for Each Product

**Table 19.5 Register settings for input/output pin function (PORT0)**

PSEL[4:0] settings	Function	pin							
		P000	P001	P002	P003	P004	P013	P014	P015
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
ASEL bit		AN000	AN001	AN002	AN003	AN004	AN011	AN012/DA0	AN013/DA1
ISEL bit		IRQ6-DS	IRQ7-DS	IRQ8-DS	—	IRQ9-DS	—	—	IRQ13
DSCR[1:0] bits	Drive capacity control <sup>1</sup>	L	L	L	L	L	L	L	L
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓	✓	✓	✓
48 pins product		✓	✓	✓	—	—	✓	✓	✓

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**Table 19.5 Register settings for input/output pin function (PORT0)**

PSEL[4:0] settings	Function	pin							
		P000	P001	P002	P003	P004	P013	P014	P015
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
ASEL bit		AN000	AN001	AN002	AN003	AN004	AN011	AN012/DA0	AN013 <del>BA+</del>
ISEL bit		IRQ6-DS	IRQ7-DS	IRQ8-DS	—	IRQ9-DS	—	—	IRQ13
DSCR[1:0] bits	Drive capacity control <sup>1</sup>	L	L	L	L	L	L	L	L
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
64 pins product		✓	✓	✓	✓	✓	✓	✓	✓
48 pins product		✓	✓	✓	—	—	✓	✓	✓

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**Table 19.7 Register settings for input/output pin function (PORT2)**

PSEL[4:0] settings	Function	Pin							
		P200 <sup>4</sup>	P201	P205	P206	P207	P208	P212	P213
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	AGTO1	—	—	—	AGTEE1	AGTEE2
00010b	GPT <sup>2</sup>	—	—	—	—	—	—	GTETRGD	GTETRGC
00011b	GPT <sup>2</sup>	—	—	GTIOC4A	—	—	—	—	—
00100b	SCI	—	—	TXD4/MOSI4/ SDA4	RXD4/MISO4/ SCL4	TXD4/MOSI4/ SDA4	—	—	—
00101b	SCI	—	—	CTS9_RTS9/ SS9	CTS9	—	—	—	—
00111b	IIC <sup>1</sup>	—	—	SCL1_B	SDA1_B	—	—	—	—

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**Table 19.7 Register settings for input/output pin function (PORT2)**

PSEL[4:0] settings	Function	Pin							
		P200 <sup>4</sup>	P201	P205	P206	P207	P208	P212	P213
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	AGTO1	—	—	—	AGTEE1	AGTEE2
00010b	GPT <sup>2</sup>	—	—	—	—	—	—	GTETRGD	GTETRGC
00011b	GPT <sup>2</sup>	—	—	GTIOC4A	—	—	—	—	—
00100b	SCI	—	—	TXD4/MOSI4/ SDA4	RXD4/MISO4/ SCL4	TXD4/MOSI4/ SDA4	—	—	—
00101b	SCI	—	—	CTS9_RTS9/ SS9	CTS9	—	—	—	—
00111b	IIC <sup>1</sup>	—	—	<del>SCL1_B</del>	<del>SDA1_B</del>	—	—	—	—