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Title	RA2L1 Group, RA2E1 Group, Disclosure of CTSU2 test registers for IEC 60730 Class-B functional safety diagnosis.		Information Category	Technical Notification		
Applicable Product	RA2L1 Group RA2E1 Group	Lot No. All	Reference Document	RA2L1 Group User's Manual Hardware Rev.1.10 RA2E1 Group User's Manual Hardware Rev.1.10		

Disclosing CTSU2 test registers used in the self-diagnosis program for IEC 60730 Class-B self-diagnosis.

[before] example: RA2L1

34.2.11 CTSUCALIB/CTSUDBGR1/CTSUDBGR0 : CTSU Calibration Register

Base address: CTSU = 0x4008_2000

Offset address: 0x28 (CTSUCALIB/CTSUDBGR0)

0x2A (CTSUDBGR1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TXREV	CCOCALIB	CCOCLK	DACCLK	SUCARRY	—	DACCARRY	—	—	CFCMODE	CFCSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DCOFF	CFCRDMD	IOC	CNTRDSEL	TSOC	SUCLKEN	CLKSEL[1:0]		DRV	TSOD	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	TSOD	All TS Pin Control This bit controls the output of all TS pins. 0: All TS pins are not fixed 1: Fixed output to all TS pins (outputs select level of the IOC bit)	R/W
3	DRV	Power Supply Forced Start This bit forces the CTSU power supply. 0: CTSU power supply is in idle state. 1: CTSU power supply is in a measurement state.	R/W
5:4	CLKSEL[1:0]	Observation Clock Select These bits select observation of 3 clocks generated by the CTSU analog macro. 0 0: Not selected (L fixed output) 0 1: Measurement clock (divided by 8) 1 0: CFC clock (divided by 8) 1 1: SUCLK (divided by 8)	R/W

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Bit	Symbol	Function	R/W
6	SUCLKEN	SUCLK Forced Oscillation Control This bit oscillates the SUCLK oscillator when not measuring. 0: SUCLK oscillation only during measurement 1: SUCLK always oscillates	R/W
7	TSOC	Switched Capacitor Operation Stop This bit stop the switched capacitor operation 0: Operation 1: Stop	R/W
8	CNTRDSEL	Read Count Select of Sensor Counter This bit selects the number of times to read the sensor counter register. 0: Read once 1: Read twice	R/W
9	IOC	ICTSU TS Pin Fixed Output Value Set This bit selects the output level of TS pins when CTSUCALIB.TSOD bit is 1. 0: Low level 1: High level	R/W
10	CFCRDMD	CTSU CFC Counter Read Mode Select This bit is set to 1 to enter mutual capacitance parallel measurement mode using CFC pins. 0: Except for mutual capacitance parallel measurement mode 1: Mutual capacitance parallel measurement mode	R/W
11	DCOFF	CTSU Down Converter Control This bit controls operation of the down converter. 0: Down converter operation (TSCAP voltage generation) 1: The down converter is off	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
21:16	CFCSEL[5:0]	Observation CFC Clock Select When CLKSEL[1:0] = 11b, these bits select the CFC clock channel to output as the observation clock.	
22	CFCMODE	CFC Oscillator Calibration Mode 0: CFC current measurement (normal operation) 1: External current measurement for calibration	R/W
24:23	—	These bits are read as 0. The write value should be 0.	R/W
25	DACCARRY	Offset Current Adjustment for Calibration 0: Normal operation 1: All current sources can be turned on	R/W
26	—	This bit is read as 0. The write value should be 0.	R/W
27	SUCARRY	Current Control Oscillator Input Current Adjustment for SUCLK This bit enables all current sources to be turned on for calibration. 0: Normal operation 1: All current sources can be turned on	R/W
28	DACCLK	Modulation Clock Select for Offset Current Circuits 0: Operating clock selected by TSUCRA.CLK [1:0] 1: SUCLK	R/W
29	CCOCLK	Modulation Clock Select for Current Controlled Oscillator Input Current of SUCLK 0: Operating clock selected by TSUCRA.CLK [1:0] 1: SUCLK	R/W
30	CCOCALIB	Calibration Selection of Current Controlled Oscillator for Measurement 0: Normal operation 1: Oscillator calibration mode	R/W
31	TXREV	Transmit Pin Inverted Output This bit controls the polarity of the pulse output from the transmission pin. 0: Normal 1: Invert	R/W

The CTSU Calibration Register (CTSUCALIB/CTSUDBGR1/CTSUDBGR0) is a 32-bit and 16-bit read/write register.

The CTSUCALIB is accessed in 32-bit units. The CTSUDBGR1 (bits [31:16] in CTSUCALIB) and CTSUDBGR0 (bits [15:0] in CTSUCALIB) are accessed in 16-bit units.

TSOD bit (All TS Pin Control)

The TSOD bit controls the output of all TS pins.

When the TSOD = 1, the valid channel outputs the value of the IOC bit according to the power supply of the TXVSEL[1:0] bits.

DRV bit (Power Supply Forced Start)

When the DRV = 1, the CTSU power supply is in the measurement state, and the offset current forced output.

CLKSEL[1:0] bits (Observation Clock Select)

CLKSEL[1:0] bits selects a clock that can be observed on the external pin.

TSOC bit (Switched Capacitor Operation Stop)

The TSOC bit is used to calibrate and is set to 0 in electrostatic capacitance measurement.

The switched capacitor operation of the TS pin is stopped and the current in the CTSU can be measured. It is possible to calibrate the current controlled oscillator based on this current.

CNTRDSEL bit (Read Count Select of Sensor Counter)

Set the CNTRDSEL bit to 0 to read the sensor counter.

To read the sensor and SUCLK counters twice with 16-bit access, set this bit to 1.

IOC bit (ICTSU TS Pin Fixed Output Value Set)

The IOC bit selects the output level of TS pins when the TSOD bit is 1.

CFCRDMD bit (CTSU CFC Counter Read Mode Select)

When entering mutual capacitance parallel measurement mode using CFC pins, the CFCRDMD bit is set to 1.

DCOFF bit (CTSU Down Converter Control)

The DCOFF bit controls the operation of the down voltage converter to generate TSCAP voltage. When DCOFF = 0 and PON = 1, TSCAP voltage is generated and normal operation is possible. When DCOFF = 1, down converter is forced to stop and only offset current is output.

CFCSEL[5:0] bits (Observation CFC Clock Select)

The CFCSEL[5:0] bits are enabled when CLKSEL[1:0] = 11b.

These bits select the channel of the CFC clock to be output as the observation clock.

CFCMODE bit (CFC Oscillator Calibration Mode)

When CFCMODE = 1, a current equivalent to the SUCLK oscillator and supply current is supplied to the current controlled oscillator in the CFC circuit on each pin.

This current is used to calibrate the current-controlled oscillator characteristics in the CFC circuit on each pin.

DACCARRY bit (Offset Current Adjustment for Calibration)

When DACCARRY = 1, all current sources can be turned on. This is used for calibration.

SUCARRY bit (Current Control Oscillator Input Current Adjustment for SUCLK)

When SUCARRY = 1, all current sources can be turned on. This is used for calibration.

DACCLK bit (Modulation Clock Select for Offset Current Circuits)

The DACCLK bit selects the modulation clock for the offset current circuit.

CCOCLK bit (Modulation Clock Select for Current Controlled Oscillator Input Current of SUCLK)

The CCOCLK bit selects the clock for the CCO modulation circuit.

CCOCALIB bit (Calibration Selection of Current Controlled Oscillator for Measurement)

When CCOCALIB = 1, the input current of the SUCLK current control oscillator and the measurement current control oscillator are swapped.

The characteristics of the measurement current controlled oscillator can be calibrated by supplying the input current of the SUCLK current controlled oscillator to the measurement current controlled oscillator.

TXREV bit (Transmit Pin Inverted Output)

When TXREV = 1, the pulse output from the transmit pin can be inverted.

34.2.1 CTSUCRA/CTSUCRAH/CTSUCRAL/CTSUCR3/CTSUCR2/CTSUCR1/ CTSUCR0 :

CTSU Control Register A

Base address: CTSU = 0x4008_2000

Offset address: 0x00 (CTSUCRA/CTSUCRAL/CTSUCR0)

0x01 (CTSUCR1)

0x02 (CTSUCRAH/CTSUCR2)

0x03 (CTSUCR3)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DCBACK	DCMODE	STCLK[5:0]						PCSEL	SDPSEL	POSE [1:0]		LOAD[1:0]		ATUNE2	MD2
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MD1	MD0	CLK[1:0]		ATUNE1	ATUNE0	CSW	PON	TXVSEL[1:0]		PUMPON	INIT	CFCON	SNZ	CAP	STRT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STRT	CTSU Measurement Operation Start 0: Stop measurement operation*1 1: Start measurement operation	R/W
1	CAP	CTSU Measurement Operation Start Trigger Select 0: Software trigger 1: External trigger	R/W
2	SNZ	CTSU Wait State Power-Saving Enable 0: Disable power-saving function during wait state 1: Enable power-saving function during wait state	R/W
3	CFCON	CTSU CFC Power On Control 0: CFC power off 1: CFC power on	R/W
4	INIT	CTSU Control Block Initialization Writing 1 to this bit initializes the CTSU control block and the CTSUSCNT, CTSUCFCCNT, CTSUMCH, and CTSUSR registers. This bit is read as 0.	W
5	PUMPON	CTSU Boost Circuit Control 0: Boost circuit off 1: Boost circuit on	R/W
7:6	TXVSEL[1:0]	CTSU Transmission Power Supply Selection 0 0: Selecting VCC as the power supply for the transmit pins of mutual capacitance method. 0 1: Selecting VCC as the power supply for the transmit pins of the mutual capacitance method. In addition, noise is reduced during GPIO operation. (Recommended) 1 0: Select VCC as the power source for the transmitter pins used as the active shield. 1 1: Setting prohibited	R/W
8	PON	CTSU Power On Control 0: Power off the CTSU 1: Power on the CTSU	R/W
9	CSW	TSCAP Pin Enable 0: Disable 1: Enable	R/W

Bit	Symbol	Function	R/W
10	ATUNE0	CTSU Power Supply Operating Mode Setting 0: VCC ≥ 2.4 V: Normal voltage operating mode VCC < 2.4 V: Setting prohibited 1: Low-voltage operating mode	R/W
11	ATUNE1	CTSU Current Range Adjustment 0: 80 µA when CTSUATUNE2 = 0 20 µA when CTSUATUNE2 = 1 1: 40 µA when CTSUATUNE2 = 0 160 µA when CTSUATUNE2 = 1	R/W
13:12	CLK[1:0]	CTSU Operating Clock Select 0 0: PCLKB 0 1: PCLKB/2 (PCLKB divided by 2) 1 0: PCLKB/4 (PCLKB divided by 4) 1 1: PCLKB/8 (PCLKB divided by 8)	R/W
14	MD0	CTSU Measurement Mode Select 0 0: Single scan mode 1: Multi-scan mode	R/W
15	MD1	CTSU Measurement Mode Select 1 0: One-time measurement (self-capacitance method) 1: Two times measurement (mutual capacitance method)	R/W
16	MD2	CTSU Measurement Mode Select 2 0: Measure the switched capacitor current and the DC current 1: Measure the charge transfer by CFC circuit (parallel measurement)	R/W
17	ATUNE2	CTSU Current Range Adjustment 0: 80 µA when CTSUATUNE1 = 0 40 µA when CTSUATUNE1 = 1 1: 20 µA when CTSUATUNE1 = 0 160 µA when CTSUATUNE1 = 1	R/W
19:18	LOAD[1:0]	CTSU Load Control During Measurement 0 0: 2.5 µA constant current load 0 1: No load 1 0: 20 µA constant current load and overcurrent detector disabled 1 1: Resistance load for calibration. To set LOAD[1:0] bits to resistance load for calibration, set these bits to 10b before they are set to 11b.	R/W
21:20	POSEL[1:0]	CTSU Non-Measured Channel Output Select 0 0: Output low 0 1: Hi-Z 1 0: Setting prohibited 1 1: Output a pulse in phase with the transmit channel	R/W
22	SDPSEL	CTSU Sensor Drive Pulse Select 0: Random pulse 1: Normal pulse using the sensor unit clock	R/W
23	PCSEL	CTSU Boost Circuit Clock Select 0: Sensor drive pulse divided by 2 1: STCLK	R/W
29:24	STCLK[5:0]	CTSU STCLK Select 0x00: Operating clock divided by 2 0x01: Operating clock divided by 4 0x02: Operating clock divided by 6 ⋮ 0x3E: Operating clock divided by 126 0x3F: Operating clock divided by 128	R/W
30	DCMODE	CTSU Current Measurement Mode Select 0: Electrostatic capacitance measurement mode 1: Current measurement mode	R/W
31	DCBACK	CTSU Current Measurement Feedback Select 0: TSCAP pin is selected 1: Measurement pin is selected. It is recommended in the current measurement mode.	R/W

Note 1. When the CTSU is not used, set this bit to 0.

The CTSU Control Register A (CTSUCRA/CTSUCRAH/CTSUCRAL/CTSUCR3/CTSUCR2/CTSUCR1/CTSUCR0) is a 32-bit, 16-bit, and 8-bit read/write register. The CTSUCRA is accessed in 32-bit units. The CTSUCRAH (bits [31:16] in CTSUCRA) and CTSUCRAL (bits [15:0] in CTSUCRA) are accessed in 16-bit units. The CTSUCR3 (bits [31:24] in CTSUCRA), CTSUCR2 (bits [23:16] in CTSUCRA), CTSUCR1 (bits [15:8] in CTSUCRA), and CTSUCR0 (bits [7:0] in CTSUCRA) are accessed in 8-bit units.

Only set the bits other than the STRT bit and INIT bit when the STRT bit is 0.

STRT bit (CTSU Measurement Operation Start)

The STRT bit specifies whether CTSU operation starts or stops. When the CAP bit is 0, measurement is started by writing 1 to the STRT bit, and the STRT bit becomes 0 when measurement is finished. When the STRT bit is 1, the CTSU waits for an external trigger by writing 1 to the STRT bit, and measurement starts on the rising edge of the external trigger. When measurement is finished, the CTSU waits for the next external trigger and operation continues.

Table 34.3 lists the CTSU states.

Table 34.3 CTSU state

STRT bit	CAP bit	CTSU state
0	0	Stopped
0	1	Stopped
1	0	Measurement in progress
1	1	Measurement in progress and waiting for an external trigger*1

Note 1. The state can be read from the CTSUSR.STC[2:0] flags as follows:

- During measurement: CTSUSR.STC[2:0] flags ≠ 000b
- While waiting for an external trigger: CTSUSR.STC[2:0] flags = 000b
- When the CTSU is not used, set this bit to 0.

If software sets the STRT bit to 1 when the bit is already 1, the write is ignored and operation continues. To force operation to stop through software when the STRT bit is 1, set the STRT bit to 0 and the INIT bit to 1 simultaneously.

CAP bit (CTSU Measurement Operation Start Trigger Select)

The CAP bit specifies the measurement start condition. For details, see STRT bit (CTSU Measurement Operation Start).

SNZ bit (CTSU Wait State Power-Saving Enable)

The SNZ bit enables or disables power-saving operation during a wait state. It can also suspend the CTSU analog macro which decreases power consumption during the wait state. In the suspended state, the CTSU power supply is turned off while the external TSCAP is still charged.

Table 34.4 shows the CTSU power supply state control.

Table 34.4 CTSU power supply state control

PON bit	SNZ bit	CAP bit	STRT bit	CTSU analog macro state
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: Other settings are prohibited.

To start measurement from the suspended state, set the SNZ bit to 0, then set the STRT bit to 1. To suspend the module after measurement stops, set the SNZ bit to 1.

CFCON bit (CTSU CFC Power On Control)

The CFCON bit controls the power supply to the CFC.

INIT bit (CTSU Control Block Initialization)

Write 1 to the INIT bit to initialize the internal control registers. To force the current operation to stop, set the STRT bit to 0 and the INIT bit to 1 simultaneously. This stops the operation and initializes the internal control registers.

Do not write 1 to the INIT bit when the STRT bit is 1.

PUMPON bit (CTSU Boost Circuit Control)

The PUMPON bit turns on or off the boost circuit. The PUMPON bit should be set to 1 when VCC < 4.5 V.

TXVSEL[1:0] bits (CTSU Transmission Power Supply Selection)

In measurement methods other than self-capacitance method, VCC is selected as the power supply for the transmit pins by setting the TXVSEL[1:0] bits to 01b. In self-capacitance method, VCC is selected as the power supply for the transmit pins used as transmit pulse output shield by setting the TXVSEL[1:0] bits to 10b. When the VCC voltage fluctuates greatly due to the switching of the output buffer, switching to the VCL can reduce the effect on the voltage fluctuation.

PON bit (CTSU Power On Control)

The PON bit controls the power supply to the CTSU.

CSW bit (TSCAP Pin Enable)

The CSW bit controls charging of the LPF capacitor connected to the TSCAP pin by turning the capacitance switch on or off. After the capacitance switch is turned on, wait about 1 ms until the capacitance connected to the TSCAP pin is charged before starting measurement by setting STRT to 1. Before starting measurement, use an I/O port to output low to the TSCAP pin, and discharge the existing LPF capacitance.

Set the PON to 1 only when CSW bit is 1. When VCC < 4.5 V, set CSW bit is 1 after PUMPON bit is set to 1.

ATUNE0 bit (CTSU Power Supply Operating Mode Setting)

The ATUNE0 bit sets the power supply operating mode. Set this bit according to the lower limit of VCC to operate the CTSU.

ATUNE2 and ATUNE1 bits (CTSU Current Range Adjustment)

The ATUNE2 and ATUNE1 bits set the current range at the time of measurement. In general, setting these bits to 00b is

recommended.

CLK[1:0] bits (CTSU Operating Clock Select)

The CLK[1:0] bits select the operating clock.

MD0 bit (CTSU Measurement Mode Select 0)

The MD0 bit selects the single scan or multi-scan mode. In single scan mode, electrostatic capacitance on a channel is measured. In multi-scan mode, electrostatic capacitance on all channels that are specified as measurement targets by setting the CTSUCHACn registers are measured sequentially in ascending order.

MD1 bit (CTSU Measurement Mode Select 1)

The MD1 bit selects the measurement method. If MD1 = 0, a channel is measured once. Set the MD1 bit to 0 when measuring in the self-capacitance method. If MD1 = 1 and the transmit channel is set, a channel is measured twice. In the first measurement, the in-phase pulse is output to the transmit channel and measured. In the second measurement, the reversed-phase pulse is output to the transmit channel and measured. Set the MD1 bit to 1 when measuring in the mutual capacitance method.

MD2 bit (CTSU Measurement Mode Select 2)

The MD2 bit enables parallel measurement using the charge transfer method.

LOAD[1:0] bits (CTSU Load Control During Measurement)

The LOAD[1:0] bits control the measurement load.

POSEL[1:0] bits (CTSU Non-Measured Channel Output Select)

The POSEL[1:0] bits select the CTSU non-measured channel output.

SDPSEL bit (CTSU Sensor Drive Pulse Select)

The SDPSEL bit selects the sensor drive pulse.

When SDPSEL = 0, the random pulse mode is selected for sensor drive pulse. PCLKB divided by CTSUCRA.CLK[1:0] and CTSUS0.SDPA[7:0] bits setting (phased-shifted by the random number generated by the CTSUCRB.PRMODE[1:0] and CTSUCRB.PRATTIO[3:0] bits) is selected as the sensor drive pulse. It is also possible to apply jitter by frequency spreading clock.

When SDPSEL = 1, the normal pulse mode using the sensor unit clock is selected. The sensor drive clock is the sensor unit clock divided by the CTSUSO.SDPA[7:0] bits. In addition, it is possible to improve the noise immunity by multiplied clock in the sensor unit and switching the frequency of drive pulse or by using a majority decision processing the frequency measurement results of the clock in the sensor unit.

PCSEL bit (CTSU Boost Circuit Clock Select)

The PCSEL bit selects the clock for the boost circuit.

STCLK[5:0] bits (CTSU STCLK Select)

STCLK is the reference clock for measurement time. It is generated by dividing PCLKB. The STCLK [5:0] bits set the

division value from PCLKB. The division value is determined by the following expression:

Division value = (STCLK[5:0] + 1) × 2

The STCLK frequency should be set to 0.5 MHz (2 µs).

DCMODE bit (CTSU Current Measurement Mode Select)

The DCMODE bit selects the capacitance measurement mode by switched-capacitor or the current measurement mode. In the current measurement mode, the switched-capacitor operation turns off and current is measured.

DCBACK bit (CTSU Current Measurement Feedback Select)

When DCMODE = 1, the DCBACK bit is enabled. When DCBACK = 1, the voltage of the TS pin is referenced during measurement.

[after]

34.2.11 CTSUCALIB/CTSUDBGR1/CTSUDBGR0 : CTSU Calibration Register

Base address: CTSU = 0x4008_2000

Offset address: 0x28 (CTSUCALIB/CTSUDBGR0)

0x2A (CTSUDBGR1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TXREV	CCOCALIB	CCOCLK	DACCLK	SUCARRY	SUMSEL	DACCARRY	DACMSEL	—	CFCMODE	CFCSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DCOFF	CFCRDMD	IOC	CNTRDSEL	TSOC	SUCLKEN	CLKSEL[1:0]		DRV	TSOD	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	TSOD	TS Pins Fixed Output 0: Capacitance measurement mode 1: Output High or Low from TS terminals (Controlling by the IOC bit)	R/W
3	DRV	Power Supply Calibration Select 0: Capacitance measurement mode 1: Power supply calibration mode	R/W
5:4	CLKSEL[1:0]	Observation Clock Select These bits select observation of 3 clocks generated by the CTSU analog macro. 0 0: Not selected (L fixed output) 2 1: Measurement clock (divided by 8) 3 0: CFC clock (divided by 8) 1 1: SUCLK (divided by 8)	R/W
6	SUCLKEN	SUCLK Forced Oscillation Control This bit oscillates the SUCLK oscillator when not measuring. 0: SUCLK oscillation only during measurement 1: SUCLK always oscillates	R/W
7	TSOC	Switched Capacitor Operation Calibration Select Bit 0: Capacitance measurement mode 1: Switched capacitor operation calibration mode	R/W
8	CNTRDSEL	Read Count Select of Sensor Counter This bit selects the number of times to read the sensor counter register. 0: Read once 1: Read twice	R/W
9	IOC	~~ICTSU~~ TS Pin Fixed Output Value Set This bit selects the output level of TS pins when CTSUCALIB.TSOD bit is 1. 0: Low level 1: High level	R/W
10	CFCRDMD	~~CTSU~~ CFC Counter Read Mode Select This bit is set to 1 to enter mutual capacitance parallel measurement mode using CFC pins. 0: Except for mutual capacitance parallel measurement mode 1: Mutual capacitance parallel measurement mode	R/W
11	DCOFF	~~CTSU~~ Down Converter Control This bit controls operation of the voltage down converter. 0: Voltage down converter operation (TSCAP voltage generation) 1: The voltage down converter is off	R/W

Bit	Symbol	Function	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
21:16	CFCSEL[5:0]	Observation CFC Clock Select When CLKSEL[1:0] = 11b, these bits select the CFC clock channel to output as the observation clock.	
22	CFCMODE	CFC Oscillator Calibration Mode Select 0: CFC current measurement (Capacitance measurement mode) 1: External current measurement for calibration	R/W
23	—	These bits are read as 0. The write value should be 0.	R/W
24	DACMSEL	Current Offset DAC Current Matrix Calibration Select 0: Capacitance measurement mode 1: Current offset DAC current Calibration mode	R/W
25	DACCARRY	Offset Current Adjustment for Calibration 0: Normal operation 1: All current sources can be turned on	R/W
26	SUMSEL	Current Control Oscillator Input Current Matrix Calibration Select 0: Capacitance measurement mode 1: Current control oscillator input current matrix calibration mode	R/W
27	SUCARRY	Current Control Oscillator Input Current Adjustment for SUCLK This bit enables all current sources to be turned on for calibration. 0: Normal operation 1: All current sources can be turned on	R/W
28	DACCLK	Modulation Clock Select for Offset Current Circuits 0: Operating clock selected by CTSUCRA.CLK [1:0] 1: SUCLK	R/W
29	CCOCLK	Modulation Clock Select for Current Controlled Oscillator Input Current of SUCLK 0: Operating clock selected by CTSUCRA.CLK [1:0] 1: SUCLK	R/W
30	CCOCALIB	Calibration Selection of Current Controlled Oscillator for Measurement 0: Capacitance measurement mode 1: Oscillator calibration mode	R/W
31	TXREV	Transmit Pin Inverted Output This bit controls the polarity of the pulse output from the transmission pin. 0: Normal 1: Invert	R/W

The CTSU Calibration Register (CTSUCALIB/CTSUDBGR1/CTSUDBGR0) is a 32-bit and 16-bit read/write register.

The CTSUCALIB is accessed in 32-bit units. The CTSUDBGR1 (bits [31:16] in CTSUCALIB) and CTSUDBGR0 (bits [15:0] in CTSUCALIB) are accessed in 16-bit units.

TSOD bit (All TS Pin Control)

The TSOD bit controls the output of all TS pins.

When the TSOD = 1, the valid channel outputs the value of the IOC bit according to the power supply of the TXVSEL[1:0] bits.

DRV bit (Power Supply Calibration Select)

DRV bit is used a calibration for power supply.

CLKSEL[1:0] bits (Observation Clock Select)

CLKSEL[1:0] bits selects a clock that can be observed on the external pin.

TSOC bit (Switched Capacitor Operation Calibration Select)

When the TSOC bit set to 1, the TS terminal switching capacitor operation stops and the CTSU current can be measured. It is used for calibration of current control oscillator based on this current.

CNTRDSEL bit (Read Count Select of Sensor Counter)

Set the CNTRDSEL bit to 0 to read the sensor counter.

To read the sensor and SUCLK counters twice with 16-bit access, set this bit to 1.

IOC bit (ICTSU TS Pin Fixed Output Value Set)

The IOC bit selects the output level of TS pins when the TSOD bit is 1.

CFCRDMD bit (CTSU CFC Counter Read Mode Select)

When entering mutual capacitance parallel measurement mode using CFC pins, the CFCRDMD bit is set to 1.

DCOFF bit (CTSU Down Converter Control)

The DCOFF bit controls the operation of the voltage down voltage converter to generate TSCAP voltage. When the DCOFF is set to 0 and the PON is set to 1, TSCAP voltage is generated and normal operation is possible. When the DCOFF is set to 1, voltage down converter is forced to stop and only offset current is output.

CFCSEL[5:0] bits (Observation CFC Clock Select)

The CFCSEL[5:0] bits are enabled when CLKSEL[1:0] = 11b.

These bits select the channel of the CFC clock to be output as the observation clock.

CFCMODE bit (CFC Oscillator Calibration Select)

When the CFCMODE is set to 1, a current equivalent to the SUCLK oscillator and supply current is supplied to the current controlled oscillator in the CFC circuit on each pin.

This current is used to calibrate the current-controlled oscillator characteristics in the CFC circuit on each pin.

DACMSEL bit (Current Offset DAC Current Matrix Calibration Select)

When the DACMSEL is set to 1, Current offset DAC current matrix calibration mode is on. This is used for calibration.

DACCARRY bit (Offset Current Adjustment for Calibration)

When the DACCARRY is set to 1, all current sources can be turned on. This is used for calibration.

SUMSEL bit (Current Control Oscillator Input Current Matrix Calibration Select)

When the SUMSEL is set to 1, Current control oscillator input current matrix calibration mode is on. This is used for calibration.

SUCARRY bit (Current Control Oscillator Input Current Adjustment for SUCLK)

When the SUCARRY is set to 1, all current sources can be turned on. This is used for calibration.

DACCLK bit (Modulation Clock Select for Offset Current Circuits)

The DACCLK bit selects the modulation clock for the offset current circuit.

CCOCLK bit (Modulation Clock Select for Current Controlled Oscillator Input Current of SUCLK)

The CCOCLK bit selects the clock for the CCO modulation circuit.

CCOCALIB bit (Calibration Selection of Current Controlled Oscillator for Measurement)

When the CCOCALIB is set to 1, the input current of the SUCLK current control oscillator and the measurement current control oscillator are swapped.

The characteristics of the measurement current controlled oscillator can be calibrated by supplying the input current of the SUCLK current controlled oscillator to the measurement current controlled oscillator.

TXREV bit (Transmit Pin Inverted Output)

When the TXREV is set to 1, the pulse output from the transmit pin can be inverted.

34.2.1 CTSUCRA/CTSUCRAH/CTSUCRAL/CTSUCR3/CTSUCR2/CTSUCR1/ CTSUCR0 :

CTSU Control Register A

Base address: CTSU = 0x4008_2000

Offset address: 0x00 (CTSUCRA/CTSUCRAL/CTSUCR0)

0x01 (CTSUCR1)

0x02 (CTSUCRAH/CTSUCR2)

0x03 (CTSUCR3)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DCBACK	DCMODE	STCLK[5:0]						PCSEL	SDPSEL	POSE [1:0]		LOAD[1:0]		ATUNE2	MD2
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MD1	MD0	CLK[1:0]		ATUNE1	ATUNE0	CSW	PON	TXVSEL[1:0]		PUMPON	INIT	CFCON	SNZ	CAP	STRT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	STRT	CTSU Measurement Operation Start 0: Stop measurement operation*1 1: Start measurement operation	R/W
1	CAP	CTSU Measurement Operation Start Trigger Select 0: Software trigger 1: External trigger	R/W
2	SNZ	CTSU Wait State Power-Saving Enable 0: Disable power-saving function during wait state 1: Enable power-saving function during wait state	R/W
3	CFCON	CTSU CFC Power On Control 0: CFC power off 1: CFC power on	R/W
4	INIT	CTSU Control Block Initialization Writing 1 to this bit initializes the CTSU control block and the CTSUSCNT, CTSUCFCCNT, CTSUMCH, and CTSUSR registers. This bit is read as 0.	W
5	PUMPON	CTSU Boost Circuit Control 0: Boost circuit off 1: Boost circuit on	R/W
7:6	TXVSEL[1:0]	CTSU Transmission Power Supply Selection 0 0: Selecting VCC as the power supply for the transmit pins of mutual capacitance method. 2 1: Selecting VCC as the power supply for the transmit pins of the mutual capacitance method. In addition, noise is reduced during GPIO operation. (Recommended) 3 0: Select VCC as the power source for the transmitter pins used as the active shield. 1 1: Setting prohibited	R/W
8	PON	CTSU Power On Control 0: Power off the CTSU 1: Power on the CTSU	R/W
9	CSW	TSCAP Pin Enable 0: Disable 1: Enable	R/W

Bit	Symbol	Function	R/W
10	ATUNE0	CTSU Power Supply Operating Mode Setting 0: VCC ≥ 2.4 V: Normal voltage operating mode VCC < 2.4 V: Setting prohibited 1: Low-voltage operating mode	R/W
11	ATUNE1	CTSU Current Range Adjustment 0: 80 µA when CTSUATUNE2 = 0 20 µA when CTSUATUNE2 = 1 1: 40 µA when CTSUATUNE2 = 0 160 µA when CTSUATUNE2 = 1	R/W
13:12	CLK[1:0]	CTSU Operating Clock Select 0 0: PCLKB 2 1: PCLKB/2 (PCLKB divided by 2) 3 0: PCLKB/4 (PCLKB divided by 4) 1 1: PCLKB/8 (PCLKB divided by 8)	R/W
14	MD0	CTSU Measurement Mode Select 0 0: Single scan mode 1: Multi-scan mode	R/W
15	MD1	CTSU Measurement Mode Select 1 0: One-time measurement (self-capacitance method) 1: Two times measurement (mutual capacitance method)	R/W
16	MD2	CTSU Measurement Mode Select 2 0: Measure the switched capacitor current and the DC current 1: Measure the charge transfer by CFC circuit (parallel measurement)	R/W
17	ATUNE2	CTSU Current Range Adjustment 0: 80 µA when CTSUATUNE1 = 0 40 µA when CTSUATUNE1 = 1 1: 20 µA when CTSUATUNE1 = 0 160 µA when CTSUATUNE1 = 1	R/W
19:18	LOAD[1:0]	CTSU Load Control During Measurement 0 0: 2.5 µA constant current load 2 1: No load 3 0: 20 µA constant current load and overcurrent detector disabled 1 1: Resistance load for calibration. To set LOAD[1:0] bits to resistance load for calibration, set these bits to 10b before they are set to 11b.	R/W
21:20	POSEL[1:0]	CTSU Non-Measured Channel Output Select 0 0: Output low 2 1: Hi-Z 3 0: Setting prohibited 1 1: Output a pulse in phase with the transmit channel	R/W
22	SDPSEL	CTSU Sensor Drive Pulse Select 0: Random pulse 1: Normal pulse using the sensor unit clock	R/W
23	PCSEL	CTSU Boost Circuit Clock Select 0: Sensor drive pulse divided by 2 1: STCLK	R/W
29:24	STCLK[5:0]	CTSU STCLK Select 0x00: Operating clock divided by 2 0x01: Operating clock divided by 4 0x02: Operating clock divided by 6 ⋮ 0x3E: Operating clock divided by 126 0x3F: Operating clock divided by 128	R/W
30	DCMODE	CTSU Current Measurement Mode Select 0: Electrostatic capacitance measurement mode 1: Current measurement mode	R/W
31	DCBACK	CTSU Current Measurement Feedback Select 0: TSCAP pin is selected 1: Measurement pin is selected. It is recommended in the current measurement mode.	R/W

Note 1. When the CTSU is not used, set this bit to 0.

The CTSU Control Register A (CTSUCRA/CTSUCRAH/CTSUCRAL/CTSUCR3/CTSUCR2/CTSUCR1/CTSUCR0) is a 32-bit, 16-bit, and 8-bit read/write register. The CTSUCRA is accessed in 32-bit units. The CTSUCRAH (bits [31:16] in CTSUCRA) and CTSUCRAL (bits [15:0] in CTSUCRA) are accessed in 16-bit units. The CTSUCR3 (bits [31:24] in CTSUCRA), CTSUCR2 (bits [23:16] in CTSUCRA), CTSUCR1 (bits [15:8] in CTSUCRA), and CTSUCR0 (bits [7:0] in CTSUCRA) are accessed in 8-bit units.

Only set the bits other than the STRT bit and INIT bit when the STRT bit is 0.

STRT bit (CTSU Measurement Operation Start)

The STRT bit specifies whether CTSU operation starts or stops. When the CAP bit is 0, measurement is started by writing 1 to the STRT bit, and the STRT bit becomes 0 when measurement is finished. When the STRT bit is 1, the CTSU waits for an external trigger by writing 1 to the STRT bit, and measurement starts on the rising edge of the external trigger. When measurement is finished, the CTSU waits for the next external trigger and operation continues.

Table 34.3 lists the CTSU states.

Table 34.3 CTSU state

STRT bit	CAP bit	CTSU state
0	0	Stopped
0	1	Stopped
1	0	Measurement in progress
1	1	Measurement in progress and waiting for an external trigger*1

Note 1. The state can be read from the CTSUSR.STC[2:0] flags as follows:

- During measurement: CTSUSR.STC[2:0] flags ≠ 000b
- While waiting for an external trigger: CTSUSR.STC[2:0] flags = 000b
- When the CTSU is not used, set this bit to 0.

If software sets the STRT bit to 1 when the bit is already 1, the write is ignored and operation continues. To force operation to stop through software when the STRT bit is 1, set the STRT bit to 0 and the INIT bit to 1 simultaneously.

CAP bit (CTSU Measurement Operation Start Trigger Select)

The CAP bit specifies the measurement start condition. For details, see STRT bit (CTSU Measurement Operation Start).

SNZ bit (CTSU Wait State Power-Saving Enable)

The SNZ bit enables or disables power-saving operation during a wait state. It can also suspend the CTSU analog macro which decreases power consumption during the wait state. In the suspended state, the CTSU power supply is turned off while the external TSCAP is still charged.

Table 34.4 shows the CTSU power supply state control.

Table 34.4 CTSU power supply state control

PON bit	SNZ bit	CAP bit	STRT bit	External trigger	Hard macro(VDC) state
0	0	0	0	—	Stopped
1	0	—	—	—	Operating state
1	1	0	0	—	Suspended state
1	1	1	1	No (Waiting)	Suspended state
1	1	1	1	Yes (Operating)	Operating state
1	1	0	0	—	S/W Suspended state
Other than above					Setting prohibited

By enabling the SNOOZE operation and setting the STRT bit to 1, the CPU can transition to STOP mode while waiting for an external trigger. When a falling edge of an external trigger is detected during STOP mode, CTSU issues a clock request to the clock generation block, transitions to the SNOOZE state, and starts measurement. Set the SNZ bit to 0 by software after the completion interrupt. When Sensor Unit clock (SUCLK) is selected for the sensor drive pulse (CTSUCRA.SDPSEL = 1) and the SNOOZE function is used, selection of the sensor drive pulse for the boost clock (CTSUCRA.PCSEL = 0) is prohibited.

CFCON bit (CTSU CFC Power On Control)

The CFCON bit controls the power supply to the CFC.

INIT bit (CTSU Control Block Initialization)

Write 1 to the INIT bit to initialize the internal control registers. To force the current operation to stop, set the STRT bit to 0 and the INIT bit to 1 simultaneously. This stops the operation and initializes the internal control registers.

Do not write 1 to the INIT bit when the STRT bit is 1.

PUMPON bit (CTSU Boost Circuit Control)

The PUMPON bit turns on or off the boost circuit. The PUMPON bit should be set to 1 when VCC < 4.5 V.

TXVSEL[1:0] bits (CTSU Transmission Power Supply Selection)

In measurement methods other than self-capacitance method, VCC is selected as the power supply for the transmit pins by setting the TXVSEL[1:0] bits to 01b. In self-capacitance method, VCC is selected as the power supply for the transmit pins used as transmit pulse output shield by setting the TXVSEL[1:0] bits to 10b. When the VCC voltage fluctuates greatly due to the switching of the output buffer, switching to the VCL can reduce the effect on the voltage fluctuation.

PON bit (CTSU Power On Control)

The PON bit controls the power supply to the CTSU.

CSW bit (TSCAP Pin Enable)

The CSW bit controls charging of the LPF capacitor connected to the TSCAP pin by turning the capacitance switch on or off. After the capacitance switch is turned on, wait about 1 ms until the capacitance connected to the TSCAP pin is charged before starting measurement by setting STRT to 1. Before starting measurement, use an I/O port to output low to the TSCAP pin, and discharge the existing LPF capacitance.

Set the PON to 1 only when CSW bit is 1. When VCC < 4.5 V, set CSW bit is 1 after PUMPON bit is set to 1.

ATUNE0 bit (CTSU Power Supply Operating Mode Setting)

The ATUNE0 bit sets the power supply operating mode. Set this bit according to the lower limit of VCC to operate the CTSU.

ATUNE2 and ATUNE1 bits (CTSU Current Range Adjustment)

The ATUNE2 and ATUNE1 bits set the current range at the time of measurement. In general, setting these bits to 00b is recommended.

CLK[1:0] bits (CTSU Operating Clock Select)

The CLK[1:0] bits select the operating clock.

MD0 bit (CTSU Measurement Mode Select 0)

The MD0 bit selects the single scan or multi-scan mode. In single scan mode, electrostatic capacitance on a channel is measured. In multi-scan mode, electrostatic capacitance on all channels that are specified as measurement targets by setting the CTSUCHACn registers are measured sequentially in ascending order.

MD1 bit (CTSU Measurement Mode Select 1)

The MD1 bit selects the measurement method. If MD1 = 0, a channel is measured once. Set the MD1 bit to 0 when measuring in the self-capacitance method. If MD1 = 1 and the transmit channel is set, a channel is measured twice. In the first measurement, the in-phase pulse is output to the transmit channel and measured. In the second measurement, the reversed-phase pulse is output to the transmit channel and measured. Set the MD1 bit to 1 when measuring in the mutual capacitance method.

MD2 bit (CTSU Measurement Mode Select 2)

The MD2 bit enables parallel measurement using the charge transfer method.

LOAD[1:0] bits (CTSU Load Control During Measurement)

The LOAD[1:0] bits control the measurement load.

POSEL[1:0] bits (CTSU Non-Measured Channel Output Select)

The POSEL[1:0] bits select the CTSU non-measured channel output.

SDPSEL bit (CTSU Sensor Drive Pulse Select)

The SDPSEL bit selects the sensor drive pulse.

When SDPSEL = 0, the random pulse mode is selected for sensor drive pulse. PCLKB divided by CTSUCRA.CLK[1:0] and CTSUS0.SDPA[7:0] bits setting (phased-shifted by the random number generated by the CTSUCRB.PRMODE[1:0] and CTSUCRB.PRATTIO[3:0] bits) is selected as the sensor drive pulse. It is also possible to apply jitter by frequency spreading clock.

When SDPSEL = 1, the normal pulse mode using the sensor unit clock is selected. The sensor drive clock is the sensor unit clock divided by the CTSUSO.SDPA[7:0] bits. In addition, it is possible to improve the noise immunity by multiplied clock in the sensor unit and switching the frequency of drive pulse or by using a majority decision processing the frequency measurement results of the clock in the sensor unit.

PCSEL bit (CTSU Boost Circuit Clock Select)

The PCSEL bit selects the clock for the boost circuit.

STCLK[5:0] bits (CTSU STCLK Select)

STCLK is the reference clock for measurement time. It is generated by dividing PCLKB. The STCLK [5:0] bits set the division value from PCLKB. The division value is determined by the following expression:

Division value = (STCLK[5:0] + 1) × 2

The STCLK frequency should be set to 0.5 MHz (2 µs).

DCMODE bit (CTSU Current Measurement Mode Select)

The DCMODE bit selects the capacitance measurement mode by switched-capacitor or the current measurement mode. In the current measurement mode, the switched-capacitor operation turns off and current is measured.

DCBACK bit (CTSU Current Measurement Feedback Select)

When DCMODE = 1, the DCBACK bit is enabled. When DCBACK = 1, the voltage of the TS pin is referenced during measurement.