The SPBYT bit of SPI Data Control Register (SPDCR) is added.

[before] example: RA2A1

**SPI Data Control Register (SPDCR)**

Address(es): SPI0.SPDCR 4007 200Bh, SPI1.SPDCR 4007 210Bh

```
+----+----+----+----+----+----+----+
<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
```

**Bit**     | **Symbol** | **Bit name** | **Description** | **R/W**
---|---|---|---|---

b3 to b0: — Reserved These bits are read as 0. The write value should be 0. R/W

b4: SPRDTD SPI Receive/Transmit Data Select
0: Read SPDR/SPDR_HA values from the receive buffer
1: Read SPDR/SPDR_HA values from the transmit buffer (but only if the transmit buffer is empty). R/W

b5: SPLW SPI Word Access/Halfword Access Specification
0: Set SPDR_HA to valid for halfword access
1: Set SPDR to valid for word access. R/W

b7, b6: — Reserved These bits are read as 0. The write value should be 0. R/W

**SPRDTD bit (SPI Receive/Transmit Data Select)**

The SPRDTD bit selects whether the SPDR/SPDR_HA register reads values from the receive buffer or from the transmit buffer. If reading is from the transmit buffer, the last value written to the SPDR/SPDR_HA register is read. Reading the transmit buffer must be done after generation of the transmit buffer empty interrupt (SPSR.SPTEF is 1).

For details, see section 30.2.5, SPI Data Register (SPDR/SPDR_HA).
SPLW bit (SPI Word Access/Halfword Access Specification)
The SPLW bit specifies the access width for the SPDR register. Access to SPDR_HA in halfwords is valid when
the SPLW bit is 0 and access to the SPDR register in words is valid when the SPLW bit is 1. In addition, when the
SPLW bit is 0, set the SPI data length setting bits, SPCMD0.SPBI[3:0], from 8 to 16 bits. Do not perform any
operations when a data length of 20, 24, or 32 bits is specified.

SPI Data Control Register (SPDCR)
Address(es): SPI0.SPDCR 4007 200Bh, SPI1.SPDCR 4007 210Bh

![Diagram]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit name</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b3 to b0</td>
<td>—</td>
<td>Reserved</td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
</tbody>
</table>
| b4 | SPRDTD | SPI Receive/Transmit Data Select | 0: Read SPDR/SPDR_HA values from receive buffer  
1: Read SPDR/SPDR_HA values from transmit buffer, but only if the transmit buffer is empty | R/W |
| b5 | SPLW | SPI Word Access/Halfword Access Specification | 0: Set SPDR_HA to valid for halfword access  
1: Set SPDR to valid for word access | R/W |
| b6 | SPBYTE | SPI Byte Access Specification | 0: SPDR is accessed in halfword or word (SPLW is valid)  
1: SPDR is accessed in byte (SPLW is invalid). | R/W |
| b7 | — | Reserved | This bit is read as 0. The write value should be 0. | R/W |

SPRDTD bit (SPI Receive/Transmit Data Select)
The SPRDTD bit selects whether the SPDR/SPDR_HA register reads values from the receive buffer or from the
transmit buffer. If reading is from the transmit buffer, the last value written to the SPDR/SPDR_HA register is read.
Reading the transmit buffer must be done after generation of the transmit buffer empty interrupt (SPSR.SPTEF is
1).
For details, see section of SPI Data Register (SPDR/SPDR_HA).

SPLW bit (SPI Word Access/Halfword Access Specification)
The SPLW bit specifies the access width for the SPDR register. Access to SPDR_HA in halfwords is valid when
the SPLW bit is 0 and access to the SPDR register in words is valid when the SPLW bit is 1. In addition, when the
SPLW bit is 0, set the SPI data length setting bits, SPCMD0.SPBI[3:0], from 8 to 16 bits. Do not perform any
operations when a data length of 20, 24, or 32 bits is specified.

SPBYTE bit (SPI Byte Access Specification)
This bit is used to set the data width of access to the SPI Data Register (SPDR). When SPBYTE = 0, use word or
half word access to SPDR. When SPBYTE = 1 (in that case, SPLW is invalid), use byte access to SPDR. When
SPBYTE = 1, set the SPI data length bits (SPBI[3:0]) in the SPI Command Register n (SPCMDn) to 8 bits. If
SPBI[3:0] are set to 9 to 16, 20, 24, or 32 bit, subsequent operation is not guaranteed.